Multilayer ceramic capacitors

Feedthrough chip capacitors, X7R

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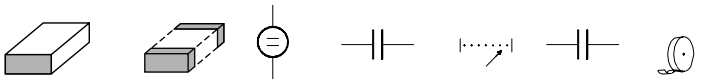
Ordering code system



B37872 U 5 222 S 0 11

Packaging

11 ≙ cardboard tape, 180-mm reel
12 ≙ blister tape, 180-mm reel

Internal coding

Capacitance tolerance

S ≙ +50% / –20% (standard for 1206)
Z ≙ +80% / –20% (standard for 1806)

Capacitance, coded (example)
222 ≙ 22 · 10^2 pF = 2.2 nF
472 ≙ 47 · 10^2 pF = 4.7 nF

Rated voltage

Rated voltage [VDC]	50
Code	5

Internal coding "U" indicates feedthrough chip capacitor

Type and size	
Chip size (**inch** / mm)	Temperature characteristic X7R
1206 / 3216 **1806** / 4616	B37872 B37971

SMD

Features

- Excellent EMI suppression
- Low parasitic inductance and low electrical losses
- High attenuation at higher natural resonant frequency
- Space saving on the PCB
- To AEC-Q200

Applications

- EMI suppression / Decoupling and filtering
- Noise suppression and broadband I/O filtering
- Automotive brake systems (e.g. ABS)
- Hall sensors

Termination

- For soldering: 4 terminations, nickel barrier terminations (Ni)

Options

- Alternative capacitance values, capacitance tolerances, C0G characteristic and feedthrough arrays available on request

Delivery mode

- Cardboard tape, 180-mm reel

Electrical data

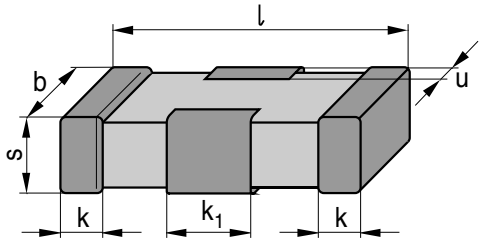
Temperature characteristic		X7R	
Max. relative capacitance change within –55 °C to +125 °C	$\Delta C/C$	±15	%
Climatic category (IEC 60068-1)		55/125/56	
Standard		EIA	
Dielectric		Class 2	
Rated voltage[1)]	V_R	50	VDC
Test voltage	V_{test}	$2.5 \cdot V_R$/5 s	VDC
Capacitance range / E series	C_R	2.2 nF … 10 nF (E3); 220 nF	
Dissipation factor (limit value)	tan δ	$<25 \cdot 10^{-3}$	
DC resistance	R_{DC}	<600	mΩ
Insulation resistance[2)] at + 25 °C	R_{ins}	$>10^5$	MΩ
Insulation resistance[2)] at +125 °C	R_{ins}	$>10^4$	MΩ
Time constant[2)] at + 25 °C	τ	>1000	s
Time constant[2)] at +125 °C	τ	>100	s
Operating temperature range	T_{op}	–55 … +125	°C
Ageing[3)]		yes	

1) Note: No operation on AC line.
2) For C_R >10 nF the time constant $\tau = C \cdot R_{ins}$ is given.
3) Refer to chapter “General technical information”, “Ageing”.

Capacitance tolerances

Code letter	S (standard for 1206)	Z (standard for 1806)
Tolerance	+50/–20%	+80/–20%

Dimensional drawing



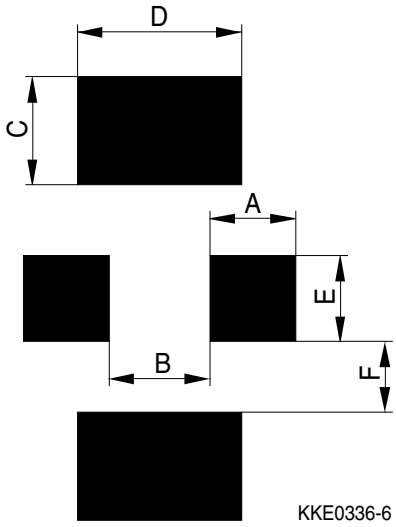
KKE0328-F

Dimensions (mm)

Case size (inch) (mm)	1206 3216	1806 4616
l	3.2 ±0.20	4.6 ±0.20
b	1.6 ±0.15	1.6 ±0.30
s	0.9 max.	1.2 max.
k	0.4 ±0.2	0.4 ±0.3
k_1	1.0 ±0.35	1.5 ±0.3
u	0.2 +0.2/–0.1	0.3 +0.3/–0.2

Tolerances to CECC 32101-801

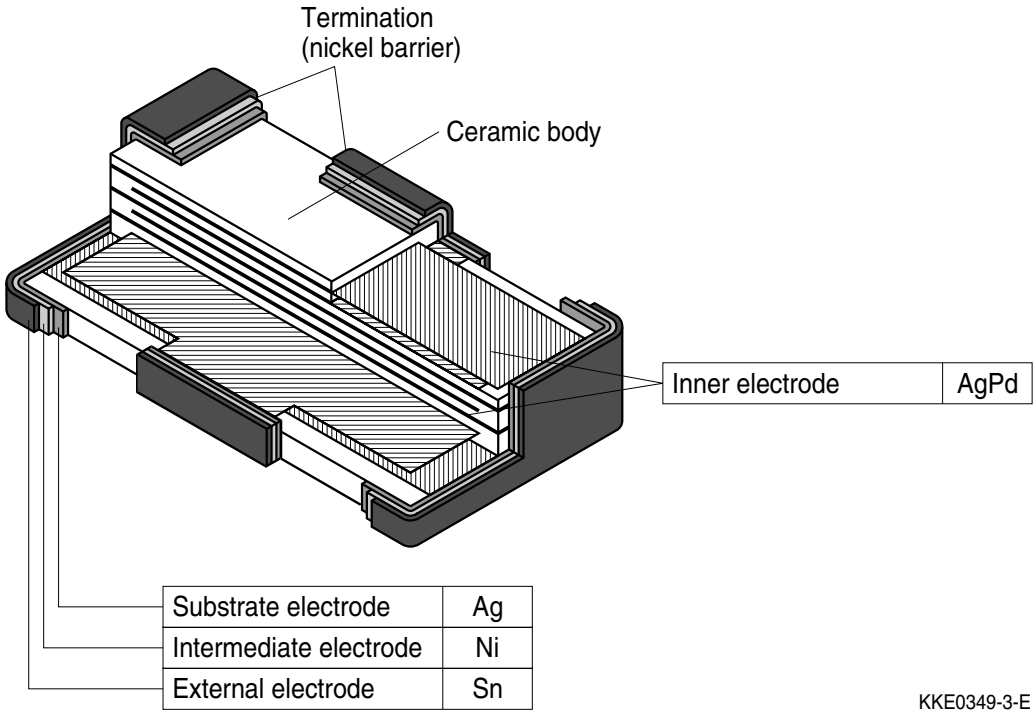
Recommended solder pad

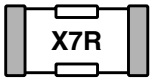


Recommended dimensions (mm) for reflow soldering

Case size (inch/mm)	Type	A	B	C	D	E	F
1206/3216	feedthrough chip	0.73 … 0.83	0.93 … 1.20	0.80 … 0.90	1.00 … 1.40	0.73 … 0.83	0.74 … 0.85
1806/4616	feedthrough chip	1.00	0.60	1.00	2.00	1.50	1.00

Termination





Product range feedthrough capacitors, X7R

Size[1)] **inch** mm	**1206** 3216	**1806** 4616
Type	B37872	B37971
V_R (VDC) C_R	50	50
2.2 nF		
4.7 nF		
10 nF		
220 nF		

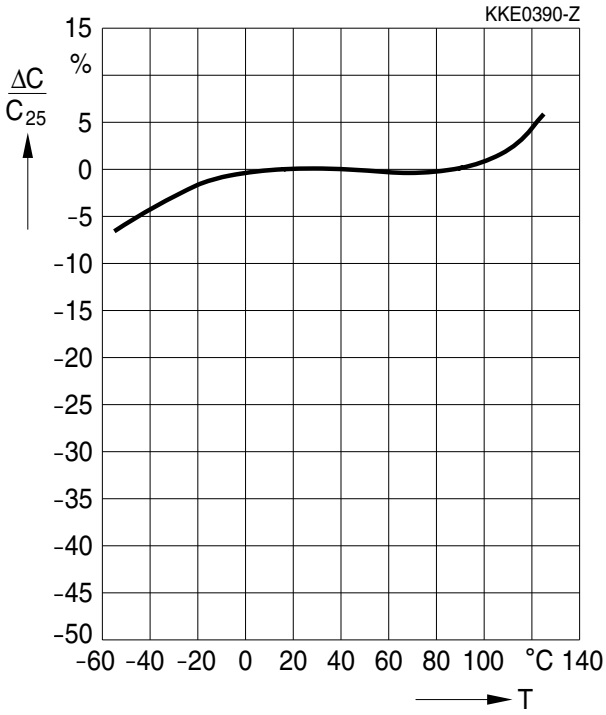
Ordering codes and packing for X7R feedthrough capacitors, 50 VDC, nickel barrier terminations

		Chip thickness	Cardboard tape, ∅ 180-mm reel	Blister tape, ∅ 180-mm reel
			** ≙ 11	** ≙ 12
C_R[2)]	Ordering code	mm	pcs/reel	pcs/reel
Case size 1206, 50 VDC				
2.2 nF	B37872U5222S0**	0.8 ±0.1	4000	—
4.7 nF	B37872U5472S0**	0.8 ±0.1	4000	—
10 nF	B37872U5103S0**	0.8 ±0.1	4000	—
Case size 1806, 50 VDC				
220 nF	B37971U5224Z0**	1.0 ±0.2	—	3000

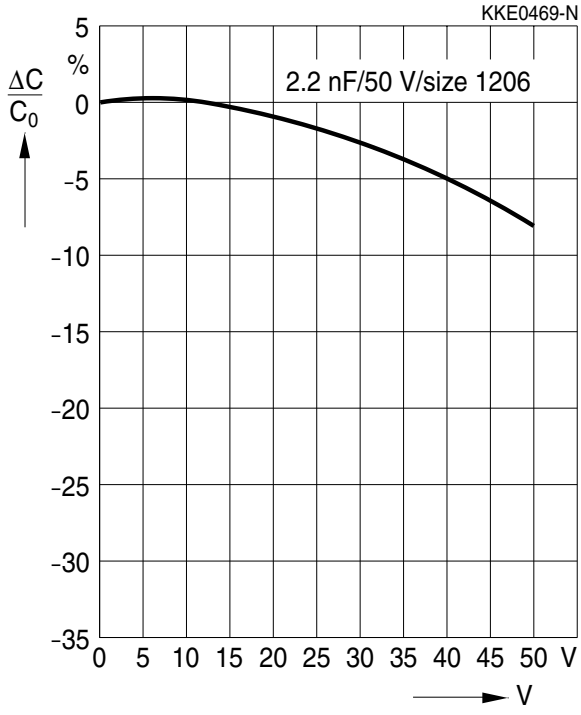
1) l × b (inch) / l × b (mm)
2) Other capacitance values on request.

Typical characteristics[1)]

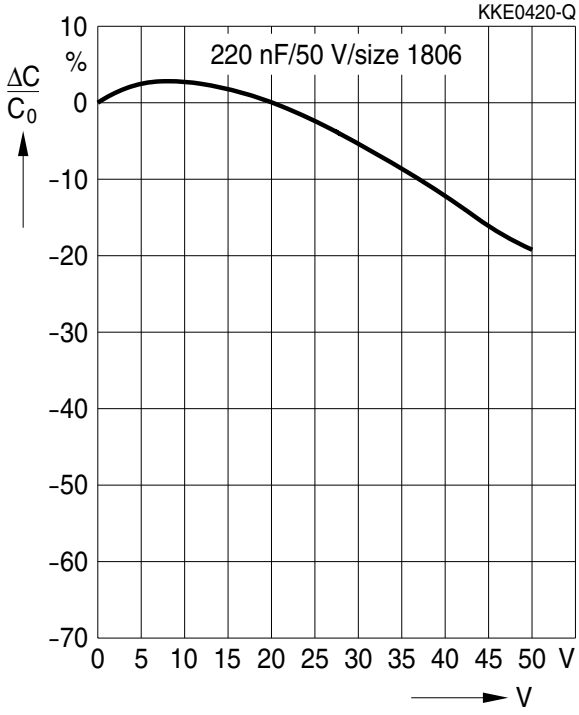
Capacitance change $\Delta C/C_{25}$ versus temperature T



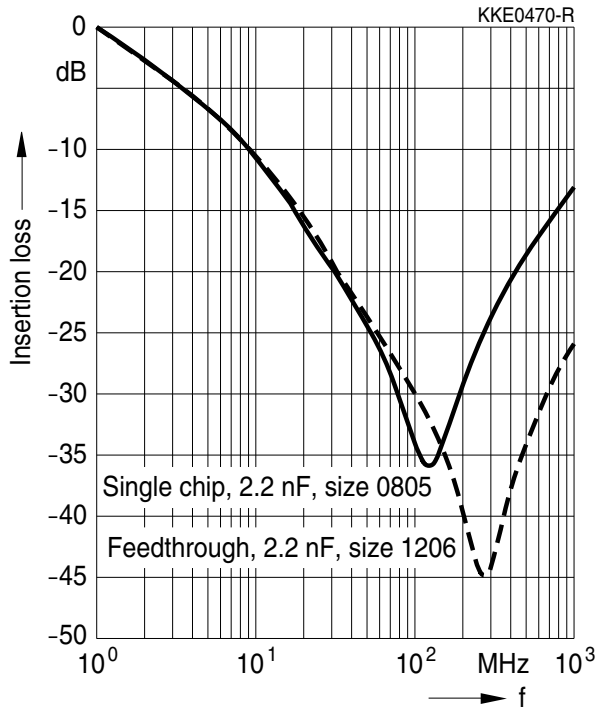
Capacitance change $\Delta C/C_0$ versus superimposed DC voltage V



Capacitance change $\Delta C/C_0$ versus superimposed DC voltage V



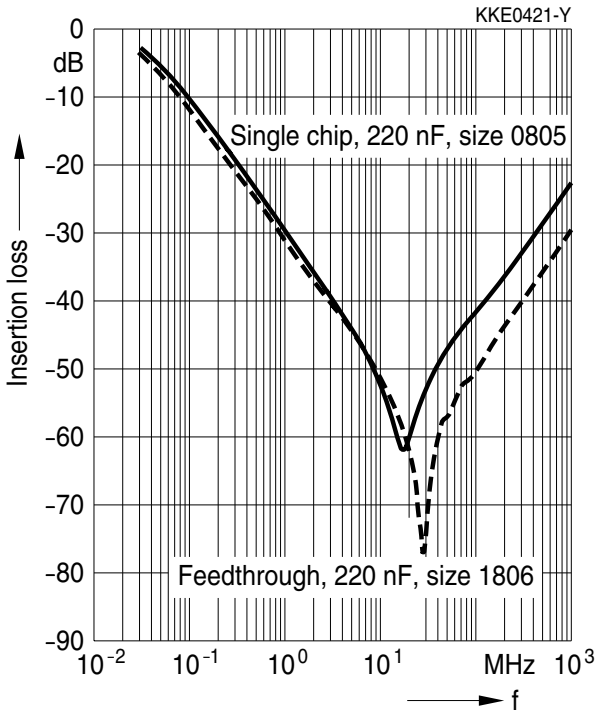
Insertion loss dB versus frequency f



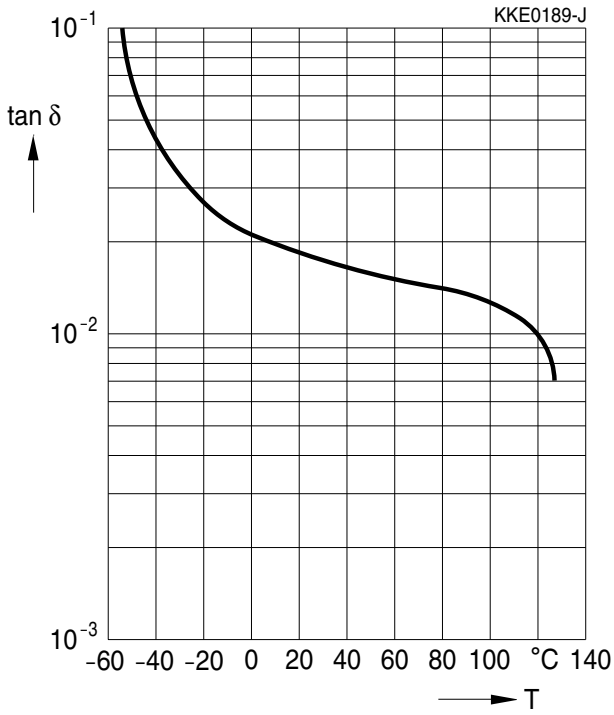
1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Typical characteristics[1)]

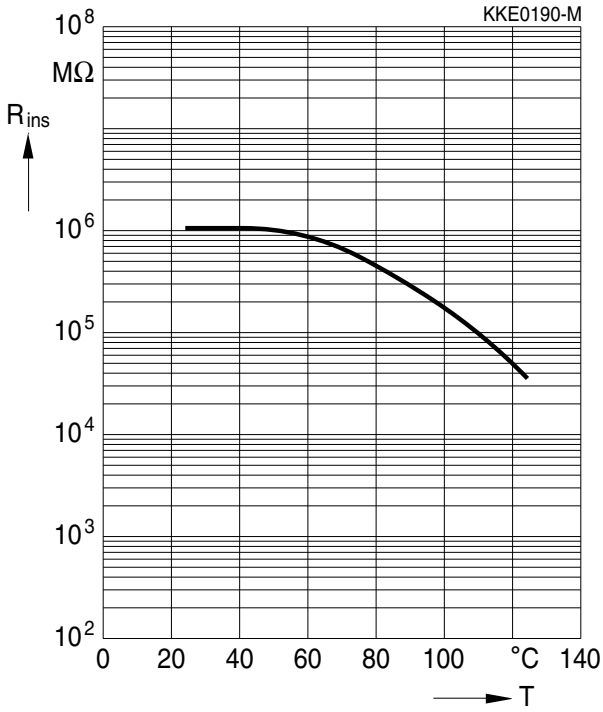
Insertion loss dB versus frequency f



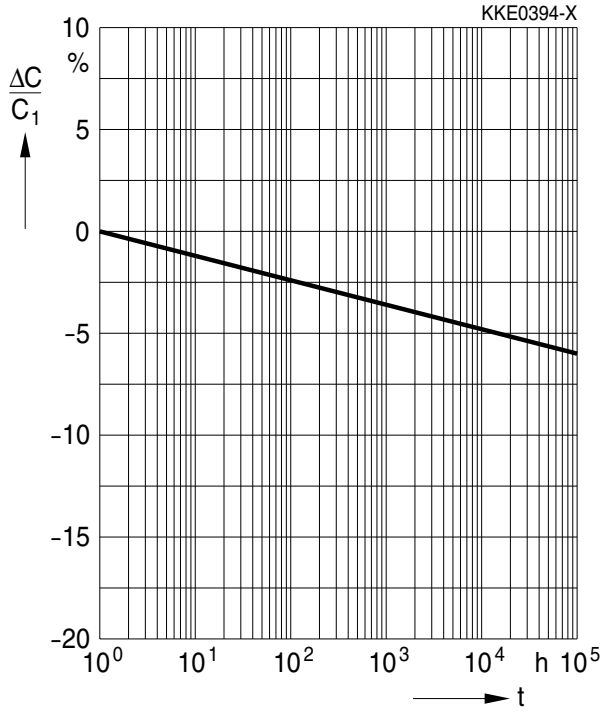
Dissipation factor tan δ versus temperature T



Insulation resistance R_{ins} versus temperature T



Capacitance change $\Delta C/C_1$ versus time t



1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Notes on the selection of ceramic capacitors

In the selection of ceramic capacitors, the following criteria must be considered:

1. Depending on the application, ceramic capacitors used to meet high quality requirements should at least satisfy the specifications to AEC-Q200. They must meet quality requirements going beyond this level in terms of ruggedness (e.g. mechanical, thermal or electrical) in the case of critical circuit configurations and applications (e.g. in safety-relevant applications such as ABS and airbag equipment or durable industrial goods).
2. At the connection to the battery or power supply (e.g. clamp 15 or 30 in the automobile) and at positions with stranding potential, to reduce the probability of short circuits following a fracture, two ceramic capacitors must be connected in series and/or a ceramic capacitor with integrated series circuit should be used. The MLSC from EPCOS contains such a series circuit in a single component.
3. Ceramic capacitors with the temperature characteristics Z5U and Y5V do not satisfy the requirements to AEC-Q200 and are mechanically and electrically less rugged than C0G or X7R/X8R ceramic capacitors. In applications that must satisfy high quality requirements, therefore, these capacitors should not be used as discrete components (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
4. For ESD protection, preference should be given to the use of multilayer varistors (MLV) (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
5. An application-specific derating or continuous operating voltage must be considered in order to cushion (unexpected) additional stresses (see the chapter “Reliability”).

The following should be considered in circuit board design

1. If technically feasible in the application, preference should be given to components having an optimal geometrical design.
2. At least FR4 circuit board material should be used.
3. Geometrically optimal circuit boards should be used, ideally those that cannot be deformed.
4. Ceramic capacitors must always be placed a sufficient minimum distance from the edge of the circuit board. High bending forces may be exerted there when the panels are separated and during further processing of the board (such as when incorporating it into a housing).
5. Ceramic capacitors should always be placed parallel to the possible bending axis of the circuit board.
6. No screw connections should be used to fix the board or to connect several boards. Components should not be placed near screw holes. If screw connections are unavoidable, they must be cushioned (for instance by rubber pads).

The following should be considered in the placement process

1. Ensure correct positioning of the ceramic capacitor on the solder pad.
2. Caution when using casting, injection-molded and molding compounds and cleaning agents, as these may damage the capacitor.
3. Support the circuit board and reduce the placement forces.
4. A board should not be straightened (manually) if it has been distorted by soldering.
5. Separate panels with a peripheral saw, or better with a milling head (no dicing or breaking).
6. Caution in the subsequent placement of heavy or leaded components (e.g. transformers or snap-in components): danger of bending and fracture.
7. When testing, transporting, packing or incorporating the board, avoid any deformation of the board not to damage the components.
8. Avoid the use of excessive force when plugging a connector into a device soldered onto the board.
9. Ceramic capacitors must be soldered only by the mode (reflow or wave soldering) permissible for them (see the chapter “Soldering directions”).
10. When soldering the most gentle solder profile feasible should be selected (heating time, peak temperature, cooling time) in order to avoid thermal stresses and damage.
11. Ensure the correct solder meniscus height and solder quantity.
12. Ensure correct dosing of the cement quantity.
13. Ceramic capacitors with an AgPd external termination are not suited for the lead-free solder process: they were developed only for conductive adhesion technology.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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