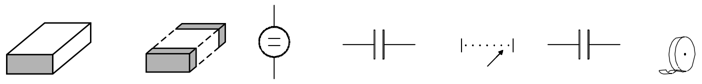
Multilayer ceramic capacitors

Chip capacitors, Z5U (Y5U)

Date: October 2006

Ordering code system



B37942 K 5 104 M 0 60

Packaging

60 ≙ cardboard tape, 180-mm reel
62 ≙ blister tape, 180-mm reel
70 ≙ cardboard tape, 330-mm reel
72 ≙ blister tape, 330-mm reel
01 ≙ bulk case

Internal coding

Capacitance tolerance

M ≙ ±20% (standard)

Capacitance, coded (example)

104 ≙ <u>10</u> · 10^4 pF = 100 nF
105 ≙ <u>10</u> · 10^5 pF = 1 µF
224 ≙ <u>22</u> · 10^4 pF = 220 nF

Rated voltage

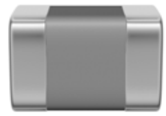
Rated voltage [VDC]	25	50
Code	0	5

Termination

Standard:
K ≙ nickel barrier for case sizes 0603, 0805, 1206, 1210
J ≙ silver-palladium for case sizes 1812, 2220

Type and size	
Chip size (**inch** / mm)	Temperature characteristic Z5U (Y5U)
0603 / 1608	B37932
0805 / 2012	B37942
1206 / 3216	B37873
1210 / 3225	B37951
1812 / 4532	B37954
2220 / 5750	B37957

Features



- Extremely high volumetric efficiency
- Non-linear capacitance change
- Y5U characteristic is also fulfilled

Applications

- Blocking
- Coupling
- Decoupling
- Interference suppression

Termination

- For soldering: Nickel barrier termination (Ni) for case sizes 0603 to 1210
  Silver-palladium termination (AgPd) for case sizes 1812 and 2220

Delivery mode

- Cardboard and blister tape (blister tape for chip thickness ≥1.2 ±0.1 mm and case sizes ≥1210), 180-mm and 330-mm reel available
- Bulk case for case sizes 0603 and 0805 (≥68 nF)

Electrical data

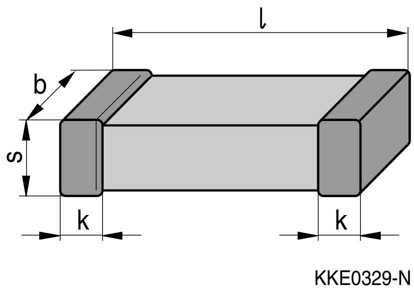
Temperature characteristic		Z5U (Y5U)[1]	
Max. relative capacitance change within –30 °C to +85 °C	$\Delta C/C$	+22/–56	%
Climatic category (IEC 60068-1)		30/85/56	
Standard		EIA	
Dielectric		Class 2	
Rated voltage[2]	V_R	25, 50	VDC
Test voltage	V_{test}	$2.5 \cdot V_R$/5 s	VDC
Capacitance range	C_R	10 nF … 4.7 µF	
Dissipation factor (limit value)	$\tan \delta$	$<50 \cdot 10^{-3}$	
Insulation resistance[3] at +25 °C	R_{ins}	$>10^4$	MΩ
Time constant[3] at +25 °C	τ	>500	s
Operating temperature range	T_{op}	–30 … +85	°C
Ageing[4]		yes	

1) Y5U specification is also fulfilled.
2) Note: No operation on AC line.
3) For C_R >10 nF the time constant $\tau = C \cdot R_{ins}$ is given.
4) Refer to chapter “General technical information”, “Ageing”.

Capacitance tolerances

Code letter	M (standard)
Tolerance	±20%

Dimensional drawing



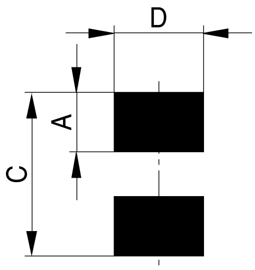
Dimensions (mm)

Case size (inch) (mm)	0603 1608	0805 2012	1206 3216	1210 3225
l	1.6 ±0.15	2.00 ±0.20	3.2 ±0.20	3.2 ±0.30
b	0.8 ±0.10	1.25 ±0.15	1.6 ±0.15	2.5 ±0.30
s	0.8 ±0.10	1.30 max.	1.30 max.	1.30 max.
k	0.1 –0.4	0.13 –0.75	0.25 –0.75	0.25 –0.75

Case size (inch) (mm)	1812 4532	2220 5750
l	4.5 ±0.30	5.7 ±0.40
b	3.2 ±0.30	5.0 ±0.40
s	1.30 max.	1.30 max.
k	0.25 –1.0	0.25 –1.0

Tolerances to CECC 32101-801

Recommended solder pad



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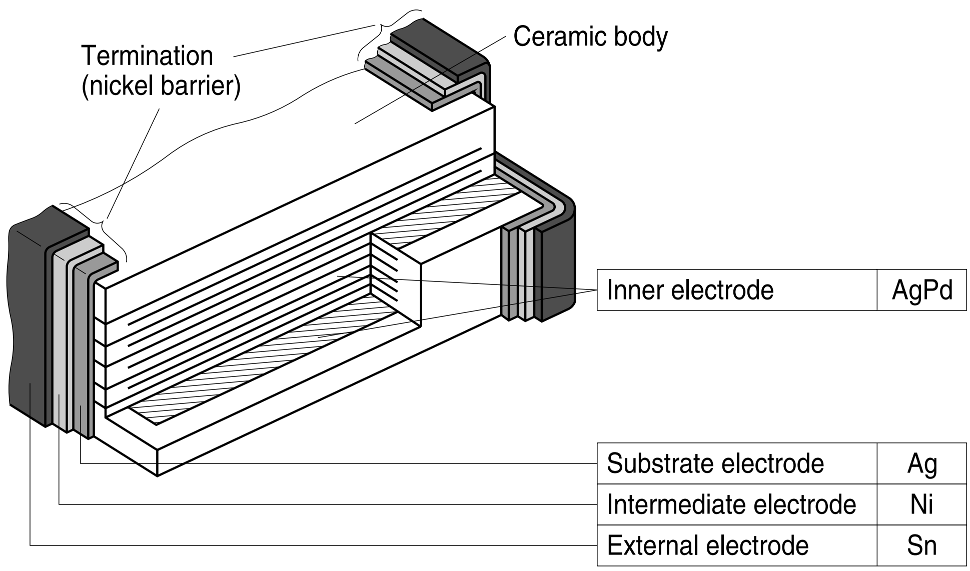
Recommended dimensions (mm) for reflow soldering

Case size (inch/mm)	Type	A	C	D
0603/1608	single chip	0.6 … 0.7	1.8 … 2.20	0.6 … 0.8
0805/2012	single chip	0.6 … 0.7	2.2 … 2.60	0.8 … 1.1
1206/3216	single chip	0.8 … 0.9	3.8 … 4.32	1.0 … 1.4
1210/3225	single chip	1.0 … 1.2	4.0 … 4.80	1.8 … 2.3
1812/4532	single chip	1.2 … 1.4	5.4 … 6.30	2.3 … 3.0
2220/5750	single chip	1.4 … 1.6	6.8 … 7.80	3.5 … 4.8

Termination



KKE0484-W

Product range chip capacitors, Z5U (Y5U)

Size[1)] **inch** mm	**0603** 1608		**0805** 2012		**1206** 3216		**1210** 3225		**1812** 4532		**2220** 5750	
Type	B37932		B37942		B37873		B37951		B37954		B37957	
V_R (VDC) / C_R	25	50	25	50	25	50		50		50		50
10 nF		■		■								
15 nF												
22 nF		■		■								
33 nF												
47 nF		■		■								
68 nF												
100 nF	■			■		■						
150 nF			■									
220 nF			■			■						
330 nF												
470 nF						■		■				
680 nF										■		
1.0 µF					■			■		■		■
1.5 µF										■		
2.2 µF												■
3.3 µF												
4.7 µF												■

1) l × b (inch) / l × b (mm)

Ordering codes and packing for Z5U (Y5U), 25 VDC, nickel barrier terminations

C_R	Ordering code	Chip thickness mm	Cardboard tape, ∅ 180-mm reel ** ≙ 60 pcs/reel	Cardboard tape, ∅ 330-mm reel ** ≙ 70 pcs/reel	Bulk case ** ≙ 01 pcs
Case size 0603, 25 VDC					
100 nF	B37932K0104M0**	0.8 ±0.1	4000	16000	15000
Case size 0805, 25 VDC					
150 nF	B37942K0154M0**	0.8 ±0.1	4000	16000	–
220 nF	B37942K0224M0**	0.8 ±0.1	4000	16000	–
Case size 1206, 25 VDC					
1.0 µF	B37873K0105M0**	1.2 ±0.1	3000[1]	12000[2]	–

Ordering codes and packing for Z5U (Y5U), 50 VDC, nickel barrier terminations

C_R	Ordering code	Chip thickness mm	Cardboard tape, ∅ 180-mm reel ** ≙ 60 pcs/reel	Cardboard tape, ∅ 330-mm reel ** ≙ 70 pcs/reel	Bulk case ** ≙ 01 pcs
Case size 0603, 50 VDC					
10 nF	B37932K5103M0**	0.8 ±0.1	4000	16000	15000
22 nF	B37932K5223M0**	0.8 ±0.1	4000	16000	15000
47 nF	B37932K5473M0**	0.8 ±0.1	4000	16000	15000
Case size 0805, 50 VDC					
10 nF	B37942K5103M0**	0.6 ±0.1	5000	20000	10000
22 nF	B37942K5223M0**	0.6 ±0.1	5000	20000	10000
47 nF	B37942K5473M0**	0.6 ±0.1	5000	20000	10000
100 nF	B37942K5104M0**	0.8 ±0.1	4000	16000	–
Case size 1206, 50 VDC					
100 nF	B37873K5104M0**	0.8 ±0.1	4000	16000	–
220 nF	B37873K5224M0**	0.8 ±0.1	4000	16000	–
470 nF	B37873K5474M0**	1.2 ±0.1	3000[1]	12000[2]	–
Case size 1210, 50 VDC					
470 nF	B37951K5474M0**	0.8 ±0.1	4000[1]	16000[2]	–
1.0 µF	B37951K5105M0**	1.2 ±0.1	3000[1]	12000[2]	–

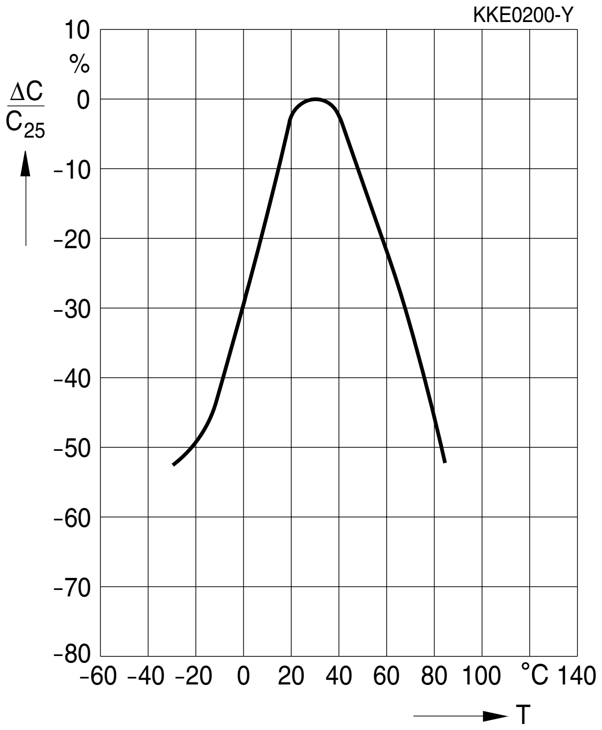
1) Blister tape, 180-mm reel, ordering code ** ≙ 62
2) Blister tape, 330-mm reel, ordering code ** ≙ 72

Ordering codes and packing for Z5U (Y5U), 50 VDC, silver-palladium terminations

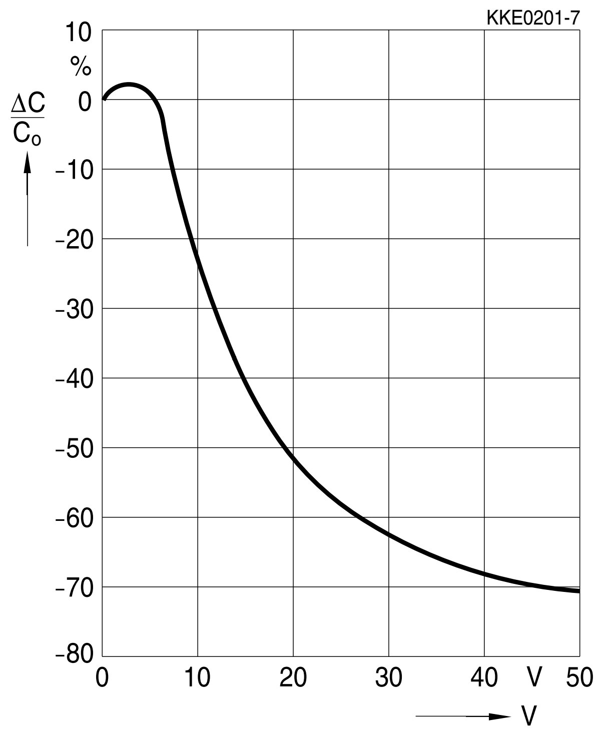
C_R	Ordering code	Chip thickness mm	Blister tape, ∅ 180-mm reel ** ≙ 62 pcs/reel	Blister tape, ∅ 330-mm reel ** ≙ 72 pcs/reel
Case size 1812, 50 VDC				
680 nF	B37954J5684M0**	1.2 ±0.1	1500	5000
1.0 µF	B37954J5105M0**	1.2 ±0.1	1500	5000
1.5 µF	B37954J5155M0**	1.2 ±0.1	1500	5000
Case size 2220, 50 VDC				
1.0 µF	B37957J5105M0**	1.2 ±0.1	1500	5000
2.2 µF	B37957J5225M0**	1.2 ±0.1	1500	5000
4.7 µF	B37957J5475M0**	1.2 ±0.1	1500	5000

Typical characteristics

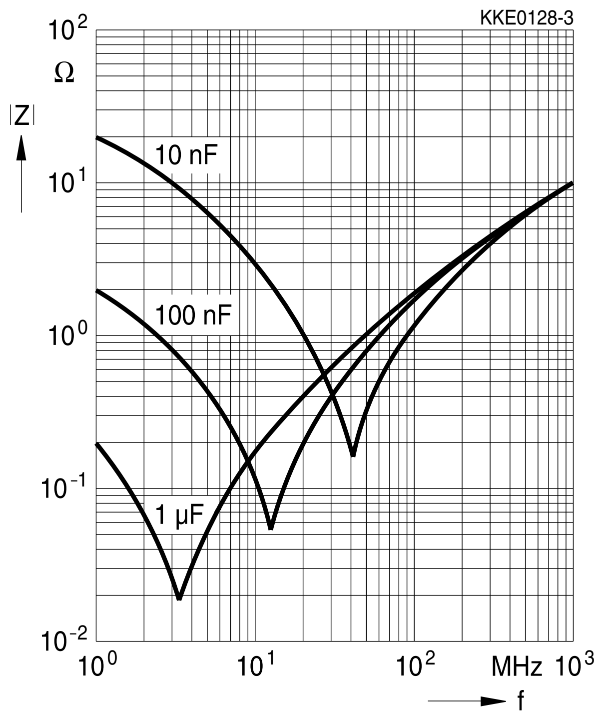
Capacitance change $\Delta C/C_{25}$ versus temperature T



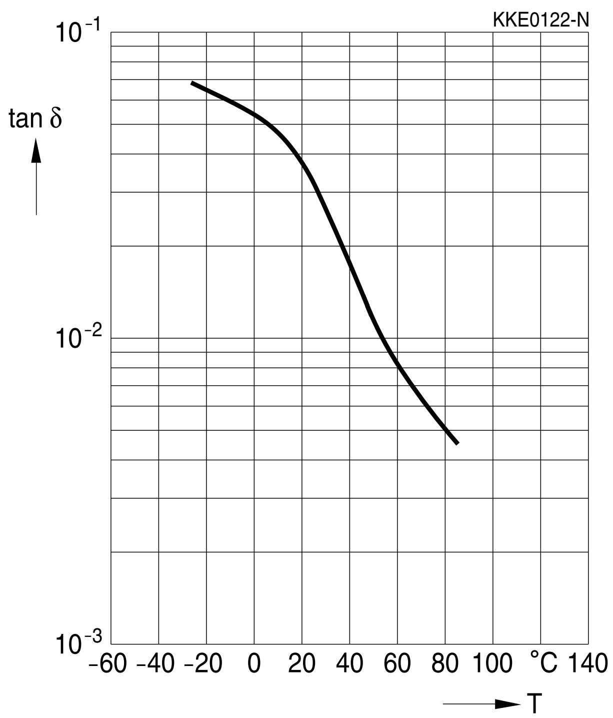
Capacitance change $\Delta C/C_0$ versus superimposed DC voltage V



Impedance |Z| versus frequency f

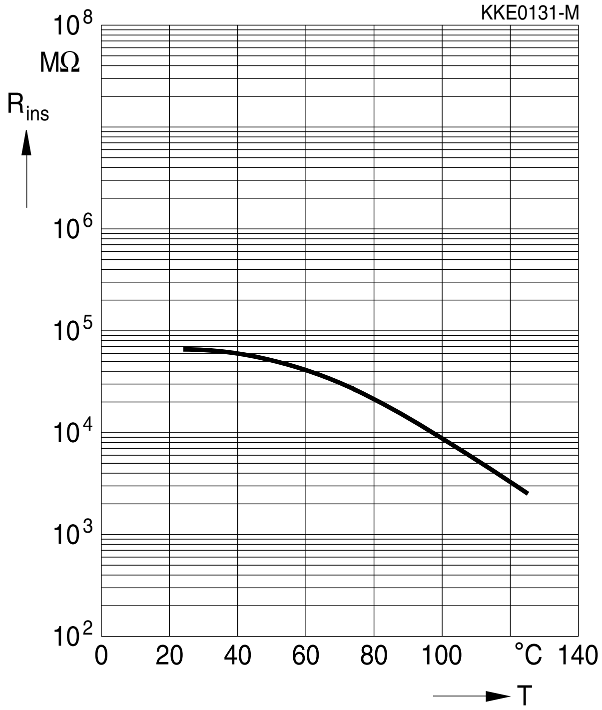


Dissipation factor tan δ versus temperature T

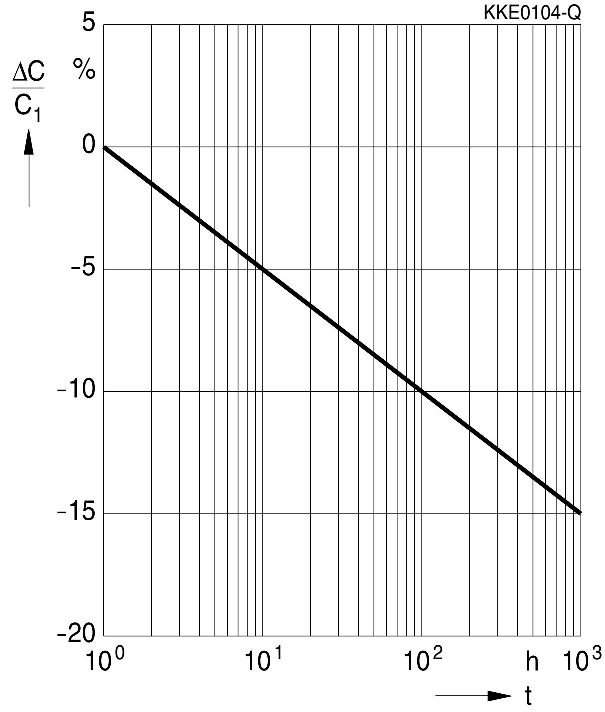


Typical characteristics

Insulation resistance R_{ins} versus temperature T



Capacitance change $\Delta C/C_1$ versus time t



Notes on the selection of ceramic capacitors

In the selection of ceramic capacitors, the following criteria must be considered:

1. Depending on the application, ceramic capacitors used to meet high quality requirements should at least satisfy the specifications to AEC-Q200. They must meet quality requirements going beyond this level in terms of ruggedness (e.g. mechanical, thermal or electrical) in the case of critical circuit configurations and applications (e.g. in safety-relevant applications such as ABS and airbag equipment or durable industrial goods).
2. At the connection to the battery or power supply (e.g. clamp 15 or 30 in the automobile) and at positions with stranding potential, to reduce the probability of short circuits following a fracture, two ceramic capacitors must be connected in series and/or a ceramic capacitor with integrated series circuit should be used. The MLSC from EPCOS contains such a series circuit in a single component.
3. Ceramic capacitors with the temperature characteristics Z5U and Y5V do not satisfy the requirements to AEC-Q200 and are mechanically and electrically less rugged than C0G or X7R/X8R ceramic capacitors. In applications that must satisfy high quality requirements, therefore, these capacitors should not be used as discrete components (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
4. For ESD protection, preference should be given to the use of multilayer varistors (MLV) (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
5. An application-specific derating or continuous operating voltage must be considered in order to cushion (unexpected) additional stresses (see the chapter “Reliability”).

The following should be considered in circuit board design

1. If technically feasible in the application, preference should be given to components having an optimal geometrical design.
2. At least FR4 circuit board material should be used.
3. Geometrically optimal circuit boards should be used, ideally those that cannot be deformed.
4. Ceramic capacitors must always be placed a sufficient minimum distance from the edge of the circuit board. High bending forces may be exerted there when the panels are separated and during further processing of the board (such as when incorporating it into a housing).
5. Ceramic capacitors should always be placed parallel to the possible bending axis of the circuit board.
6. No screw connections should be used to fix the board or to connect several boards. Components should not be placed near screw holes. If screw connections are unavoidable, they must be cushioned (for instance by rubber pads).

The following should be considered in the placement process

1. Ensure correct positioning of the ceramic capacitor on the solder pad.
2. Caution when using casting, injection-molded and molding compounds and cleaning agents, as these may damage the capacitor.
3. Support the circuit board and reduce the placement forces.
4. A board should not be straightened (manually) if it has been distorted by soldering.
5. Separate panels with a peripheral saw, or better with a milling head (no dicing or breaking).
6. Caution in the subsequent placement of heavy or leaded components (e.g. transformers or snap-in components): danger of bending and fracture.
7. When testing, transporting, packing or incorporating the board, avoid any deformation of the board not to damage the components.
8. Avoid the use of excessive force when plugging a connector into a device soldered onto the board.
9. Ceramic capacitors must be soldered only by the mode (reflow or wave soldering) permissible for them (see the chapter “Soldering directions”).
10. When soldering the most gentle solder profile feasible should be selected (heating time, peak temperature, cooling time) in order to avoid thermal stresses and damage.
11. Ensure the correct solder meniscus height and solder quantity.
12. Ensure correct dosing of the cement quantity.
13. Ceramic capacitors with an AgPd external termination are not suited for the lead-free solder process: they were developed only for conductive adhesion technology.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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