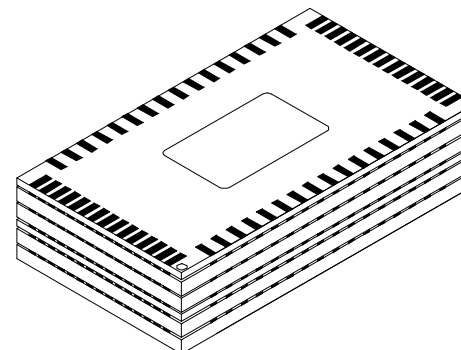


**ADVANCED INFORMATION**

**DESCRIPTION:**

The DP3S128X32Y5 is the 128K x 32 SRAM module the utilize the new and innovative space saving TSOP stacking technology. The module is constructed of four 128K x 8 SRAM's that are configured as 128K x 32.

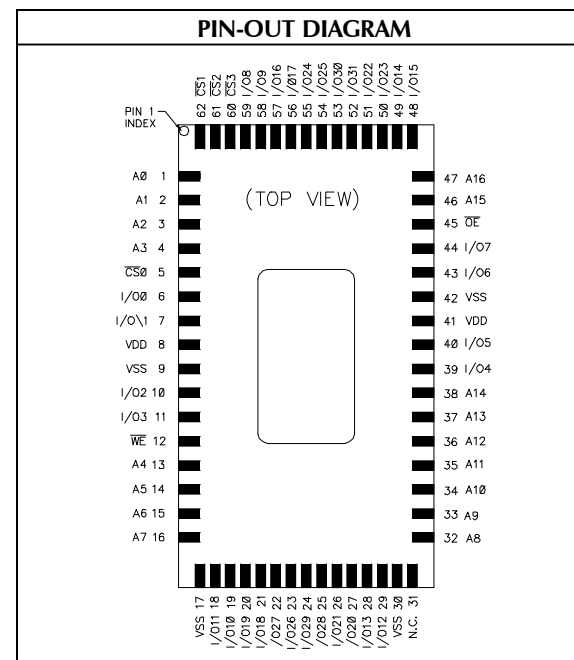
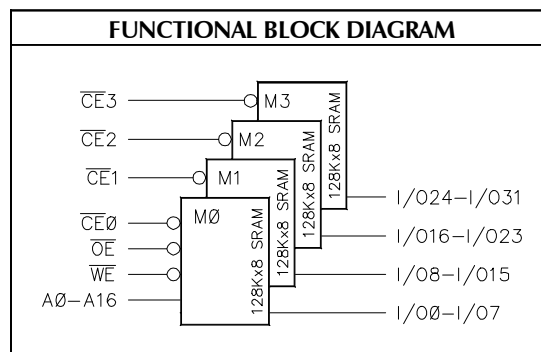
The DP3S128X32Y5 provides for a compatible upgrade path to lower density compatible modules. The module features high speed access times with common data inputs and outputs.



**FEATURES:**

- Organizations Available:  
128K x 32, 256K x 16 or 512K x 8
- Access Times: 10, 12, 15ns
- Fully Static Operation  
- No clock or refresh required
- Single +3.3V Power Supply,  $\pm 10\%$  Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Package: 64-Pin TSOP Stack

PIN NAMES	
A0 - A16	Address
I/O0 - I/O31	Data Input / Output
$\overline{CE}0 - \overline{CE}3$	Low Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$V_{DD}$	Power (+3.3V)
VSS	Ground
N.C.	No Connect



## ADVANCED INFORMATION

RECOMMENDED OPERATING RANGE<sup>3</sup>

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>IH</sub>	Input HIGH Voltage	2.0		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage	-0.3 <sup>2</sup>		0.8	V
T <sub>A</sub>	Operating Temperature	C	0	+25	°C
		CI	-40	+25	
				+70	
				+85	

CAPACITANCE<sup>4</sup>: T<sub>A</sub> = +25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C <sub>ADR</sub>	Address Input	35	pF	V <sub>IN</sub> <sup>2</sup> = 0V
C <sub>CE</sub>	Chip Enable	15		
C <sub>WE</sub>	Write Enable	35		
C <sub>OE</sub>	Output Enable	35		
C <sub>I/O</sub>	Data Input/Output	15		

## AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

## OUTPUT LOAD

Load	C <sub>L</sub>	Parametric Measured
1	30pF	except t <sub>LZ</sub> , t <sub>HZ</sub> , t <sub>OHZ</sub> , t <sub>OLZ</sub> and t <sub>WHZ</sub>
2	5pF	t <sub>LZ</sub> , t <sub>HZ</sub> , t <sub>OHZ</sub> , t <sub>OLZ</sub> and t <sub>WHZ</sub>

## TRUTH TABLE

Mode	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D <sub>OUT</sub> Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D <sub>OUT</sub>	Active
Write	L	L	X	D <sub>IN</sub>	Active

H = HIGH

L = LOW

X = Don't Care

ABSOLUTE MAXIMUM RATING<sup>3</sup>

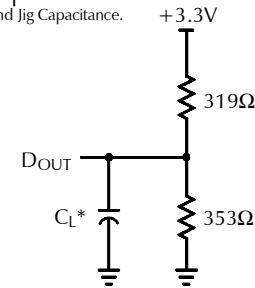
Symbol	Parameter	Max.	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.5 to +4.6	V
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to +4.6	V

## DC OUTPUT CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>OH</sub>	HIGH Voltage	I <sub>OH</sub> = -4mA	2.4		V
V <sub>OL</sub>	LOW Voltage	I <sub>OL</sub> = 8mA		0.4	V

Figure 1. Output Load

\* Including Probe and Jig Capacitance.



## DC OPERATING CHARACTERISTICS: Over Operating Ranges

Symbol	Characteristics	Test Condition	Min.	Max.	Unit
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-8	+8	μA
I <sub>OUT</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>DD</sub> , $\overline{\text{CE}}$ or $\overline{\text{OE}}$ = V <sub>IH</sub> or $\overline{\text{WE}}$ = V <sub>IL</sub>	-2	+2	μA
I <sub>CC</sub>	Operating Supply Current	Cycle = min., Duty = 100%, I <sub>OUT</sub> = 0mA	X8	355	mA
			X16	450	
			X32	640	
I <sub>SB1</sub>	Full Standby Standby Current	V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> +0.2V		180	mA
I <sub>SB2</sub>	Standby Current (TTL)	$\overline{\text{CE}}$ = V <sub>IH</sub>		260	mA
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 8.0mA		0.4	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4.0mA	2.4		V

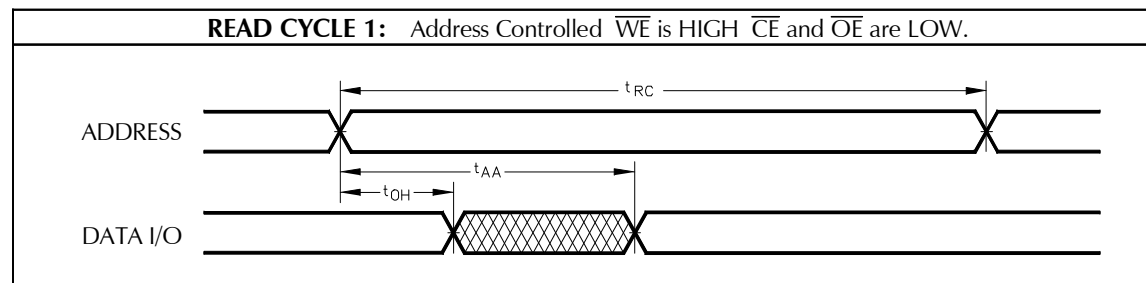
Note: Typical measurements made at +25°C. Cycle = min., V<sub>DD</sub> = 5.0V.

## ADVANCED INFORMATION

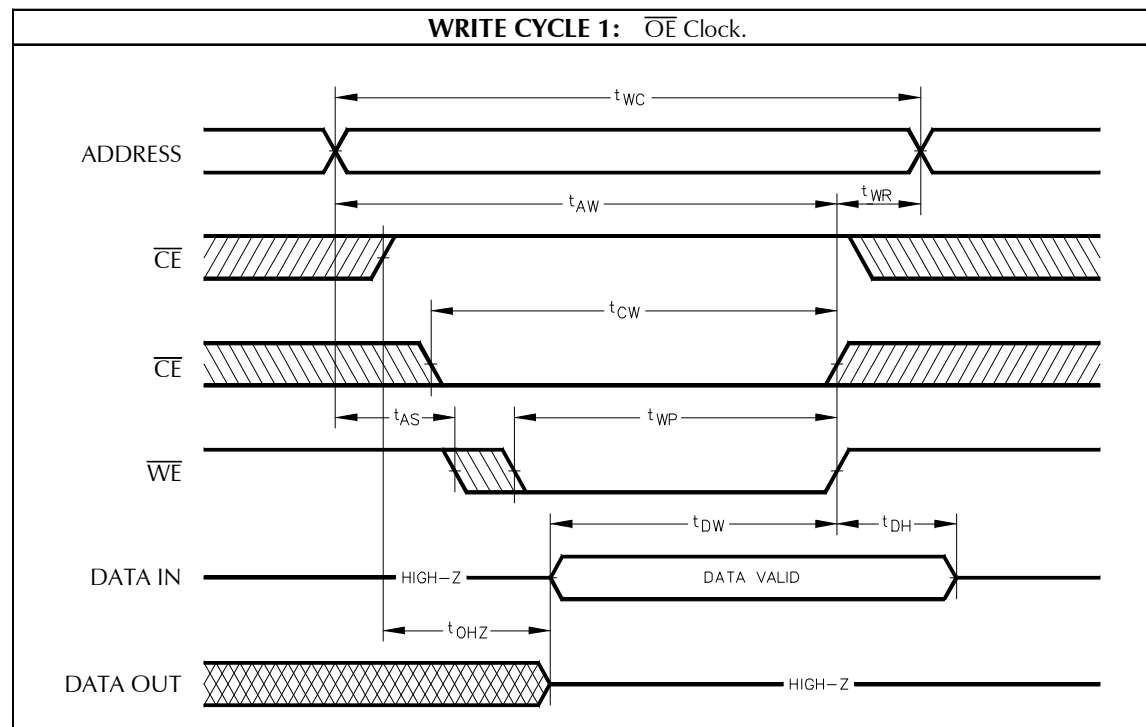
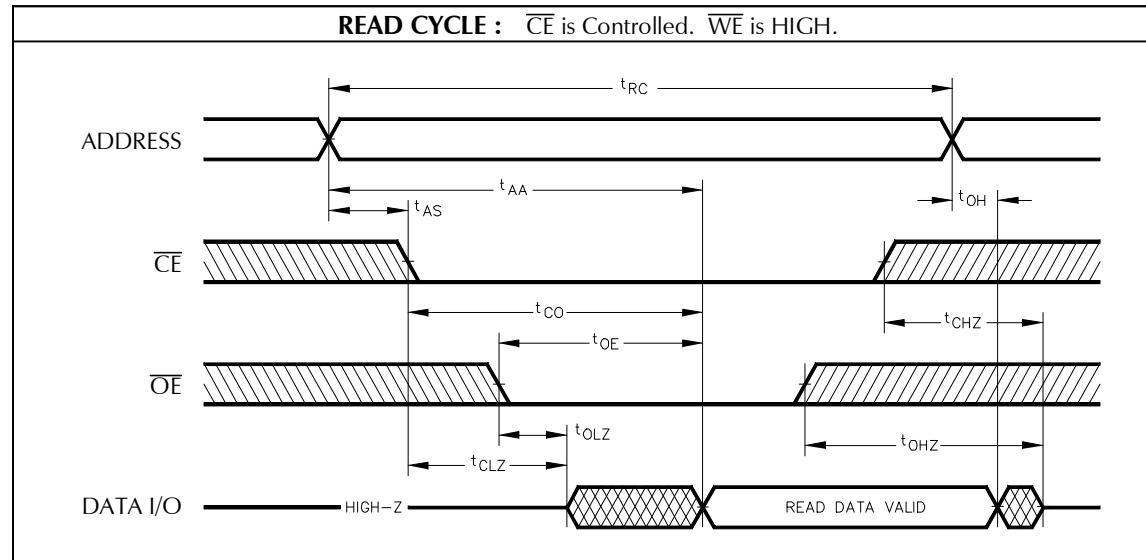
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over Operating Ranges									
No.	Symbol	Parameter	10ns		12ns		15ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>RC</sub>	Read Cycle Time	10		12		15		ns
2	t <sub>AA</sub>	Address Cycle Time		10		12		15	ns
3	t <sub>CO</sub>	Chip Enable Access Time		10		12		15	ns
4	t <sub>OE</sub>	Output Enable to Output Valid		5		6		7	ns
5	t <sub>CLZ</sub>	Chip Enable to Output in LOW-Z <sup>4, 6</sup>	3		3		3		ns
6	t <sub>OLZ</sub>	Output Enable to Output in LOW-Z <sup>4, 5</sup>	0		0		0		ns
7	t <sub>CHZ</sub>	Chip Enable to Output in HIGH-Z <sup>4, 5</sup>	0	5	0	6	0	7	ns
8	t <sub>OHZ</sub>	Output Enable to Output in HIGH-Z <sup>4, 5</sup>	0	5	0	6	0	7	ns
9	t <sub>OH</sub>	Output Hold from Address Change	3		3		3		ns

AC OPERATING CONDITION AND CHARACTERISTIC READ CYCLE: Over Operating Ranges <sup>6, 7</sup>									
No.	Symbol	Parameter	10ns		12ns		15ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
10	t <sub>WC</sub>	Write Cycle Time	10		12		15		ns
11	t <sub>AW</sub>	Address Valid to End of Write	8		9		10		ns
12	t <sub>CW</sub>	Chip Enable to End of Write	8		9		10		ns
13	t <sub>SA</sub>	Address Setup Time *	0		0		0		ns
14	t <sub>WP</sub>	Write Pulse Width ( $\overline{OE}$ High)	8		9		10		ns
15	t <sub>WP1</sub>	Write Pulse Width ( $\overline{OE}$ Low)	10		12		14		ns
16	t <sub>WR</sub>	Write Recovery Time	0		0		0		ns
17	t <sub>WHZ</sub>	Write Enable to Output in HIGH <sup>4, 5</sup>	0	5	0	6	0	7	ns
18	t <sub>DW</sub>	Data to Write Time Overlap	6		6		7		ns
19	t <sub>DH</sub>	Data Hold Time form Write Time	0		0		0		ns
20	t <sub>OW</sub>	Output Active from End of Write <sup>4, 5</sup>	3		3		3		ns

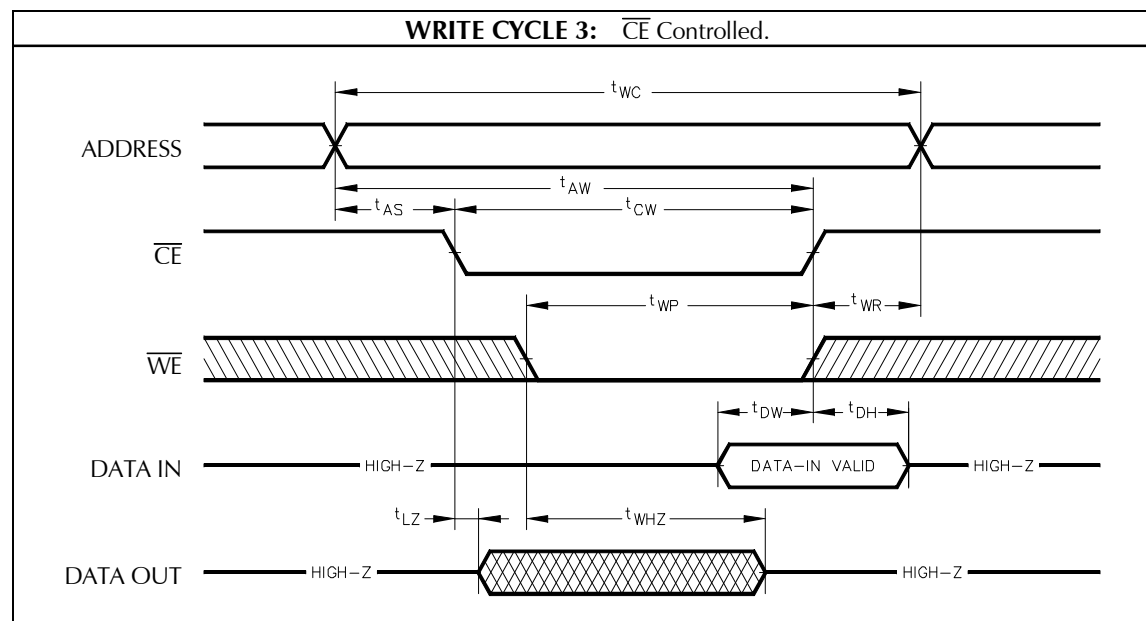
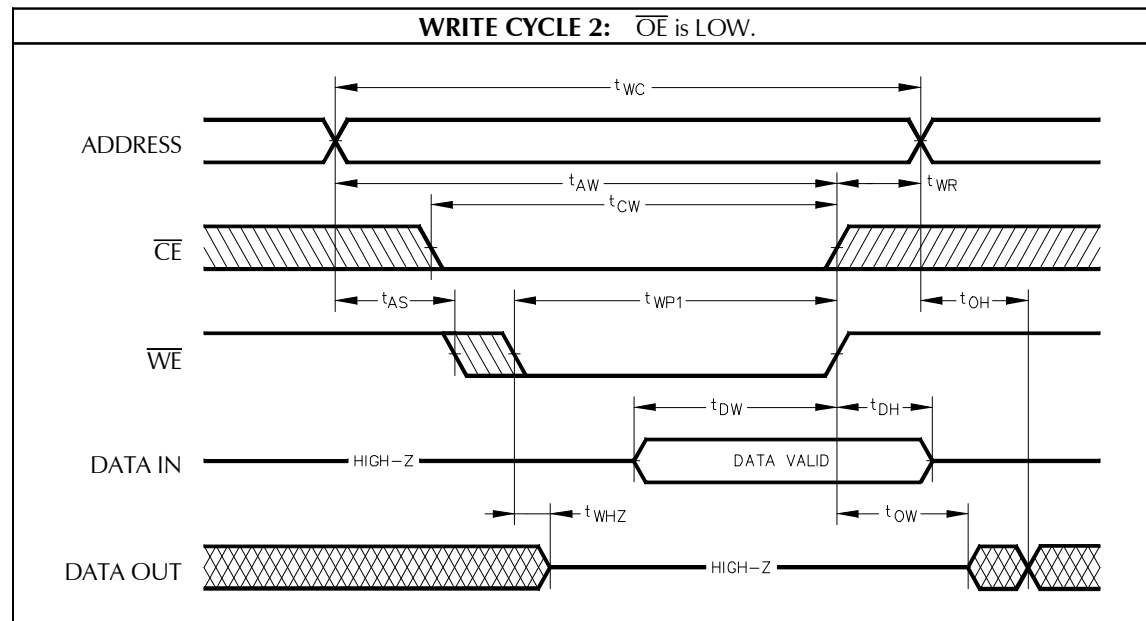
\* Valid for both Read and Write Cycles.



ADVANCED INFORMATION



## ADVANCED INFORMATION



ADVANCED INFORMATION

ORDERING INFORMATION

DP

3S

128

X

32

Y5

—

XX

X

PREFIX

TYPE

MEMORY DEPTH

DESIG

MEMORY WIDTH

PACKAGE

SPEED

GRADE

C

CI

10

12

15

64—PIN

TSOP STACK

MEMORY MODULE WITHOUT SUPPORT LOGIC

3.3 VOLT CMOS SRAM

COMMERCIAL

COMMERCIAL PROCESSED—

INDUSTRIAL TEMPERATURE

0°C to +70°C

—40°C to +85°C

10ns

12ns

15ns

NOTE:

1.

All voltages are with respect to V<sub>SS</sub>.
2.

-2.0V min. for pulse width less than 20ns (V<sub>IL</sub> min. = -0.5V at DC level).
3.

Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4.

This parameter is guaranteed and not 100% tested.
5.

Transition is measured at the point of ±500mV from steady state voltage.
6.

When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7.

The outputs are in a high impedance state when  $\overline{WE}$  is LOW.
8.

$\overline{CE}$  and  $\overline{WE}$  can initiate and terminate WRITE Cycle.

WAVEFORM KEY

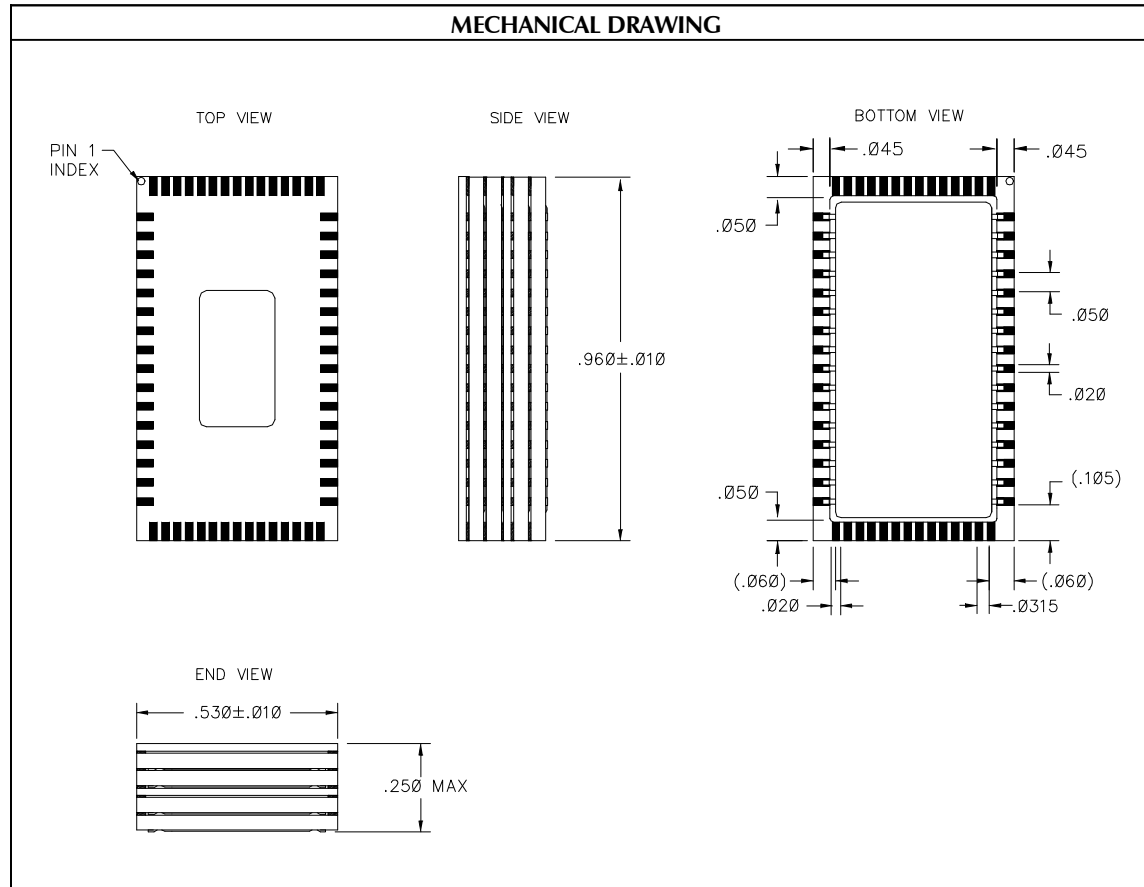
Data Valid  
HIGH to LOW

Transition from  
LOW to HIGH

Transition from  
or Don't Care

Data Undefined

## ADVANCED INFORMATION

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