Fast Logic

Pulse Width Controller

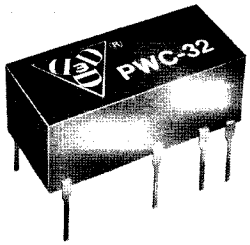
SERIES: PWC-32

TTL Interfaced
14 pin DIP

data delay devices, inc.

Features:

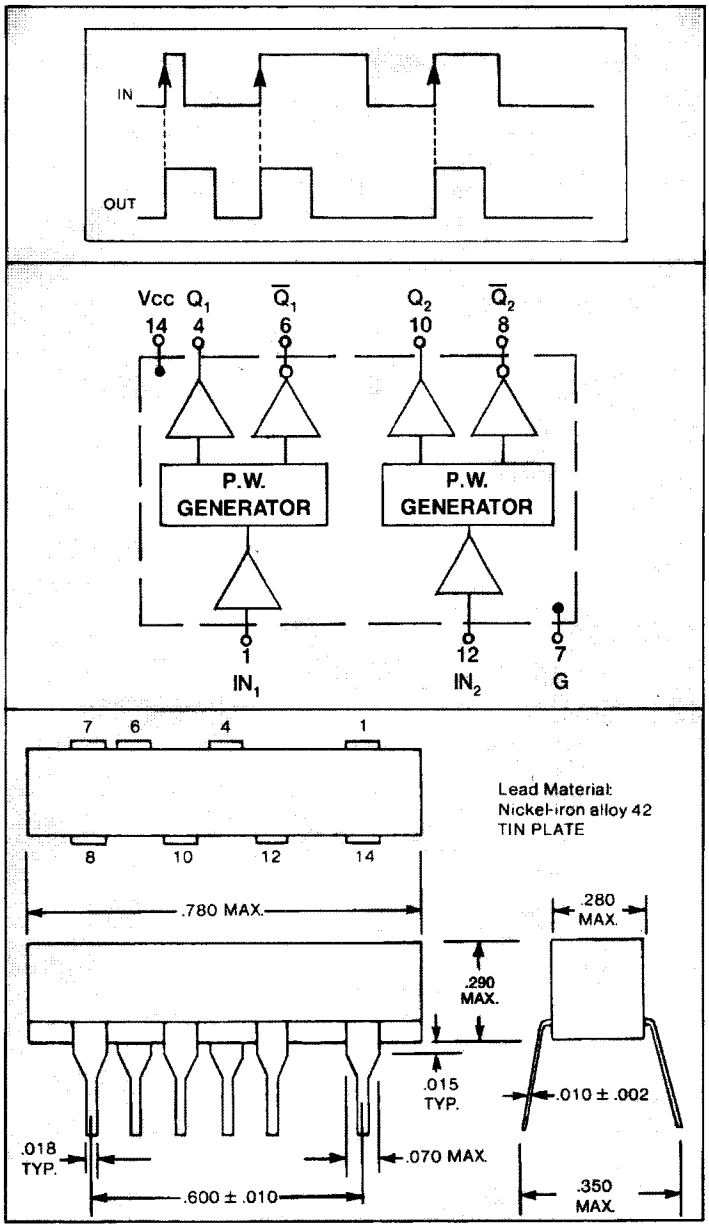
- **Two separate & equal pulse width controllers/package**
- **Exact control of pulse width**
- **Rising edge trigger**
- **Auto-insertable**
- **Low power consumption**
- **High speed**



Specifications:

- **Trigger inherent delay:** (T_{DO}) = 7 ns ± 1 ns.
  $(\overline{T_{DO}})$ = 9.5 ns ± 1 ns.
- **Pulse-width tolerance** = 5% or 2 ns (others on request).
- **Max. Input PRR** = PW + 20 ns.
- **Supply voltage:** 5 Vdc ± 5%.
- **Supply current:** 70 ma. typ.
- **Operating temperature:** 0°C to 70°C (–55° to 125°C on request).*
- **Temperature coefficient:** 100 PPM/°C.
- **Output rise-time:** 2 ns typ.
- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.

*DIL package used. E5 case.



Part Number	Pulse Width (ns)
PWC-32-5	5
PWC-32-10	10
PWC-32-15	15
PWC-32-20	20
PWC-32-30	30
PWC-32-40	40
PWC-32-50	50
PWC-32-60	60
PWC-32-75	75
PWC-32-100	100
PWC-32-125	125
PWC-32-150	150
PWC-32-175	175
PWC-32-200	200
PWC-32-250	250

Other pulse-widths available on request.

3 Mt. Prospect Avenue, Clifton, New Jersey 07013 ■ (973) 773-2299 ■ Fax (973) 773-9672