



# 1:10 Clock Fanout Buffer

## Features

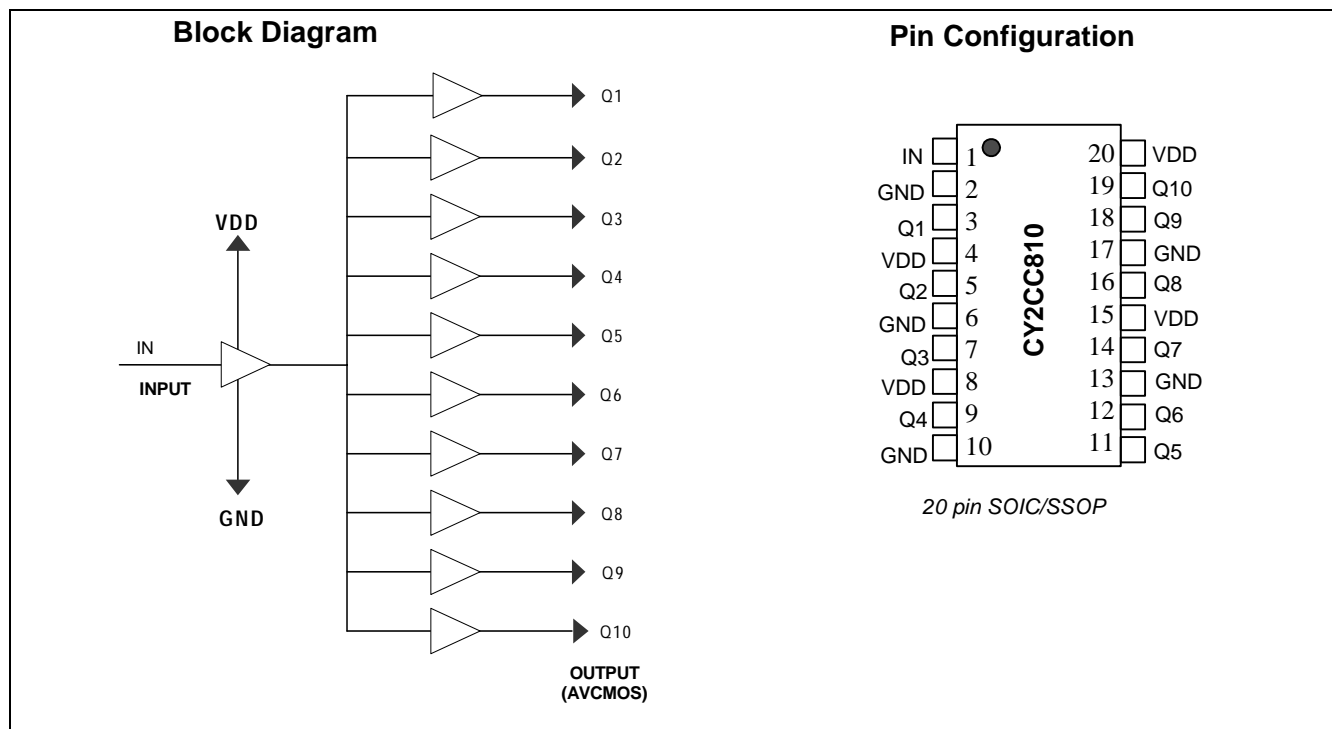
- Low-voltage operation
- $V_{DD}$  range from 2.5V to 3.3V
- 1:10 fanout
- Over voltage tolerant input hot swappable
- Drives either a 50-Ohm or 75-Ohm transmission line
- Low-input capacitance
- Low-output skew
- Low-propagation delay
- Typical ( $t_{pd} < 4$  ns)
- High-speed operation  $> 500$  MHz
- Industrial versions available
- Available packages include: SOIC, SSOP

## Description

The Cypress series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industries fastest logic and buffers.

The Cypress CY2CC810 fanout buffer features one input and ten outputs. Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

AVCMOS-type outputs dynamically adjust for variable impedance matching and eliminate the need for series damping resistors; they also reduce noise overall.



## Pin Description

Pin Number	Pin Name	Description	
1	IN	Input	LVC MOS
2, 6, 10, 13, 17	GND	Ground	Power
4, 8, 15, 20	$V_{DD}$	Power Supply	Power
3, 5, 7, 9, 11, 12, 14, 16, 18, 19	Q1... Q10	Output	AVCMOS



## Maximum Ratings<sup>[1][2]</sup>

Storage Temperature: ..... -65°C to + 150°C  
Ambient Temperature: ..... -40°C to +85°C  
Supply Voltage to Ground Potential  
 $V_{CC}$  ..... -0.5V to 4.6V  
Input ..... -0.5V to 5.8V

Supply Voltage to Ground Potential  
(Outputs only) ..... -0.5V to  $V_{DD} + 1V$   
DC Output Voltage ..... -0.5V to  $V_{DD} + 1V$   
Power Dissipation ..... 0.75W

## DC Electrical Characteristics @ 3.3V (see Figure 5)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
$V_{OH}$	Output High Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12 \text{ mA}$	2.3	3.3		V
$V_{OL}$	Output Low Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12 \text{ mA}$		0.2	0.5	V
$V_{IH}$	Input High Voltage	Guaranteed Logic High Level		2		5.8	V
$V_{IL}$	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
$I_{IH}$	Input High Current	$V_{DD} = \text{Max.}$	$V_{IN} = 2.7V$			1	uA
$I_{IL}$	Input Low Current	$V_{DD} = \text{Max.}$	$V_{IN} = 0.5V$			-1	uA
$I_I$	Input High Current	$V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max.})$				20	uA
$V_{IK}$	Clamp Diode Voltage	$V_{DD} = \text{Min.}, I_{IN} = -18 \text{ mA}$			-0.7	-1.2	V
$I_{OK}$	Continuous Clamp Current	$V_{DD} = \text{Max.}, V_{OUT} = \text{GND}$				-50	mA
$O_{OFF}$	Power-down Disable	$V_{DD} = \text{GND}, V_{OUT} = < 4.5V$				100	uA
$V_H$	Input Hysteresis	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$			80		mV

## DC Electrical Characteristics @ 2.5V (see Figure 1)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
$V_{OH}$	Output High Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -7 \text{ mA}$	1.8			V
			$I_{OH} = 12 \text{ mA}$	1.6			V
$V_{OL}$	Output Low Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12 \text{ mA}$			0.65	V
$V_{IH}$	Input High Voltage	Guaranteed Logic High Level		1.6		5.0	V
$V_{IL}$	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
$I_{IH}$	Input High Current	$V_{DD} = \text{Max.}$	$V_{IN} = 2.4V$			1	uA
$I_{IL}$	Input Low Current	$V_{DD} = \text{Max.}$	$V_{IN} = 0.5V$			-1	uA
$I_I$	Input High Current	$V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max.})$				20	uA
$V_{IK}$	Clamp Diode Voltage	$V_{DD} = \text{Min.}, I_{IN} = -18 \text{ mA}$			-0.7	-1.2	V
$I_{OK}$	Continuous Clamp Current	$V_{DD} = \text{Max.}, V_{OUT} = \text{GND}$				-50	mA
$O_{OFF}$	Power-down Disable	$V_{DD} = \text{GND}, V_{OUT} = < 4.5V$				100	uA
$V_H$	Input Hysteresis				80		mV

## Capacitance

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$C_{in}$	Input Capacitance	$V_{IN} = 0V$		2.5		pF
$C_{out}$	Output Capacitance	$V_{OUT} = 0V$		6.5		pF

### Notes:

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Power Supply Characteristics** (see Figure 5)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$\Delta I_{CC}$	Delta $I_{CC}$ Quiescent Power Supply Current	$(I_{DD} @ V_{DD} = \text{Max. and } V_{IN} = V_{DD}) - (I_{DD} @ V_{DD} = \text{Max. and } V_{IN} = V_{DD} - 0.6V)$			50	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current	$V_{DD} = \text{Max.}$ Input toggling 50% Duty Cycle, Outputs Open			0.63	mA/MHz
$I_C$	Total Power Supply Current	$V_{DD} = \text{Max.}$ Input toggling 50% Duty Cycle, Outputs Open $f_L = 40 \text{ MHz}$			25	mA

**High-frequency Parametrics**

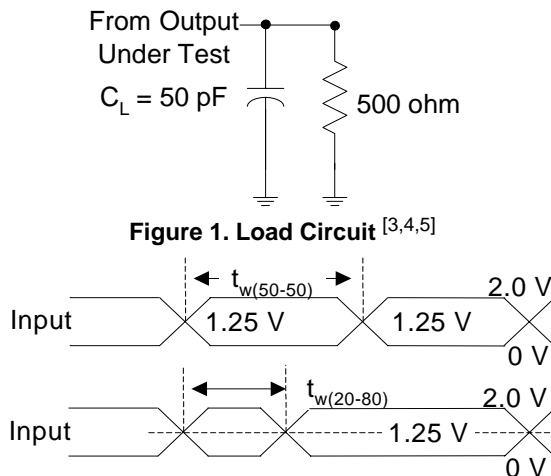
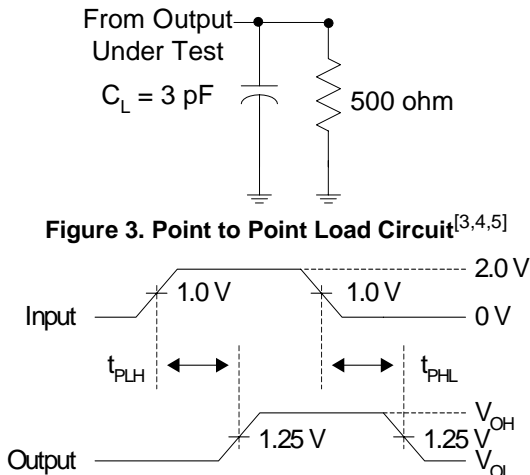
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$D_J$	Jitter, Deterministic	50% duty cycle tW(50–50) The “point to point load circuit” Output Jitter – Input Jitter	See Figure 5		20	ps
$F_{\max}$	Maximum frequency $V_{DD} = 3.3V$	50% duty cycle tW(50–50) Standard Load Circuit.			160	MHz
		50% duty cycle tW(50–50) The “point to point load circuit”	See Figure 7		650	
$F_{\max 2.5V}$	Maximum frequency $V_{DD} = 2.5 V$	The “point to point load circuit” $V_{IN} = 2.4V/0.0V$ $V_{OUT} = 1.7V/0.7V$	See Figure 7		200	MHz
$F_{\max(20)}$	Maximum frequency $V_{DD} = 3.3 V$	20% duty cycle tW(20–80) The “point to point load circuit” $V_{IN} = 3.0V/0.0V$ $V_{OUT} = 2.3V/0.4V$	See Figure 7		250	MHz
	Maximum frequency $V_{DD} = 2.5 V$	The “point to point load circuit” $V_{IN} = 2.4V/0.0V$ $V_{OUT} = 1.7V/0.7V$	See Figure 3		200	MHz
$t_W$	Minimum pulse $V_{DD} = 3.3 V$	The “point to point load circuit” $V_{IN} = 3.0V/0.0V$ $F = 100 \text{ MHz}$ $V_{OUT} = 2.0V/0.8V$	See Figure 7		1	ns
	Minimum pulse $V_{DD} = 2.5 V$	The “point to point load circuit” $V_{IN} = 2.4V/0.0V$ $F = 100 \text{ MHz}$ $V_{OUT} = 1.7V/0.7V$	See Figure 3		1	

**AC Switching Characteristics** @ 3.3V  $V_{DD} = 3.3V \pm 5\%$ , Temperature =  $-40^\circ C$  to  $+85^\circ C$ 

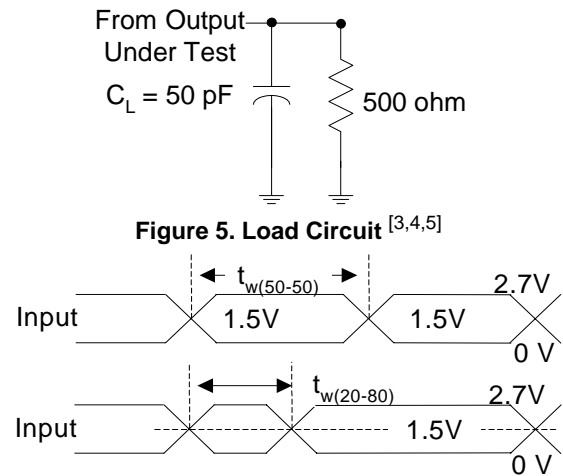
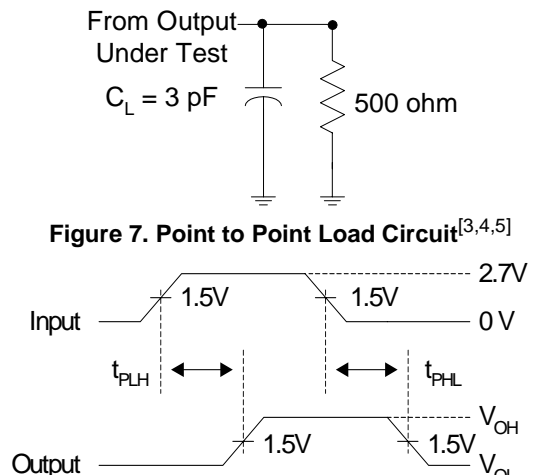
Parameter	Description		Min.	Typ.	Max.	Unit
$t_{PLH}$	Propagation Delay – Low to High	See Figure 4	1.5	2.7	3.5	nS
$t_{PHL}$	Propagation Delay – High to Low		1.5	2.7	3.5	nS
$t_R$	Output Rise Time			0.8		V/nS
$t_F$	Output Fall Time			0.8		V/nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 10			0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ( $t_{PHL} - t_{PLH}$ )	See Figure 9			0.2	nS
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 11			0.4	nS

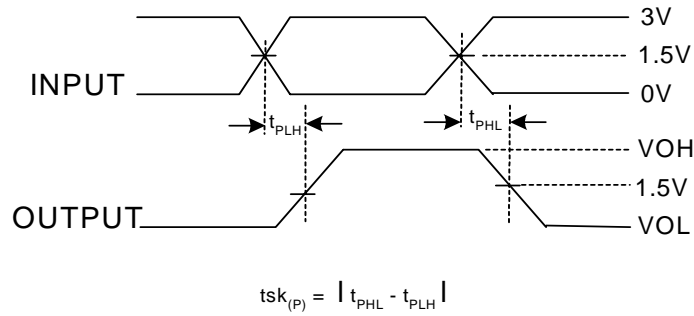
**AC Switching Characteristics @ 2.5V  $V_{DD} = 2.5V \pm 5\%$ , Temperature =  $-40^{\circ}C$  to  $+85^{\circ}C$** 

Parameter	Description		Min.	Typ.	Max.	Unit
t <sub>PLH</sub>	Propagation Delay – Low to High	See Figure 4	1.5	2.0	3.5	nS
t <sub>PHL</sub>	Propagation Delay – High to Low		1.5	2.0	3.5	nS
t <sub>R</sub>	Output Rise Time			0.8		V/nS
t <sub>F</sub>	Output Fall Time			0.8		V/nS
t <sub>SK(0)</sub>	Output Skew: Skew between outputs of the same package (in phase)	See Figure 10			0.2	nS
t <sub>SK(p)</sub>	Pulse Skew: Skew between opposite transitions of the same output (t <sub>PHL</sub> – t <sub>PLH</sub> ).	See Figure 9			0.2	nS
t <sub>SK(t)</sub>	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 11			0.65	nS

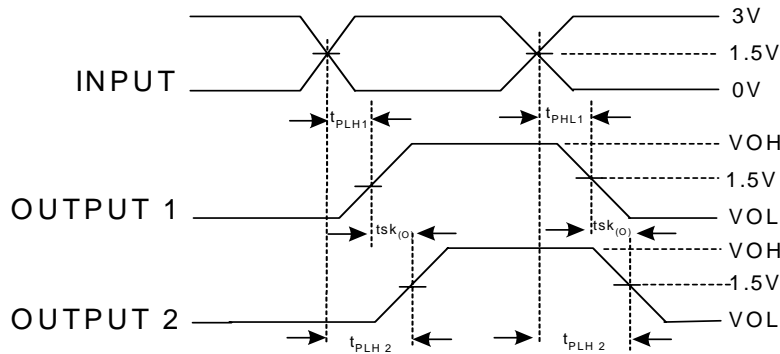
**Parameter Measurement Information:  
 $V_{DD}$  @ 2.5V**

**Figure 2. Voltage Waveforms–Pulse Duration<sup>[6]</sup>**

**Figure 4. Voltage Waveforms–Propagation Delay Times<sup>[4]</sup>**
**Notes:**

- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz,  $Z_0 = 50\Omega$ ,  $t_R < 2.5$  nS,  $t_F < 2.5$  nS.
- The outputs are measured one at a time with one transition per measurement.
- $T_{PLH}$  and  $T_{PHL}$  are the same as  $t_{pd}$ .

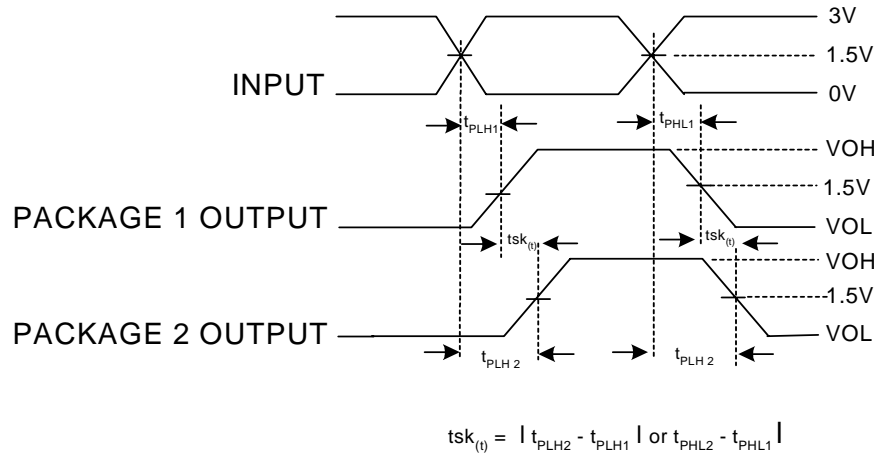
**Parameter Measurement Information:  
 $V_{DD}$  @ 3.3V**

**Figure 6. Voltage Waveforms–Pulse Duration<sup>[6]</sup>**

**Figure 8. Voltage Waveforms–Propagation Delay Times<sup>[4]</sup>**



**Figure 9. Pulse Skew- $tsk_{(p)}$**



**Figure 10. Output Skew- $tsk_{(o)}$**



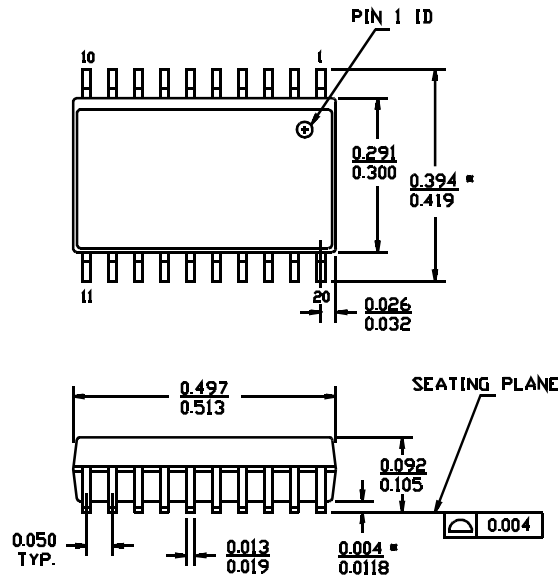
**Figure 11. Package Skew- $tsk_{(t)}$**

## Ordering Information

Part Number	Package Type	Product Flow
CY2CC810SI	20-pin SOIC	Industrial, -40°C to 85°C
CY2CC810SIT	20-pin SOIC-Tape and Reel	Industrial, -40°C to 85°C
CY2CC810OI	20-pin SSOP	Industrial, -40°C to 85°C
CY2CC810OIT	20-pin SSOP-Tape and Reel	Industrial, -40°C to 85°C
CY2CC810SC	20-pin SOIC	Commercial, 0°C to 70°C
CY2CC810SCT	20-pin SOIC-Tape and Reel	Commercial, 0°C to 70°C
CY2CC810OC	20-pin SSOP	Commercial, 0°C to 70°C
CY2CC810OCT	20-pin SSOP-Tape and Reel	Commercial, 0°C to 70°C

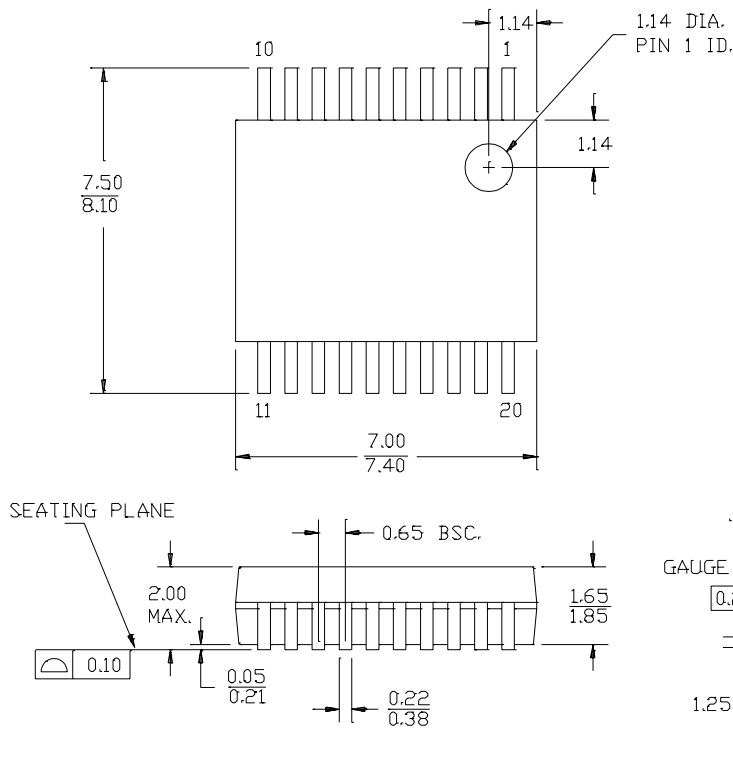
## Package Drawing and Dimensions

20-lead (300-mil) Molded SOIC S5



DIMENSIONS IN INCHES MIN.  
MAX.

20-lead (5.3-mm) Shrunk Small Outline Package O20



DIMENSIONS IN MILLIMETERS MIN.  
MAX.

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## Document History Page

Document Title: CY2CC810 1:10 Clock Fanout Buffer Document #: 38-07056				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107081	06/07/01	IKA	Convert from IMI to Cypress
*A	114315	05/09/02	TSM	$\Delta I_{DD}$ Validation
*B	119117	10/07/02	RGL	Added 5.8 as the Max. value of $V_{IH}$ in the DC Electrical Characteristics @3.3V table. Changed the Max. value of $V_{IH}$ from 1.8 to 5.0 in the DC Electrical Characteristics @2.5V table.
*C	122743	12/14/02	RBI	Added power up requirements to maximum ratings information.