

**CMLDM8002A
CMLDM8002AJ
SURFACE MOUNT PICOmini™
DUAL P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**

PICOmini™



SOT-563 CASE

**MARKING CODE: CMLDM8002A: C08
CMLDM8002AJ: CJ8**

**Central™
Semiconductor Corp.**

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM8002A and CMLDM8002AJ are dual chip Enhancement-mode P-Channel Field Effect Transistors, manufactured by the P-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM8002A utilizes the USA pinout configuration, while the CMLDM8002AJ, utilizing the Japanese pinout configuration, is available as a special order. These special Dual Transistor devices offer Low $R_{DS(on)}$ and Low $V_{DS(on)}$.

FEATURES:

- Dual Chip Device
- Low $R_{DS(on)}$
- Low $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small SOT-563 package

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
Drain-Gate Voltage
Gate-Source Voltage
Continuous Drain Current
Continuous Source Current (Body Diode)
Maximum Pulsed Drain Current
Maximum Pulsed Source Current
Power Dissipation
Power Dissipation
Power Dissipation
Operating and Storage
Junction Temperature
Thermal Resistance

SYMBOL

V_{DS}

50

UNITS

V

V_{DG}

50

V

V_{GS}

20

V

I_D

280

mA

I_S

280

mA

I_{DM}

1.5

A

I_{SM}

1.5

A

P_D

350

mW (Note 1)

P_D

300

mW (Note 2)

P_D

150

mW (Note 3)

T_J, T_{stg}

-65 to +150

$^\circ\text{C}$

θ_{JA}

357

$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$		100	nA
I_{GSSR}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$		100	nA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0\text{V}$		1.0	μA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$		500	μA
$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=10\text{V}$	500		mA
BV_{DSS}	$V_{GS}=0\text{V}, I_D=10\mu\text{A}$	50		V

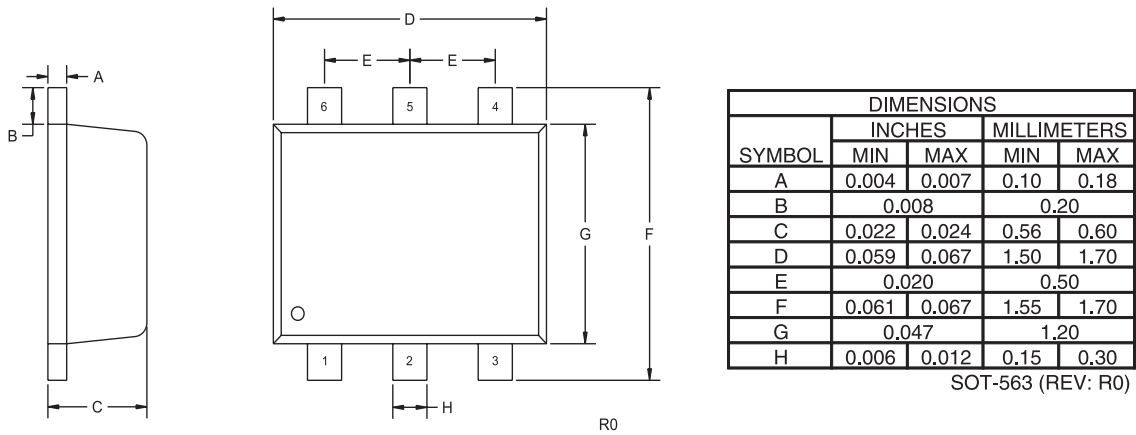
Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm²
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm²
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm²

R0 (24-January 2006)

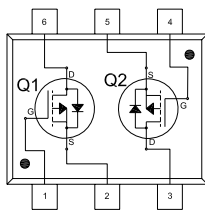
ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	2.5	V
$V_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$		1.5	V
$V_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$		0.15	V
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$		2.5	Ω
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$, $T_j=125^\circ\text{C}$		4.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$		3.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$, $T_j=125^\circ\text{C}$		5.0	Ω
Y_{fs}	$V_{DS}=10\text{V}$, $I_D=200\text{mA}$	200		msec
C_{rss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		7.0	pF
C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		70	pF
C_{oss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		15	pF
t_{on}	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=200\text{mA}$		20	ns
t_{off}	$R_G=25\Omega$, $R_L=150\Omega$		20	ns
V_{SD}	$V_{GS}=0\text{V}$, $I_S=115\text{mA}$		1.3	V

SOT-563 CASE - MECHANICAL OUTLINE



CMLDM8002A (USA Pinout)

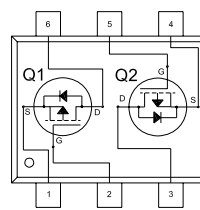


LEAD CODE:

- 1) GATE Q1
- 2) SOURCE Q1
- 3) DRAIN Q2
- 4) GATE Q2
- 5) SOURCE Q2
- 6) DRAIN Q1

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CMLDM8002AJ (Japanese Pinout)



LEAD CODE:

- 1) SOURCE Q1
- 2) GATE Q1
- 3) DRAIN Q2
- 4) SOURCE Q2
- 5) GATE Q2
- 6) DRAIN Q1

MARKING CODE: CJ8