



**■ PIN DESCRIPTIONS**

Name	Function
<b>A0-A16 Address Input</b>	These 17 address inputs select one of the 131,072 x 16-bit words in the RAM.
<b>SAE Address Input</b>	This address input incorporates with the above 17 address input select one of the 262,144 x 8-bit bytes in the RAM if the CIO is LOW. Don't use when CIO is HIGH.
<b>CIO x8/x16 select input</b>	This input selects the organization of the SRAM. 131,072 x 16-bit words configuration is selected if CIO is HIGH. 262,144 x 8-bit bytes configuration is selected if CIO is LOW.
<b><math>\overline{CE1}</math> Chip Enable 1 Input CE2 Chip Enable 2 Input</b>	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b><math>\overline{WE}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{OE}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
<b><math>\overline{LB}</math> and <math>\overline{UB}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins. The chip is deselected when both $\overline{LB}$ and $\overline{UB}$ pins are HIGH.
<b>D0 - D15 Data Input/Output Ports</b>	These 16 bi-directional ports are used to read data from or write data into the RAM.
<b>Vcc</b>	Power Supply
<b>Gnd</b>	Ground

**■ TRUTH TABLE**

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	CIO	$\overline{LB}$	$\overline{UB}$	SAE	D0~7	D8~15	VCC Current
Fully Standby	H	X	X	X	X	X	X	X	High-Z	High-Z	$I_{CCSB1}$ $I_{CCSB1}$
	X	L				X	X				
Output Disable	L	H	H	H	X	X	X	X	High-Z	High-Z	$I_{CC}$
Read from SRAM (WORD mode)	L	H	L	H	H	L	H	X	Dout	High-Z	$I_{CC}$
						H	L		High-Z	Dout	
						L	L		Dout	Dout	
Write to SRAM (WORD mode)	L	H	X	L	H	L	H	X	Din	X	$I_{CC}$
						H	L		X	Din	
						L	L		Din	Din	
Read from SRAM (BYTE Mode)	L	H	L	H	L	X	X	A-1	Dout	High-Z	$I_{CC}$
Write to SRAM (BYTE Mode)	L	H	X	L	L	X	X	A-1	Din	X	$I_{CC}$

**■ ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V TERM	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
T BIAS	Temperature Under Bias	-40 to +125	°C
T STG	Storage Temperature	-60 to +150	°C
P T	Power Dissipation	1.0	W
I OUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**■ OPERATING RANGE**

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to +70°C	2.4V ~ 3.6V
Industrial	-40°C to +85°C	2.4V ~ 3.6V

**■ CAPACITANCE<sup>(1)</sup> (TA = 25°C, f = 1.0 MHz)**

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	VI/O=0V	8	pF

1. This parameter is guaranteed and not 100% tested.

**■ DC ELECTRICAL CHARACTERISTICS (TA = 0°C to +70°C)**

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)</sup>	V <sub>CC</sub> =3.0V	-0.5	--	0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>	V <sub>CC</sub> =3.0V	2.0	--	V <sub>CC</sub> +0.2	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V to V <sub>CC</sub>	--	--	1	uA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max, $\overline{CE1} = V_{IH}$ or CE2=V <sub>IL</sub> or $\overline{OE} = V_{IH}$ , V <sub>I/O</sub> = 0V to V <sub>CC</sub>	--	--	1	uA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 2mA	V <sub>CC</sub> =3.0V	--	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>bH</sub> = -1mA	V <sub>CC</sub> =3.0V	2.4	--	V
I <sub>CC</sub>	Operating Power Supply Current	V <sub>CC</sub> = Max, $\overline{CE1} = V_{IL}$ , CE2=V <sub>IH</sub> , I <sub>DD</sub> = 0mA, F = Fmax <sup>(3)</sup>	V <sub>CC</sub> =3.0V	--	20	mA
I <sub>CCSB</sub>	Standby Current TL	V <sub>CC</sub> = Max, $\overline{CE1} = V_{IH}$ or CE2=V <sub>IL</sub> , I <sub>DD</sub> = 0mA	V <sub>CC</sub> =3.0V	--	1	mA
I <sub>CCSB1</sub>	Standby Current MOS	V <sub>CC</sub> = Max, $\overline{CE1} \geq V_{CC}-0.2V$ or CE2 $\leq 0.2V$ , Other inputs $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	V <sub>CC</sub> =3.0V	--	0.1	0.7 uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

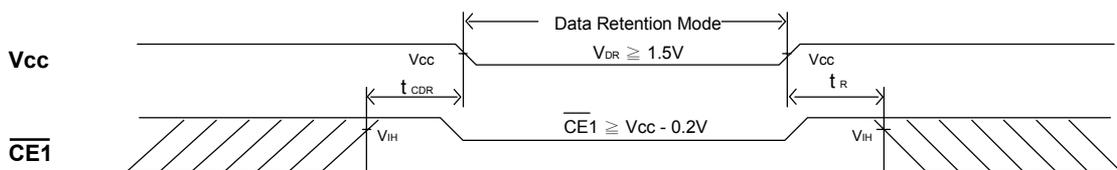
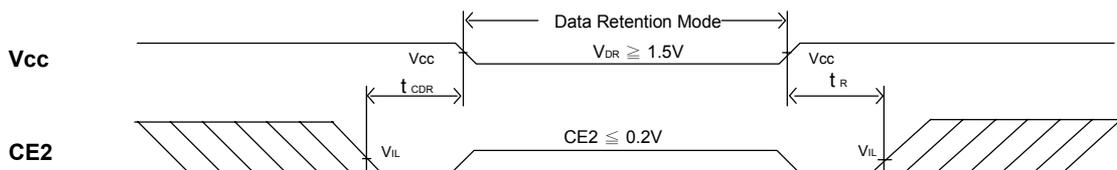
3. Fmax = 1/t<sub>RC</sub>.

**DATA RETENTION CHARACTERISTICS ( TA = 0 to + 70°C )**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	1.5	--	--	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	--	0.05	0.5	uA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t <sub>R</sub>	Operation Recovery Time		T <sub>RC</sub> <sup>(2)</sup>	--	--	ns

 1. V<sub>CC</sub> = 1.5V, T<sub>A</sub> = + 25°C

 2. t<sub>RC</sub> = Read Cycle Time

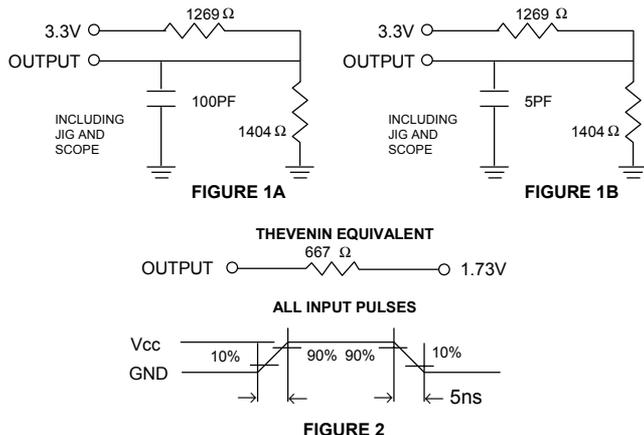
**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (1) (  $\overline{CE1}$  Controlled )**

**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (1) ( CE2 Controlled )**


**■ AC TEST CONDITIONS**

Input Pulse Levels	V <sub>cc</sub> /0V
Input Rise and Fall Times	1V/ns
Input and Output	
Timing Reference Level	0.5V <sub>cc</sub>

**■ KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

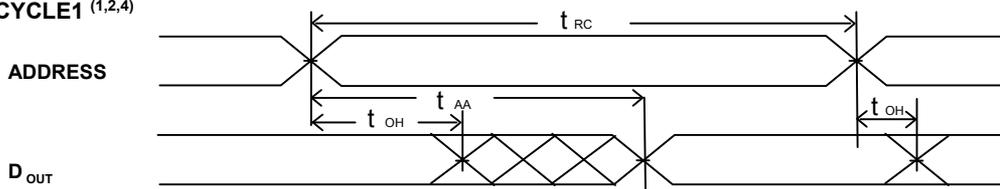
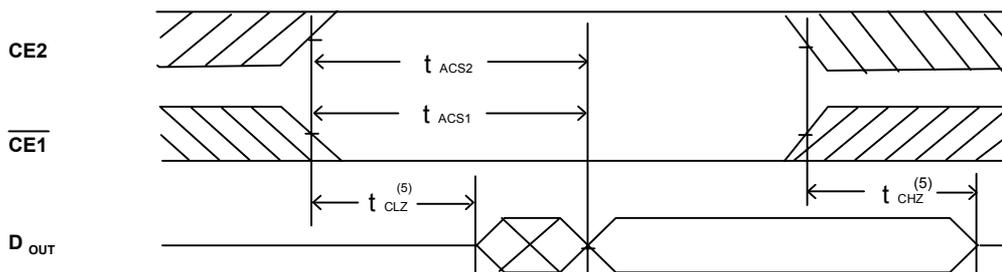
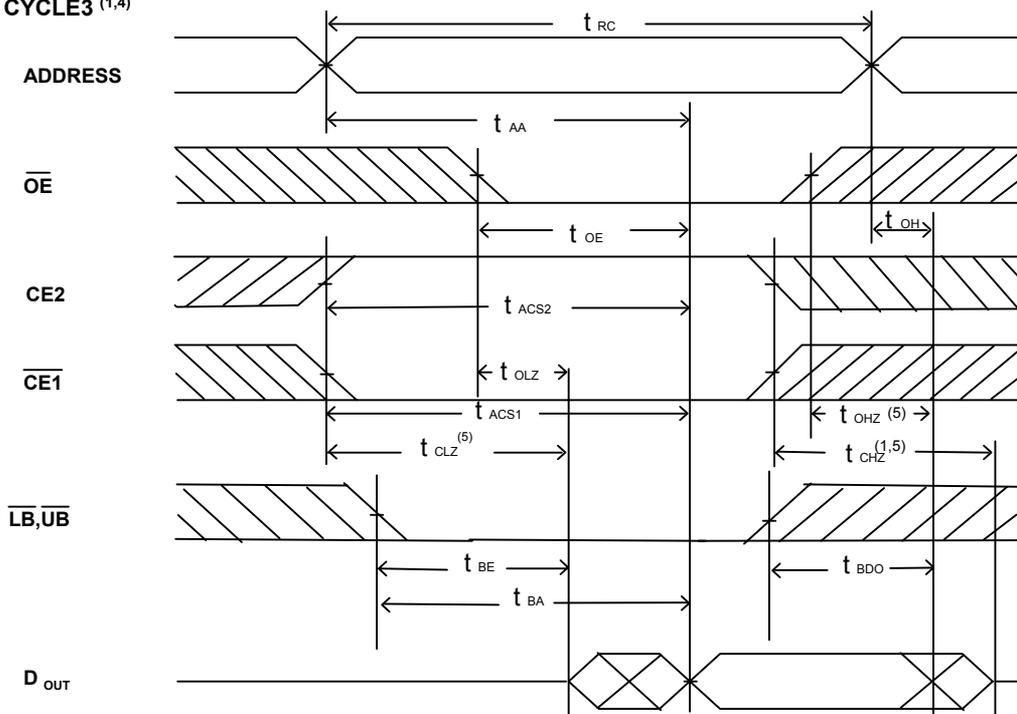
**■ AC TEST LOADS AND WAVEFORMS**

**■ AC ELECTRICAL CHARACTERISTICS ( TA = 0 to +70°C , V<sub>cc</sub> = 3.0V )**
**READ CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616LV2023-70			BS616LV2023-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>RC</sub>	Read Cycle Time	70	--	--	100	--	--	ns
t <sub>AVQV</sub>	t <sub>AA</sub>	Address Access Time	--	--	70	--	--	100	ns
t <sub>E1LQV</sub>	t <sub>ACS1</sub>	Chip Select Access Time (CE1)	--	--	70	--	--	100	ns
t <sub>E2LQV</sub>	t <sub>ACS2</sub>	Chip Select Access Time (CE2)	--	--	70	--	--	100	ns
t <sub>BA</sub>	t <sub>BA</sub> <sup>(1)</sup>	Data Byte Control Access Time (LB, UB)	--	--	35	--	--	50	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Valid	--	--	35	--	--	50	ns
t <sub>ELQX</sub>	t <sub>CLZ</sub>	Chip Select to Output Low Z (CE1, CE2)	10	--	--	15	--	--	ns
t <sub>BE</sub>	t <sub>BE</sub>	Data Byte Control to Output Low Z (LB, UB)	10	--	--	15	--	--	ns
t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output in Low Z	10	--	--	15	--	--	ns
t <sub>EHQZ</sub>	t <sub>CHZ</sub>	Chip Deselect to Output in High Z (CE1, CE2)	0	--	35	0	--	40	ns
t <sub>BDO</sub>	t <sub>BDO</sub>	Data Byte Control to Output High Z (LB, UB)	0	--	35	0	--	40	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	0	--	30	0	--	35	ns
t <sub>AXOX</sub>	t <sub>OH</sub>	Output Disable to Address Change	10	--	--	15	--	--	ns

NOTE :

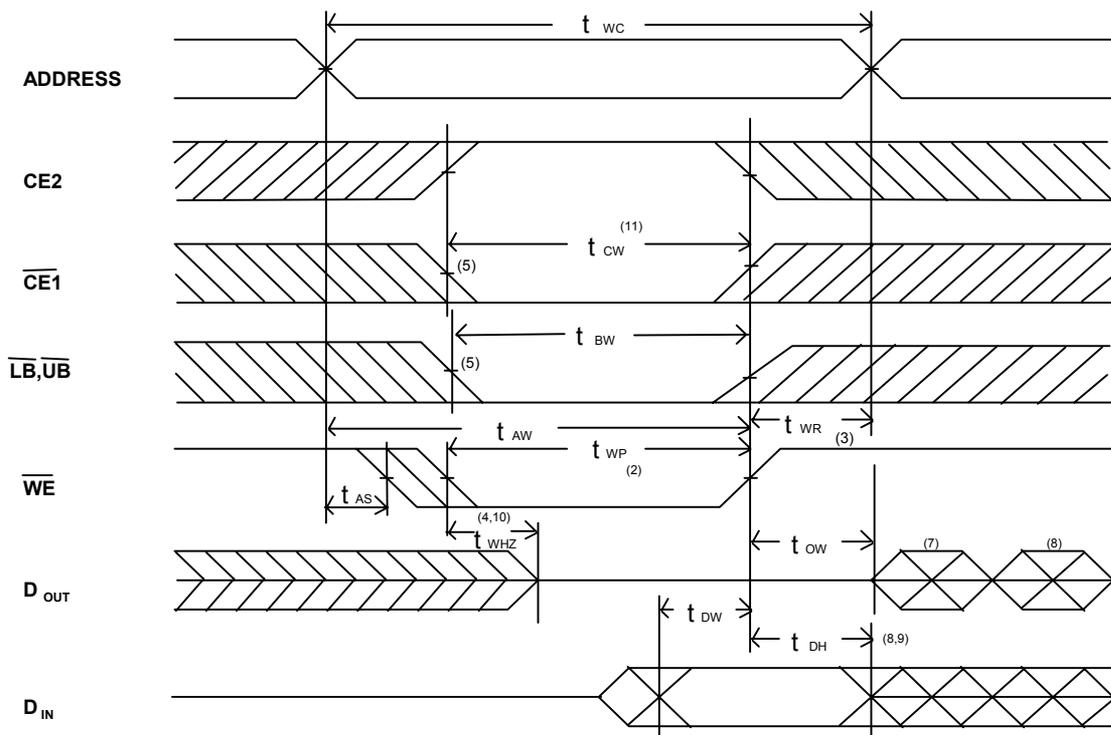
1. t<sub>BA</sub> is 35ns/50ns (@speed=70ns/100ns) with address toggle .

t<sub>BA</sub> is 70ns/100ns (@speed=70ns/100ns) without address toggle .

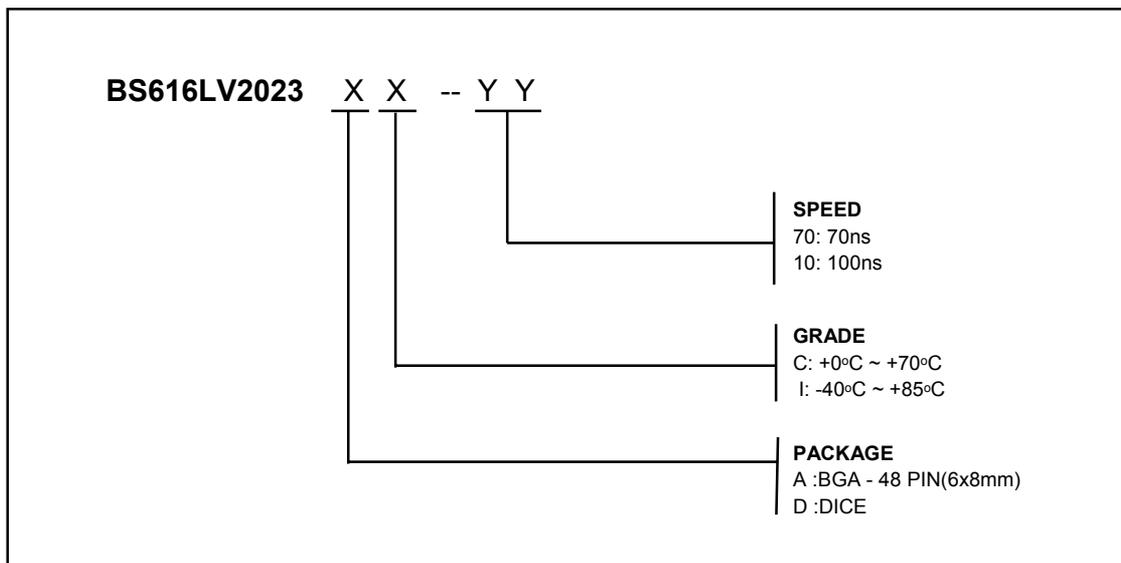
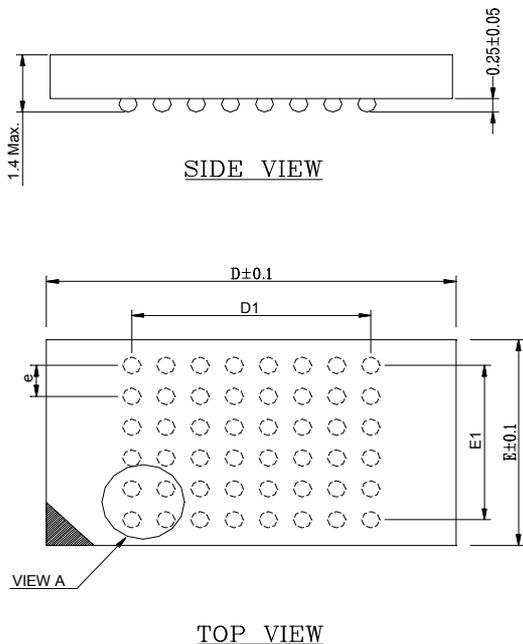
**SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE1 (1,2,4)**

**READ CYCLE2 (1,3,4)**

**READ CYCLE3 (1,4)**

**NOTES:**

1.  $\overline{WE}$  is high in read Cycle.
2. Device is continuously selected when  $\overline{CE1} = V_{IL}$  and  $CE2 = V_{IH}$ .
3. Address valid prior to or coincident with  $\overline{CE1}$  transition low and  $CE2$  transition high.
4.  $OE = V_{IL}$ .
5. Transition is measured  $\pm 500mV$  from steady state with  $CL = 30pF$  as shown in Figure 1B.  
The parameter is guaranteed but not 100% tested.



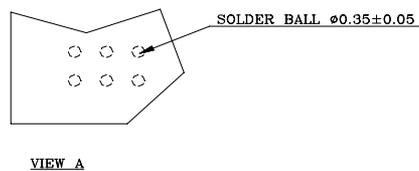
**WRITE CYCLE2 (1,6)**

**NOTES:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2,  $\overline{CE1}$  and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of CE2 going low, or  $\overline{CE1}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or  $\overline{CE1}$  low transition or  $\overline{LB}, \overline{UB}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7. DOUT is the same phase of write data of this write cycle.
8. DOUT is the read data of next address.
9. If CE2 is high or  $\overline{CE1}$  is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 30\text{pF}$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of CE2 going high or  $\overline{CE1}$  going low to the end of write.

**■ ORDERING INFORMATION**

**■ PACKAGE DIMENSIONS**

**NOTES:**

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



*48 mini-BGA (6 x 8mm)*