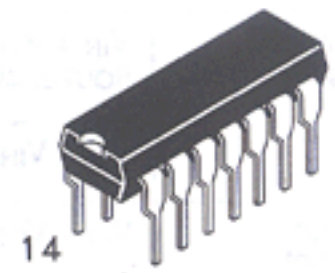
Quad 2-Input NAND Gate with Open-Drain Outputs

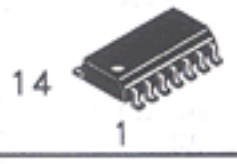
DV74HC03A

This device contains four independent 2-input NAND buffers, each of which performs the logic NAND function in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-high wired-AND functions.

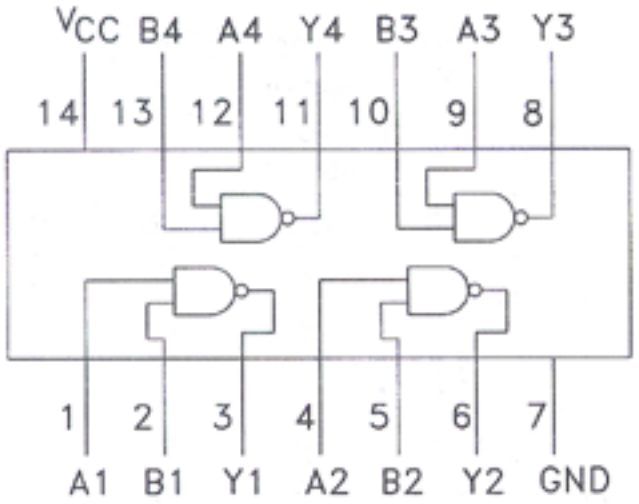
- **Output Drive Capability: 10 LSTTL Loads**
- **Outputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range: 2 to 6 V for HC devices**
- **Low Input Current: 1 μA**
- **DC, AC parameters guaranteed from -55°C to 125°C**



N Suffix
Plastic DIP
AVG-001 Case



D Suffix
Plastic SOP
AVG-002 Case



TRUTH TABLE
$Y = \overline{AB}$

Inputs		Outputs
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = High Logic Level
L = Low Logic Level
Z = High Impedence

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	–1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP SOP Package	750 500	mW
T_{STG}	Storage Temperature Range	–65 to +150	°C
TL	Lead Temperature, 1mm from Case for 10 Seconds (Plastic DIP or Sop Package)	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage Referenced to GND	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Ambient Temperature	–55	+125	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Vcc V	Guaranteed Limits			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT} =0.1 V or = V_{CC}−0.1V $\|I_{OUT}\| \leq$ 20 µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low- Level Input Voltage	V_{OUT} =0.1 V or = V_{CC}−0.1V $\|I_{OUT}\| \leq$ 20 µA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq$ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq$ 4.0mA $\|I_{OUT}\| \leq$ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{IN} = V_{CC} or GND $\|I_{OUT}\|$= 0 µA	6.0	1	10	40	µA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedence State V_{IN}=V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	6.0	±0.5	±5.0	±10.0	µA

AC ELECTRICAL CHARACTERISTICS over full operating conditions (C_L=50pF, Input t_f=t_r=6ns, R_L=1kΩ)

Symbol	Parameter	Vcc V	Guaranteed Limits			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLZ}, t_{PZL}	Maximum Propagation Delay Time, Input A or B To Output Y	2.0 4.5 6.0	125 24 20	150 30 26	180 36 31	ns
t_{THL}	Maximum Output Transition Time Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in HIgh-Impedence State)	—	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V_{CC} = 5 V	pF
		8	

SWITCHING WAVEFORMS (Input Threshold Voltage, V_T=50% V_{CC}, V_H=V_{CC})