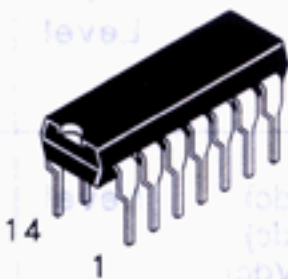


Dual D-Type Flip-Flop

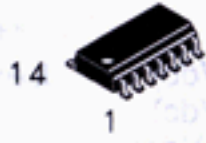
This device is a dual D-Type Flip-flop constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, Set, Reset, and Clock inputs and complementary outputs.

- Supply voltage range = 3.0 Vdc to 18 Vdc
- All outputs buffered
- Capable of driving 4 Low Power TTL loads or one LS TTL load over the rated temperature range
- Diode protection on all inputs
- Highest noise immunity at 12V supply

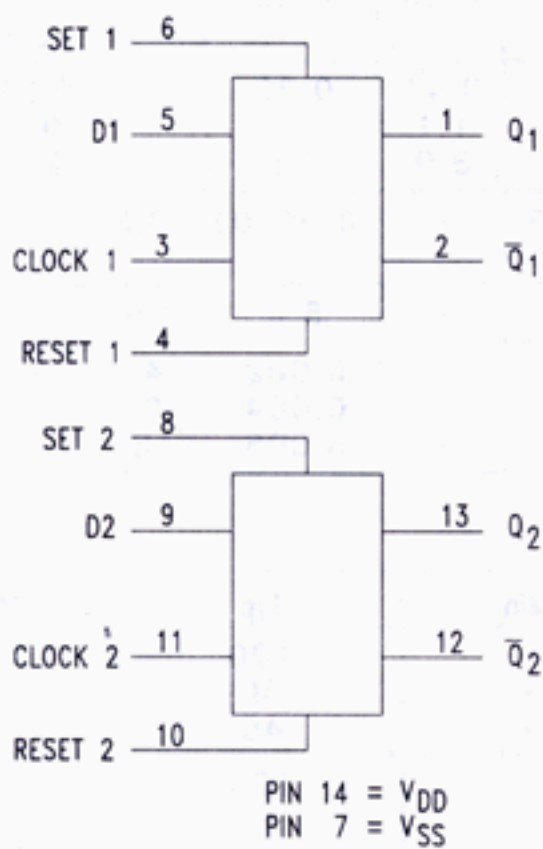
DV4013B



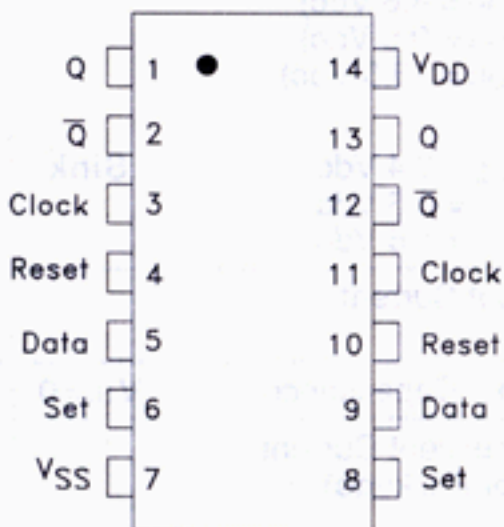
N Suffix
Plastic DIP
AVG-001 Case



D Suffix
Plastic SOP
AVG-002 Case



PIN ASSIGNMENT



TRUTH TABLE

Clock	D	Reset	Set	Q	Q̄
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	No Change	
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

↑ = Low to High Transition
↓ = High to Low Transition
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage (Referenced to V _{SS})	-0.5 to +18.0	V
V _{IN} , V _{OUT}	Input or Output Voltage	-0.5 to V _{DD} +0.5	V
I _{IN} , I _{OUT}	DC Current Into or Out of Any Pin	± 10	mA
P _D	Power Dissipation in Still Air, Derating: 12 mW/°C from 65° to 85°C	500	mW
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, (8 Second Soldering)	260	°C

4013B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter		V _{DD}	Guaranteed Limits							Unit
				-40°C		25°C			85°C		
				Min	Max	Min	Typ	Max	Min	Max	
V _{OL}	Output Voltage V _{IN} =V _{DD} or 0	"0" Level	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	V _{dc}
V _{OH}	V _{IN} = 0 or V _{DD}	"1" Level	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	V _{dc}
V _{IL}	Input Voltage (V _O =4.5 or 0.5 V _{dc}) (V _O =9.0 or 1.0 V _{dc}) (V _O =13.5 or 1.5 V _{dc})	"0" Level	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	V _{dc}
V _{IH}	(V _O =0.5 or 4.5 V _{dc}) (V _O =1.0 or 9.0 V _{dc}) (V _O =1.5 or 13.5 V _{dc})	"1" Level	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	V _{dc}
I _{OH}	Output Drive Current (V _{OH} = 2.5 V _{dc}) (V _{OH} = 4.6 V _{dc}) (V _{OH} = 9.5 V _{dc}) (V _{OH} = 13.5 V _{dc})	Source	5.0 5.0 10 15	-2.5 -0.52 -1.3 -3.6	- - - -	-2.1 -0.44 -1.1 -3.0	-4.2 -0.88 -2.25 -8.8	- - - -	-1.7 - 0.36 -0.9 -2.4	- - - -	mAdc
I _{OL}	(V _{OL} = 0.4 V _{dc}) (V _{OL} = 0.5 V _{dc}) (V _{OL} = 1.5 V _{dc})	Sink	5.0 10 15	0.52 1.3 3.6	- - -	0.44 1.1 3.0	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
I _{IN}	Input Current		15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdc
C _{IN}	Input Capacitance	V _{IN} =0	-	-	-	-	5.0	7.5	-	-	pF
I _{DD}	Quiescent Current (Per Package)		5.0 10 15	- - -	4 8 16	- - -	0.002 0.004 0.006	4 8 16	- - -	30 60 120	μAdc

SWITCHING CHARACTERISTICS (C_L=50 pF, T_A=25°C)

Symbol	Characteristics	V _{DD}	Min	Typ	Max	Unit
t _{TLH} , t _{THL}	Output Rise and Fall Time	5.0	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
t _{PLH} , t _{PHL}	Propagation Delay Time, Clock and Set to Q, \bar{Q}	5.0	-	175	350	ns
		10	-	75	150	
		15	-	50	100	
	Reset to Q, \bar{Q}	5.0	-	350	450	
		10	-	100	200	
		15	-	75	150	
t _{WL} , t _{WH}	Clock, Set and Reset Pulse Width	5.0	250	125	-	ns
		10	100	50	-	
		15	70	35	-	
f _{cl}	Clock Pulse Frequency	5.0	-	4.0	2.0	MHz
		10	-	10	5.0	
		15	-	14	7.0	
t _{TLH} , t _{THL}	Clock Pulse Rise and Fall Time	5.0	-	-	15	μs
		10	-	-	5	
		15	-	-	4	
t _{su}	Setup Time (Data must be valid for 250 ns with a 5V supply, 100 ns with 10V, and 70 ns with 15V)	5.0	40	20	-	ns
		10	20	10	-	
		15	15	7.5	-	

SWITCHING CHARACTERISTICS (Continued)

Symbol	Characteristics	V _{DD}	Min	Typ	Max	Unit
t _h	Hold Time (Data must be valid for 250 ns with a 5V supply, 100 ns with 10V, and 70 ns with 15V)	5.0	40	20	-	ns
		10	20	10	-	
		15	15	7.5	-	
t _{rem}	Removal Times Set	5.0	80	0	-	ns
		10	45	5	-	
		15	35	5	-	
	Reset	5.0	50	-35	-	
		10	30	-10	-	
		15	25	-5	-	

SWITCHING WAVEFORMS

