

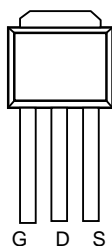
**AOU412**
**N-Channel Enhancement Mode Field Effect Transistor**
**General Description**

The AOU412 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and low gate resistance. This device is ideally suited for use as a high side switch in CPU core power conversion. *Standard Product AOU412 is Pb-free (meets ROHS & Sony 259 specifications). AOU412L is a Green Product ordering option. AOU412 and AOU412L are electrically identical.*

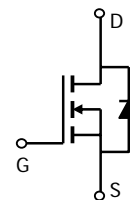
**Features**

$V_{DS} (V) = 30V$   
 $I_D = 85A (V_{GS} = 10V)$   
 $R_{DS(ON)} < 7.5m\Omega (V_{GS} = 10V)$   
 $R_{DS(ON)} < 11m\Omega (V_{GS} = 4.5V)$

TO-251



Top View  
 Drain  
 Connected to  
 Tab


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,G</sup>	$T_C=25^\circ C^G$	$I_D$	85	A
	$T_C=100^\circ C^B$		65	
Pulsed Drain Current		$I_{DM}$	200	
Avalanche Current <sup>C</sup>		$I_{AR}$	30	A
Repetitive avalanche energy $L=0.1mH^C$		$E_{AR}$	120	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	$P_D$	100	W
	$T_C=100^\circ C$		50	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 175	$^\circ C$

**Thermal Characteristics**

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	Steady-State	$R_{\theta JA}$	105	125	$^\circ C/W$
Maximum Junction-to-Lead <sup>C</sup>	Steady-State	$R_{\theta JL}$	1	1.5	$^\circ C/W$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		0.005	1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.5	2.15	2.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	85			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		5.7 8.4	7.5 10	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		8.7	11	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		60		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.72	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				85	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		1320	1600	pF
C <sub>oss</sub>	Output Capacitance			533		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			154		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		0.95	1.2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		26	32	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			13.3	16.2	nC
Q <sub>gs</sub>	Gate Source Charge			3.2		nC
Q <sub>gd</sub>	Gate Drain Charge			6.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		7.2	10	ns
t <sub>r</sub>	Turn-On Rise Time			12.5	18	ns
t <sub>D(off)</sub>	Turn-Off DelayTime			22	33	ns
t <sub>f</sub>	Turn-Off Fall Time			6	9	ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=100A/μs		29.7	36	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=100A/μs		29	36	nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: The maximum current rating is limited by bond-wires.

Rev3: August 2005

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

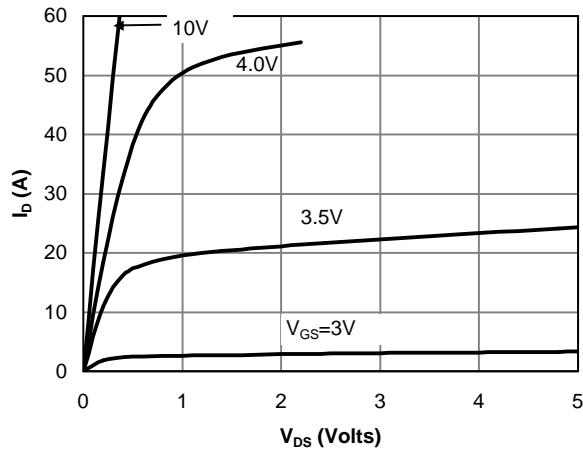


Fig 1: On-Region Characteristics

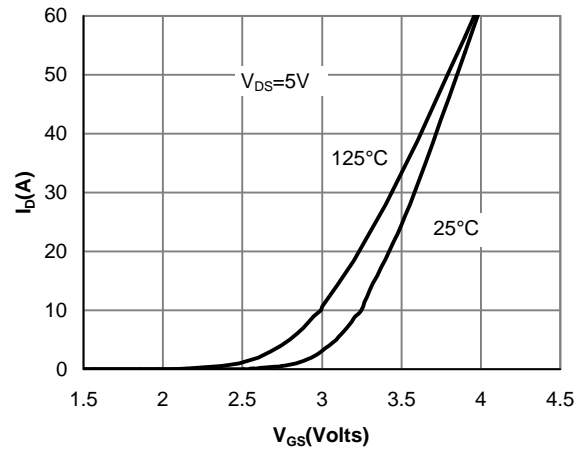


Figure 2: Transfer Characteristics

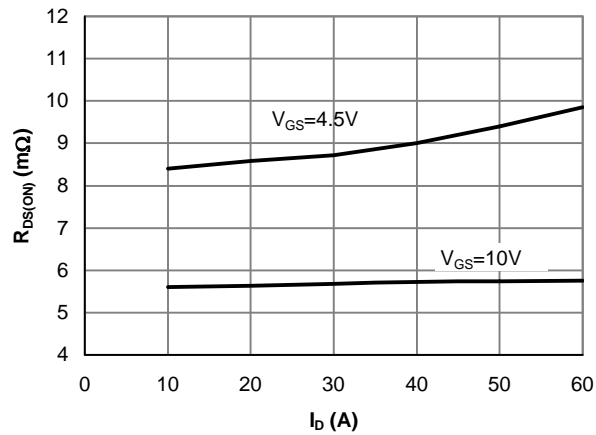


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

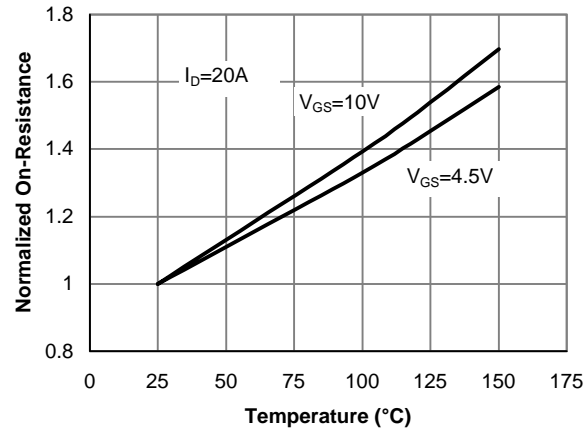


Figure 4: On-Resistance vs. Junction Temperature

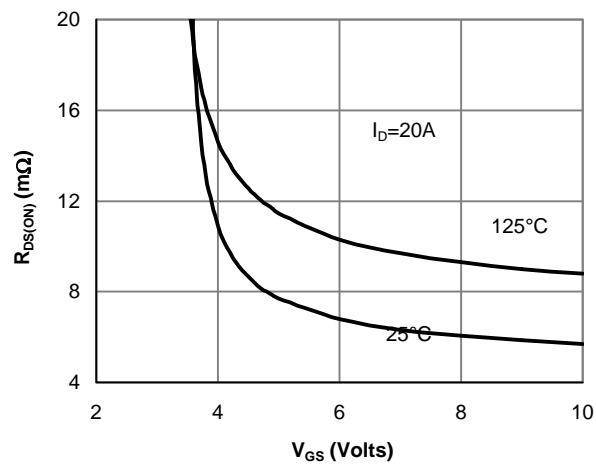


Figure 5: On-Resistance vs. Gate-Source Voltage

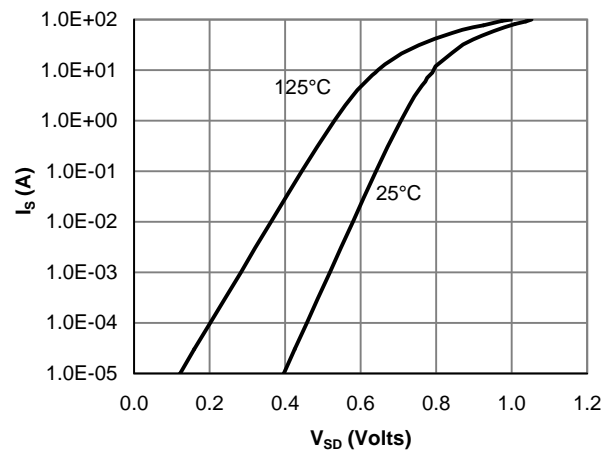


Figure 6: Body-Diode Characteristics

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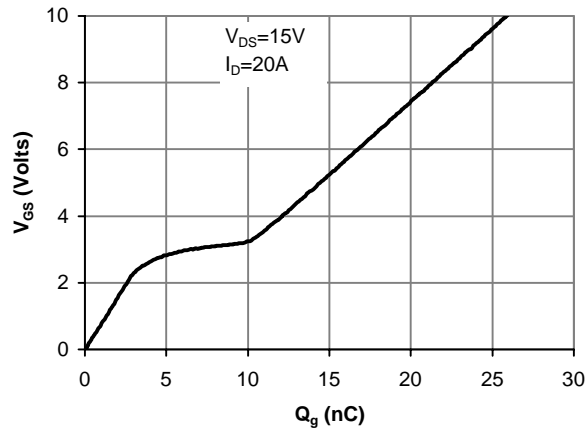


Figure 7: Gate-Charge Characteristics

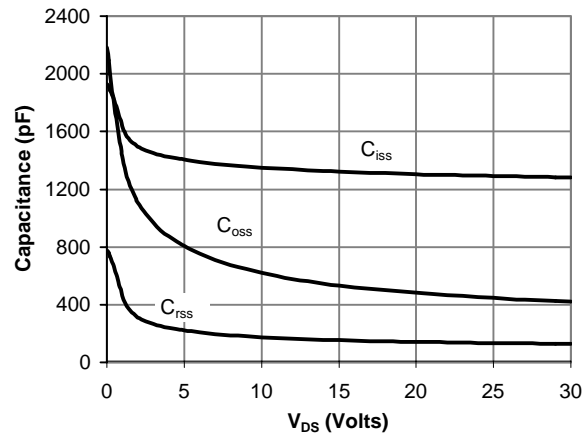


Figure 8: Capacitance Characteristics

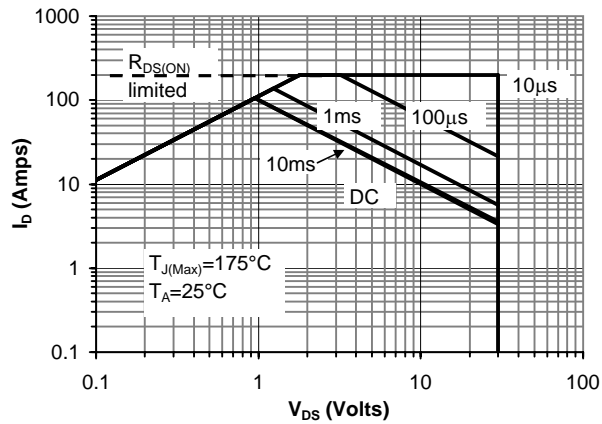


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

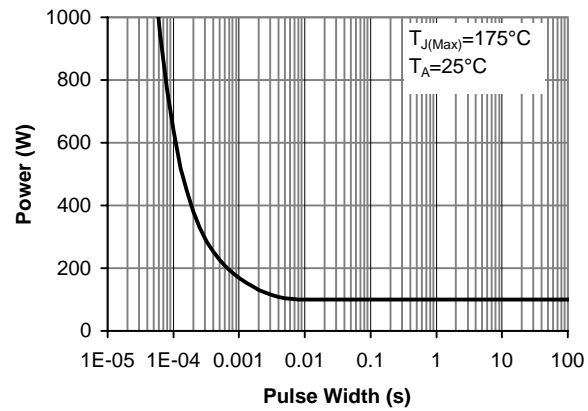


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

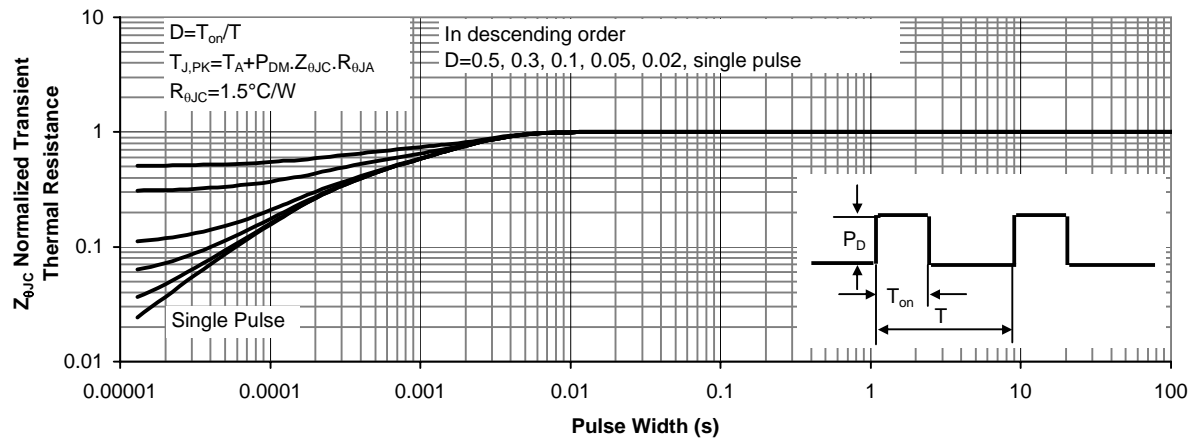


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

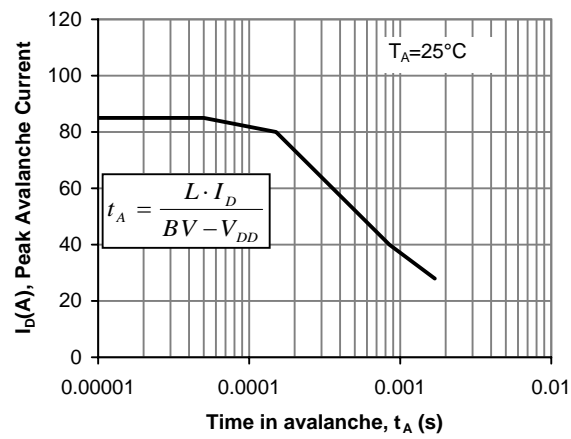


Figure 12: Single Pulse Avalanche capability

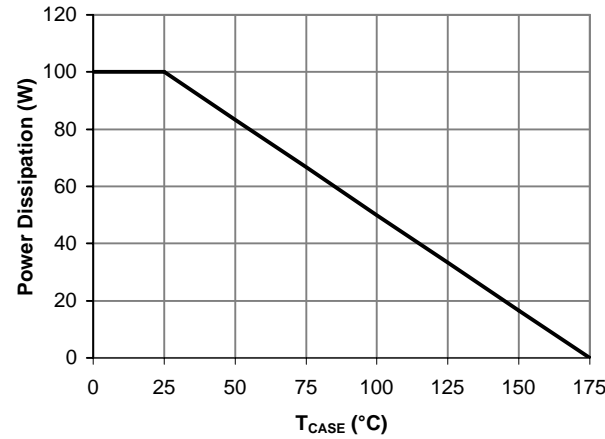


Figure 13: Power De-rating (Note B)

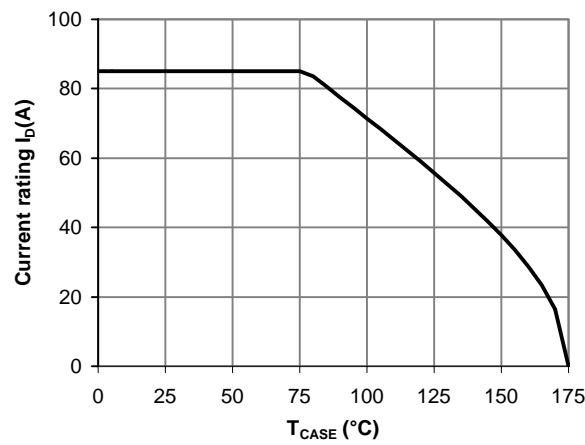


Figure 14: Current De-rating (Note B)