

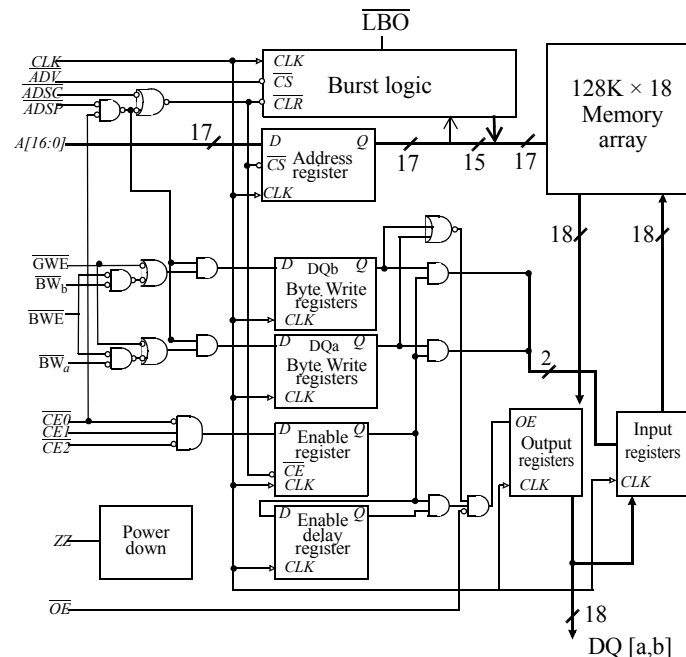


### 3.3V 128K $\times$ 18 pipeline burst synchronous SRAM

## Features

- Organization: 131,072 words  $\times$  18 bits
- Fast clock speeds to 200 MHz
- Fast clock to data access: 3.0/3.5/4.0 ns
- Fast  $\overline{\text{OE}}$  access time: 3.0/3.5/4.0 ns
- Fully synchronous register-to-register operation
- Double-cycle deselect
- Asynchronous output enable control
- Available in 100-pin TQFP package
- Individual byte write and global write
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate  $V_{\text{DDQ}}$
- Linear or interleaved burst control
- Snooze mode for reduced power-standby
- Common data inputs and data outputs

## Logic block diagram



## Selection guide

	<b>–200</b>	<b>–166</b>	<b>–133</b>	<b>Units</b>
Minimum cycle time	5	6	7.5	ns
Maximum clock frequency	200	166	133	MHz
Maximum clock access time	3.0	3.5	4	ns
Maximum operating current	375	350	325	mA
Maximum standby current	130	100	90	mA
Maximum CMOS standby current (DC)	30	30	30	mA



## 2 Mb Synchronous SRAM products list<sup>1,2</sup>

Org	Part Number	Mode	Speed
128KX18	AS7C33128PFS18B	PL-SCD	200/166/133 MHz
64KX32	AS7C3364PFS32B	PL-SCD	200/166/133 MHz
64KX36	AS7C3364PFS36B	PL-SCD	200/166/133 MHz
128KX18	AS7C33128PFD18B	PL-DCD	200/166/133 MHz
64KX32	AS7C3364PFD32B	PL-DCD	200/166/133 MHz
64KX36	AS7C3364PFD36B	PL-DCD	200/166/133 MHz
128KX18	AS7C33128FT18B	FT	6.5/7.5/8.0/10 ns
64KX32	AS7C3364FT32B	FT	6.5/7.5/8.0/10 ns
64KX36	AS7C3364FT36B	FT	6.5/7.5/8.0/10 ns

1 Core Power Supply: VDD = 3.3V  $\pm$  0.165V

2 I/O Supply Voltage: VDDQ = 3.3V  $\pm$  0.165V for 3.3V I/O  
VDDQ = 2.5V  $\pm$  0.125V for 2.5V I/O

PL-SCD : Pipelined Burst Synchronous SRAM - Single Cycle Deselect  
 PL-DCD : Pipelined Burst Synchronous SRAM - Double Cycle Deselect  
 FT : Flow-through Burst Synchronous SRAM

**TQFP 14 × 20mm**

Pin	Function	Pin	Function
100	A	80	A
99	A	79	NC
98	CE0	78	NC
97	CE1	77	V <sub>DDQ</sub>
96	NC	76	V <sub>SSQ</sub>
95	NC	75	NC
94	BW <sub>b</sub>	74	DQ <sub>pa</sub>
93	BW <sub>a</sub>	73	DQ <sub>a7</sub>
92	CE2	72	DQ <sub>a6</sub>
91	V <sub>DD</sub>	71	V <sub>SSQ</sub>
90	V <sub>SS</sub>	70	V <sub>DDQ</sub>
89	CLK	69	DQ <sub>a5</sub>
88	GWE	68	DQ <sub>a4</sub>
87	BWE	67	V <sub>SS</sub>
86	OE	66	NC
85	ADSC	65	V <sub>DD</sub>
84	ADSP	64	ZZ
83	ADV	63	DQ <sub>a3</sub>
82	A	62	DQ <sub>a2</sub>
81	A	61	V <sub>DDQ</sub>
31	LBO	60	V <sub>SSQ</sub>
32	A	59	DQ <sub>a1</sub>
33	A	58	DQ <sub>a0</sub>
34	A	57	NC
35	A	56	NC
36	A1	55	V <sub>SSQ</sub>
37	A0	54	V <sub>DDQ</sub>
38	NC	53	NC
39	NC	52	NC
40	V <sub>SS</sub>	51	NC
41	V <sub>DD</sub>		
42	NC		
43	NC		
44	A		
45	A		
46	A		
47	A		
48	A		
49	A		
50	NC		
1	NC		
2	NC		
3	NC		
4	V <sub>DDQ</sub>		
5	V <sub>SSQ</sub>		
6	NC		
7	NC		
8	DQ <sub>b0</sub>		
9	DQ <sub>b1</sub>		
10	V <sub>SSQ</sub>		
11	V <sub>DDQ</sub>		
12	DQ <sub>b2</sub>		
13	DQ <sub>b3</sub>		
14	NC		
15	V <sub>DD</sub>		
16	NC		
17	V <sub>SS</sub>		
18	DQ <sub>b4</sub>		
19	DQ <sub>b5</sub>		
20	V <sub>DDQ</sub>		
21	V <sub>SSQ</sub>		
22	DQ <sub>b6</sub>		
23	DQ <sub>b7</sub>		
24	DQ <sub>pb</sub>		
25	NC		
26	V <sub>SSQ</sub>		
27	V <sub>DDQ</sub>		
28	NC		
29	NC		
30	NC		



## Functional description

The AS7C33128PFD18B is a high performance CMOS 2 Mbit synchronous Static Random Access Memory (SRAM) devices organized as 131,072 words  $\times$  18 bits and incorporate a pipeline for highest frequency on any given technology.

Timing for this device is compatible with existing Pentium® synchronous cache specifications. This architecture is suited for ASIC, DSP, and PowerPC™-based systems in computing, datacom, instrumentation, and telecommunications systems.

Fast cycle times of 5.0/6.0/7.5 ns with clock access times ( $t_{CD}$ ) of 3.0/3.5/4.0 ns enable 200, 166 and 133 MHz bus frequencies. Three chip enable inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ( $\overline{ADSC}$ ), or the processor address strobe ( $\overline{ADSP}$ ). The burst advance pin ( $\overline{ADV}$ ) allows subsequent internally generated burst addresses.

Read cycles are initiated with  $\overline{ADSP}$  (regardless of  $\overline{WE}$  and  $\overline{ADSC}$ ) using the new external address clocked into the on-chip address register. When  $\overline{ADSP}$  is sampled LOW, the chip enables are sampled active, and the output buffer is enabled with  $\overline{OE}$ . In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers and driven on the output pins on the next positive edge of CLK.  $\overline{ADV}$  is ignored on the clock edge that samples  $\overline{ADSP}$  asserted but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when  $\overline{ADV}$  is sampled LOW and both address strobes are HIGH. Burst mode is selectable with the  $\overline{LBO}$  input. With  $\overline{LBO}$  unconnected or driven HIGH, burst operations use a Pentium® count sequence. With  $\overline{LBO}$  driven LOW the device uses a linear count sequence suitable for PowerPC™ and many other applications.

Write cycles are performed by disabling the output buffers with  $\overline{OE}$  and asserting a write command. A global write enable  $\overline{GWE}$  writes all 18 bits regardless of the state of individual  $BW[a:b]$  inputs. Alternately, when  $\overline{GWE}$  is HIGH, one or more bytes may be written by asserting  $\overline{BWE}$  and the appropriate individual byte  $BWn$  signal(s).

$\overline{BWn}$  is ignored on the clock edge that samples  $\overline{ADSP}$  LOW, but is sampled on all subsequent clock edges. Output buffers are disabled when  $\overline{BWn}$  is sampled LOW (regardless of  $\overline{OE}$ ). Data is clocked into the data input register when  $\overline{BWn}$  is sampled LOW. Address is incremented internally to the next burst address if  $\overline{BWn}$  and  $\overline{ADV}$  are sampled LOW. This device operates in double-cycle deselect feature during read cycles.

Read or write cycles may also be initiated with  $\overline{ADSC}$  instead of  $\overline{ADSP}$ . The differences between cycles initiated with  $\overline{ADSC}$  and  $\overline{ADSP}$  are as follows:

- $\overline{ADSP}$  must be sampled HIGH when  $\overline{ADSC}$  is sampled LOW to initiate a cycle with  $\overline{ADSC}$ .
- $\overline{WE}$  signals are sampled on the clock edge that samples  $\overline{ADSC}$  LOW (and  $\overline{ADSP}$  HIGH).
- Master chip select  $\overline{CE0}$  blocks  $\overline{ADSP}$ , but not  $\overline{ADSC}$ .

The AS7C33128PFD18B operates from a 3.3V supply. I/Os use a separate power supply that can operate at 2.5V or 3.3V. These devices are available in a 100-pin 14 $\times$ 20 mm TQFP package.

## TQFP capacitance

Parameter	Symbol	Test conditions	Min	Max	Unit
Input capacitance	$C_{IN}^*$	$V_{IN} = 0V$	-	5	pF
I/O capacitance	$C_{I/O}^*$	$V_{OUT} = 0V$	-	7	pF

\* Guaranteed not tested

## TQFP thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient) <sup>1</sup>	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1-layer	$\theta_{JA}$	40	°C/W
		4-layer	$\theta_{JA}$	22	°C/W
Thermal resistance (junction to top of case) <sup>1</sup>			$\theta_{JC}$	8	°C/W

<sup>1</sup> This parameter is sampled

1. PowerPC™ is a trademark International Business Machines Corporation



### Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ , ZZ, $\overline{LBO}$ are synchronous to this clock.
A, A0, A1	I	SYNC	Address. Sampled when all chip enables are active and ADSP or ADSC are asserted.
DQ[a,b]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when ADSP or ADSC is active. When CE0 is inactive, ADSP is blocked. Refer to the Synchronous Truth Table for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active LOW, respectively. Sampled on clock edges when ADSC is active or when $\overline{CE0}$ and ADSP are active.
ADSP	I	SYNC	Address strobe (processor). Asserted LOW to load a new address or to enter standby mode.
ADSC	I	SYNC	Address strobe (controller). Asserted LOW to load a new address or to enter standby mode.
ADV	I	SYNC	Burst advance. Asserted LOW to continue burst read/write.
$\overline{GWE}$	I	SYNC	Global write enable. Asserted LOW to write all 18 bits. When HIGH, BWE and BW[a,b] control write enable.
$\overline{BWE}$	I	SYNC	Byte write enable. Asserted LOW with $\overline{GWE}$ = HIGH to enable effect of BW[a,b] inputs.
$\overline{BW[a,b]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW. If any of $\overline{BW[a,b]}$ is active with $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW the cycle is a write cycle. If all $\overline{BW[a,b]}$ are inactive, the cycle is a read cycle.
$\overline{OE}$	I	ASYN	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is in read mode.
$\overline{LBO}$	I	STATIC	Selects Burst mode. When tied to $V_{DD}$ or left floating, device follows interleaved Burst order. When driven Low, device follows linear Burst order. <i>This signal is internally pulled High.</i>
ZZ	I	ASYN	Snooze. Places device in low power mode; data is retained. Connect to GND if unused.
NC	-	-	No connect

### Snooze Mode

SNOOZE MODE is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of SNOOZE MODE is dictated by the length of time the ZZ is in a High state.

The ZZ pin is an asynchronous, active high input that causes the device to enter SNOOZE MODE.

When the ZZ pin becomes a logic High,  $I_{SB2}$  is guaranteed after the time  $t_{ZZ1}$  is met. After entering SNOOZE MODE, all inputs except ZZ is disabled and all outputs go to High-Z. Any operation pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during  $t_{PUS}$ , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SNOOZE MODE.



### Write enable truth table (per byte)

Function	$\overline{\text{GWE}}$	$\overline{\text{BWE}}$	$\overline{\text{BWa}}$	$\overline{\text{BWb}}$
Write All Bytes	L	X	X	X
	H	L	L	L
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Read	H	H	X	X
	H	L	H	H

**Key:** X = don't care, L = low, H = high, n = a, b;  $\overline{\text{BWE}}$ ,  $\overline{\text{BWn}}$  = internal write signal.

### Asynchronous Truth Table

Operation	ZZ	$\overline{\text{OE}}$	I/O Status
Snooze mode	H	X	High-Z
Read	L	L	Dout
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care"
2. ZZ pin is pulled down internally
3. For write cycles that follows read cycles, the output buffers must be disabled with  $\overline{\text{OE}}$ , otherwise data bus contention will occur.
4. Snooze mode means power down state of which stand-by current does not depend on cycle times
5. Deselected means power down state of which stand-by current depends on cycle times

### Burst sequence table

Interleaved burst address ( $\overline{\text{LBO}} = 1$ )					Linear burst address ( $\overline{\text{LBO}} = 0$ )				
	A1 A0	A1 A0	A1 A0	A1 A0		A1 A0	A1 A0	A1 A0	A1 A0
1 <sup>st</sup> Address	0 0	0 1	1 0	1 1	1 <sup>st</sup> Address	0 0	0 1	1 0	1 1
2 <sup>nd</sup> Address	0 1	0 0	1 1	1 0	2 <sup>nd</sup> Address	0 1	1 0	1 1	0 0
3 <sup>rd</sup> Address	1 0	1 1	0 0	0 1	3 <sup>rd</sup> Address	1 0	1 1	0 0	0 1
4 <sup>th</sup> Address	1 1	1 0	0 1	0 0	4 <sup>th</sup> Address	1 1	1 0	0 1	1 0

Synchronous truth table<sup>[4]</sup>

$\overline{\text{CE0}}^1$	CE1	$\overline{\text{CE2}}$	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}^{[2]}$	$\overline{\text{OE}}$	Address accessed	CLK	Operation	DQ
H	X	X	X	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	L	X	L	X	X	X	X	NA	L to H	Deselect	Hi-Z
L	L	X	H	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	X	H	L	X	X	X	X	NA	L to H	Deselect	Hi-Z
L	X	H	H	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	H	L	L	X	X	X	L	External	L to H	Begin read	Q
L	H	L	L	X	X	X	H	External	L to H	Begin read	Hi-Z
L	H	L	H	L	X	H	L	External	L to H	Begin read	Q
L	H	L	H	L	X	H	H	External	L to H	Begin read	Hi-Z
X	X	X	H	H	L	H	L	Next	L to H	Continue read	Q
X	X	X	H	H	L	H	H	Next	L to H	Continue read	Hi-Z
X	X	X	H	H	H	H	L	Current	L to H	Suspend read	Q
X	X	X	H	H	H	H	H	Current	L to H	Suspend read	Hi-Z
H	X	X	X	H	L	H	L	Next	L to H	Continue read	Q
H	X	X	X	H	L	H	H	Next	L to H	Continue read	Hi-Z
H	X	X	X	H	H	H	L	Current	L to H	Suspend read	Q
H	X	X	X	H	H	H	H	Current	L to H	Suspend read	Hi-Z
L	H	L	H	L	X	L	X	External	L to H	Begin write	D <sup>3</sup>
X	X	X	H	H	L	L	X	Next	L to H	Continue write	D
H	X	X	X	H	L	L	X	Next	L to H	Continue write	D
X	X	X	H	H	H	L	X	Current	L to H	Suspend write	D
H	X	X	X	H	H	L	X	Current	L to H	Suspend write	D

1 X = don't care, L = low, H = high

2 For  $\overline{\text{WRITE}}$ , L means any one or more byte write enable signals ( $\overline{\text{BWa}}$  or  $\overline{\text{BWb}}$ ) and  $\overline{\text{BWE}}$  are LOW or  $\overline{\text{GWE}}$  is LOW.  $\overline{\text{WRITE}} = \text{HIGH}$  for all  $\overline{\text{BWx}}$ ,  $\overline{\text{BWE}}$ ,  $\overline{\text{GWE}}$  HIGH. See "Write enable truth table (per byte)," on page 7 for more information.

3 For write operation following a READ,  $\overline{\text{OE}}$  must be high before the input data set up time and held high throughout the input hold time.

4. ZZ pin is always Low.



### Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	$V_{DD}, V_{DDQ}$	-0.5	+4.6	V
Input voltage relative to GND (input pins)	$V_{IN}$	-0.5	$V_{DD} + 0.5$	V
Input voltage relative to GND (I/O pins)	$V_{IN}$	-0.5	$V_{DDQ} + 0.5$	V
Power dissipation	$P_d$	—	1.8	W
Short circuit output current	$I_{OUT}$	—	20	mA
Storage temperature	$T_{stg}$	-65	+150	°C
Temperature under bias	$T_{bias}$	-65	+135	°C

Stresses greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

### Recommended operating conditions at 3.3V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	$V_{DD}$	3.135	3.3	3.465	V
Supply voltage for I/O	$V_{DDQ}$	3.135	3.3	3.465	V
Ground supply	$V_{SS}$	0	0	0	V

### Recommended operating conditions at 2.5V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	$V_{DD}$	3.135	3.3	3.465	V
Supply voltage for I/O	$V_{DDQ}$	2.375	2.5	2.625	V
Ground supply	$V_{SS}$	0	0	0	V





### DC electrical characteristics for 3.3V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current <sup>†</sup>	$ I_{LI} $	$V_{DD} = \text{Max}, 0V \leq V_{IN} \leq V_{DD}$	-2	2	$\mu A$
Output leakage current	$ I_{LO} $	$OE \geq V_{IH}, V_{DD} = \text{Max}, 0V \leq V_{OUT} \leq V_{DDQ}$	-2	2	$\mu A$
Input high (logic 1) voltage	$V_{IH}$	Address and control pins	2*	$V_{DD}+0.3$	V
		I/O pins	2*	$V_{DDQ}+0.3$	
Input low (logic 0) voltage	$V_{IL}$	Address and control pins	-0.3**	0.8	V
		I/O pins	-0.5**	0.8	
Output high voltage	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{DDQ} = 3.135V$	2.4	—	V
Output low voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{DDQ} = 3.465V$	—	0.4	V

### DC electrical characteristics for 2.5V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current <sup>†</sup>	$ I_{LI} $	$V_{DD} = \text{Max}, 0V \leq V_{IN} \leq V_{DD}$	-2	2	$\mu A$
Output leakage current	$ I_{LO} $	$OE \geq V_{IH}, V_{DD} = \text{Max}, 0V \leq V_{OUT} \leq V_{DDQ}$	-2	2	$\mu A$
Input high (logic 1) voltage	$V_{IH}$	Address and control pins	1.7*	$V_{DD}+0.3$	V
		I/O pins	1.7*	$V_{DDQ}+0.3$	V
Input low (logic 0) voltage	$V_{IL}$	Address and control pins	-0.3**	0.7	V
		I/O pins	-0.3**	0.7	V
Output high voltage	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{DDQ} = 2.375V$	1.7	—	V
Output low voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{DDQ} = 2.625V$	—	0.7	V

<sup>†</sup> LBO and ZZ pins and have an internal pull-up or pull-down, and input leakage =  $\pm 10 \mu A$ .

\* $V_{IH} \text{ max} < V_{DD} + 1.5V$  for pulse width less than  $0.2 \times t_{CYC}$

\*\* $V_{IL} \text{ min} = -1.5$  for pulse width less than  $0.2 \times t_{CYC}$

### I<sub>DD</sub> operating conditions and maximum limits

Parameter	Sym	Conditions	-200	-166	-133	Unit
Operating power supply current <sup>1</sup>	$I_{CC}$	$\overline{CE0} \leq V_{IL}, CE1 \geq V_{IH}, \overline{CE2} \leq V_{IL}, f = f_{Max},$ $I_{OUT} = 0 \text{ mA}, ZZ \leq V_{IL}$	375	350	325	mA
Standby power supply current	$I_{SB}$	All $V_{IN} \leq 0.2V$ or $\geq V_{DD} - 0.2V$ , Deselected, $f = f_{Max}, ZZ \leq V_{IL}$	130	100	90	mA
	$I_{SB1}$	Deselected, $f = 0, ZZ \leq 0.2V$ , all $V_{IN} \leq 0.2V$ or $\geq V_{DD} - 0.2V$	30	30	30	
	$I_{SB2}$	Deselected, $f = f_{Max}, ZZ \geq V_{DD} - 0.2V$ , all $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$	30	30	30	

<sup>1</sup>  $I_{CC}$  given with no output loading.  $I_{CC}$  increases with faster cycle times and greater output loading.



### Timing characteristics over operating range

Parameter	Sym	-200		-166		-133		Unit	Notes <sup>1</sup>
		Min	Max	Min	Max	Min	Max		
Clock frequency	$f_{\text{Max}}$	–	200	–	166	–	133	MHz	
Cycle time	$t_{\text{CYC}}$	5	–	6	–	7.5	–	ns	
Clock access time	$t_{\text{CD}}$	–	3.0	–	3.5	–	4.0	ns	
Output enable LOW to data valid	$t_{\text{OE}}$	–	3.0	–	3.5	–	4.0	ns	
Clock HIGH to output Low Z	$t_{\text{LZC}}$	0	–	0	–	0	–	ns	2,3,4
Data output invalid from clock HIGH	$t_{\text{OH}}$	1.5	–	1.5	–	1.5	–	ns	2
Output enable LOW to output Low Z	$t_{\text{LZOE}}$	0	–	0	–	0	–	ns	2,3,4
Output enable HIGH to output High Z	$t_{\text{HZOE}}$	–	3.0	–	3.5	–	4.0	ns	2,3,4
Clock HIGH to output High Z	$t_{\text{HZC}}$	–	3.0	–	3.5	–	4.0	ns	2,3,4
Output enable HIGH to invalid output	$t_{\text{OHOE}}$	0	–	0	–	0	–	ns	
Clock HIGH pulse width	$t_{\text{CH}}$	2.0	–	2.4	–	2.5	–	ns	5
Clock LOW pulse width	$t_{\text{CL}}$	2.3	–	2.4	–	2.5	–	ns	5
Address setup to clock HIGH	$t_{\text{AS}}$	1.4	–	1.5	–	1.5	–	ns	6
Data setup to clock HIGH	$t_{\text{DS}}$	1.4	–	1.5	–	1.5	–	ns	6
Write setup to clock HIGH	$t_{\text{WS}}$	1.4	–	1.5	–	1.5	–	ns	6,7
Chip select setup to clock HIGH	$t_{\text{CSS}}$	1.4	–	1.5	–	1.5	–	ns	6,8
Address hold from clock HIGH	$t_{\text{AH}}$	0.4	–	0.5	–	0.5	–	ns	6
Data hold from clock HIGH	$t_{\text{DH}}$	0.4	–	0.5	–	0.5	–	ns	6
Write hold from clock HIGH	$t_{\text{WH}}$	0.4	–	0.5	–	0.5	–	ns	6,7
Chip select hold from clock HIGH	$t_{\text{CSH}}$	0.4	–	0.5	–	0.5	–	ns	6,8
$\overline{\text{ADV}}$ setup to clock HIGH	$t_{\text{ADVS}}$	1.4	–	1.5	–	1.5	–	ns	6
$\overline{\text{ADSP}}$ setup to clock HIGH	$t_{\text{ADSPS}}$	1.4	–	1.5	–	1.5	–	ns	6
$\overline{\text{ADSC}}$ setup to clock HIGH	$t_{\text{ADSCS}}$	1.4	–	1.5	–	1.5	–	ns	6
$\overline{\text{ADV}}$ hold from clock HIGH	$t_{\text{ADVH}}$	0.4	–	0.5	–	0.5	–	ns	6
$\overline{\text{ADSP}}$ hold from clock HIGH	$t_{\text{ADSPH}}$	0.4	–	0.5	–	0.5	–	ns	6
$\overline{\text{ADSC}}$ hold from clock HIGH	$t_{\text{ADSCH}}$	0.4	–	0.5	–	0.5	–	ns	6

<sup>1</sup> See “Notes” on page 16.

### Snooze Mode Electrical Characteristics

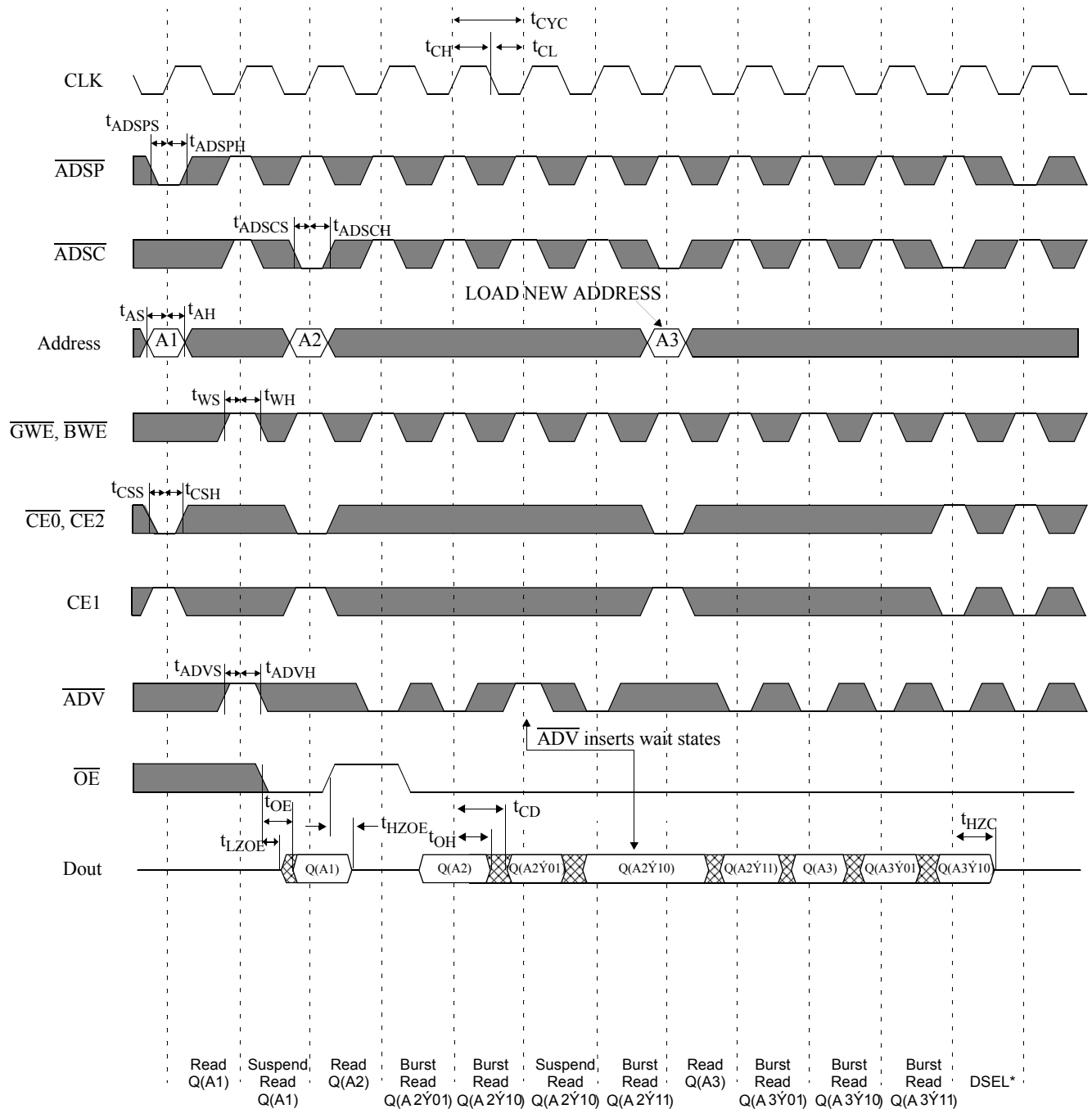
Description	Conditions	Symbol	Min	Max	Units
Current during Snooze Mode	$ZZ \geq V_{\text{IH}}$	$I_{\text{SB2}}$		30	mA
$ZZ$ active to input ignored		$t_{\text{PDS}}$	2		cycle
$ZZ$ inactive to input sampled		$t_{\text{PUS}}$	2		cycle
$ZZ$ active to SNOOZE current		$t_{\text{ZZI}}$		2	cycle
$ZZ$ inactive to exit SNOOZE current		$t_{\text{RZZI}}$	0		



## Key to switching waveforms

Rising input    
 Falling input    
 don't care    
 Undefined

## Timing waveform of read cycle

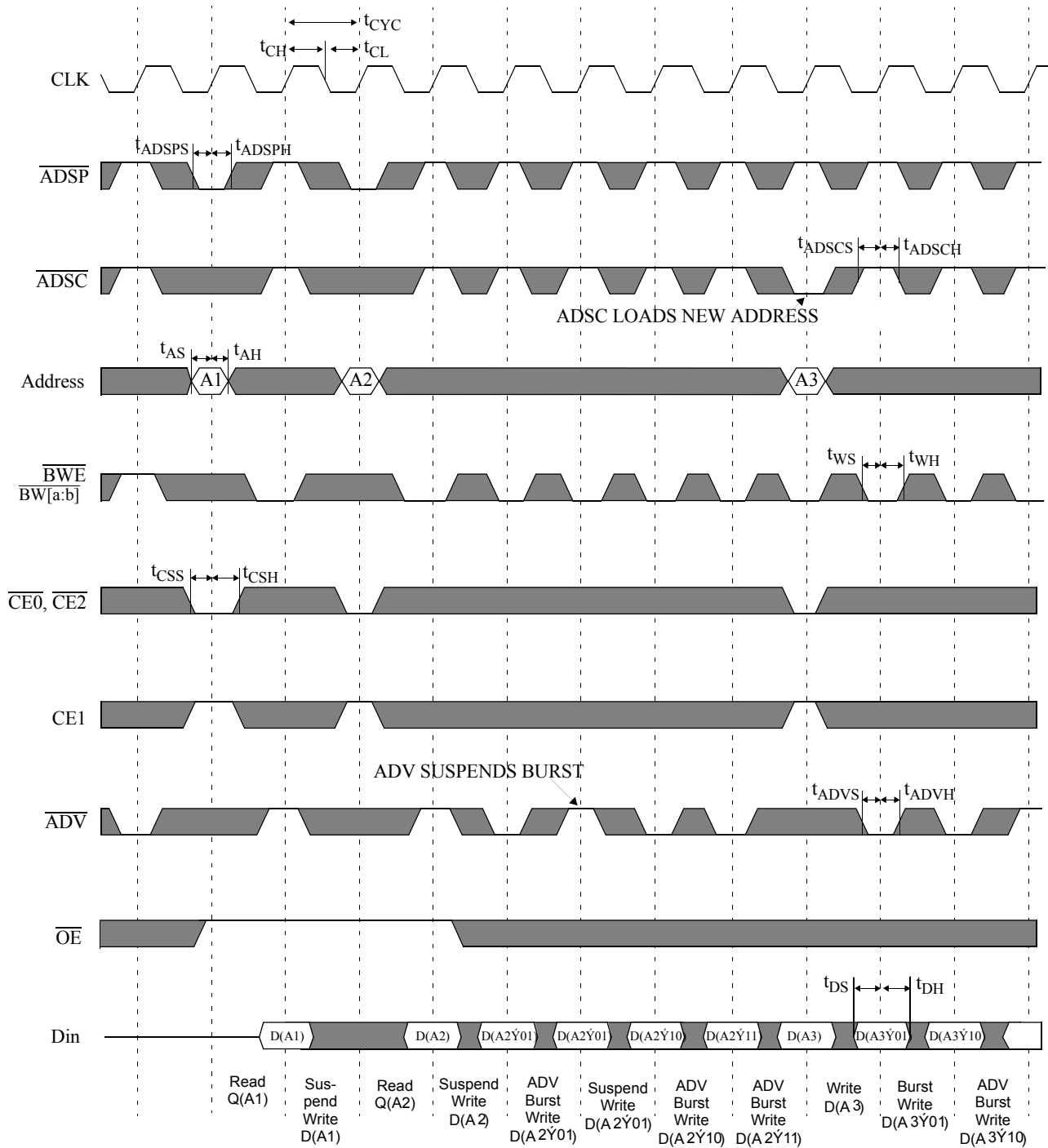


Note:  $\dot{Y}$  = XOR when  $\overline{LBO}$  = high/no connect;  $\dot{Y}$  = ADD when  $\overline{LBO}$  = low.  $\overline{BW[a:d]}$  is don't care.

\*Outputs are disabled within two clk cycles after DSEL command



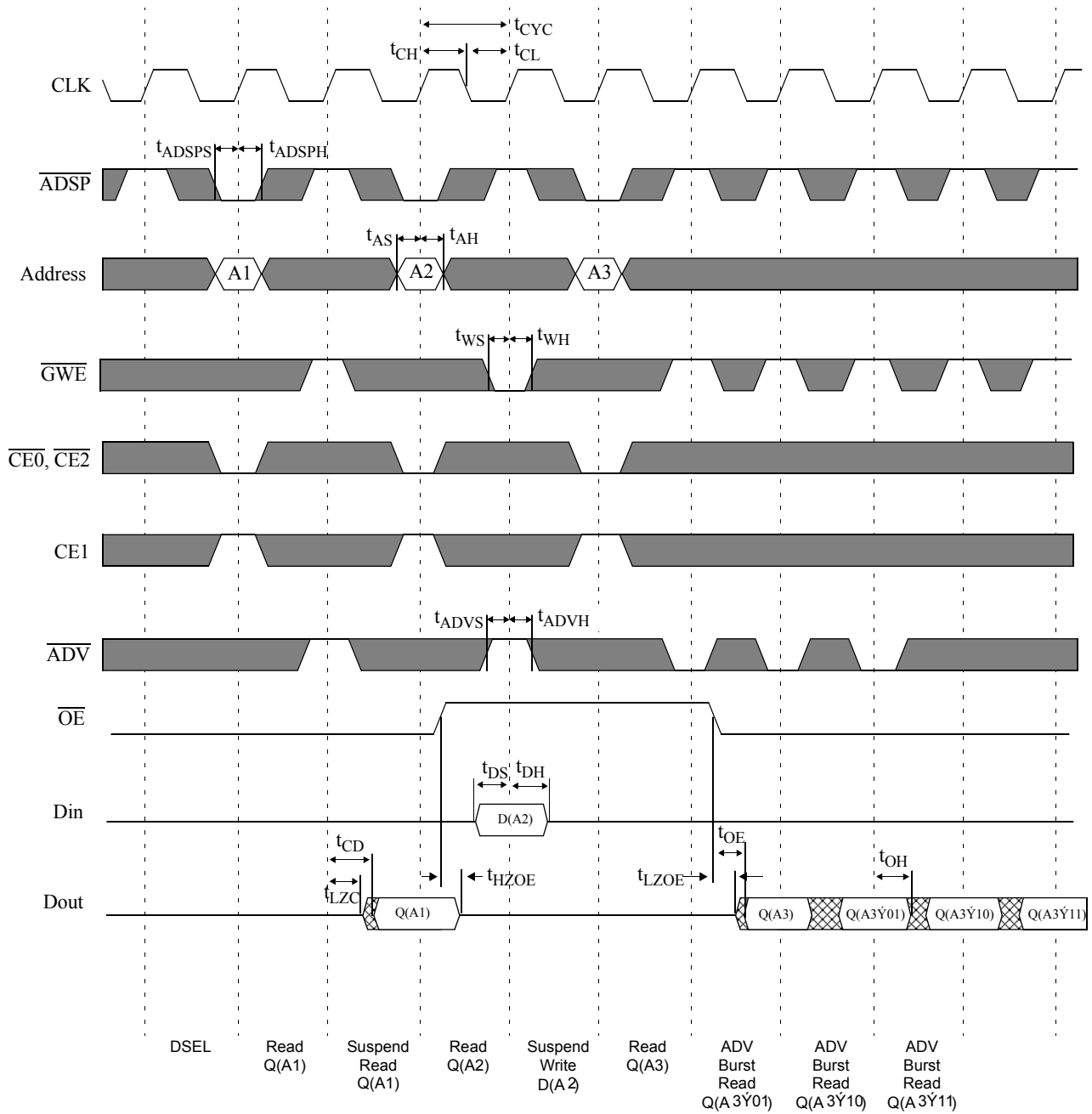
### Timing waveform of write cycle



Note:  $\hat{Y}$  = XOR when  $\overline{LBO}$  = high/no connect;  $\hat{Y}$  = ADD when  $\overline{LBO}$  = low.



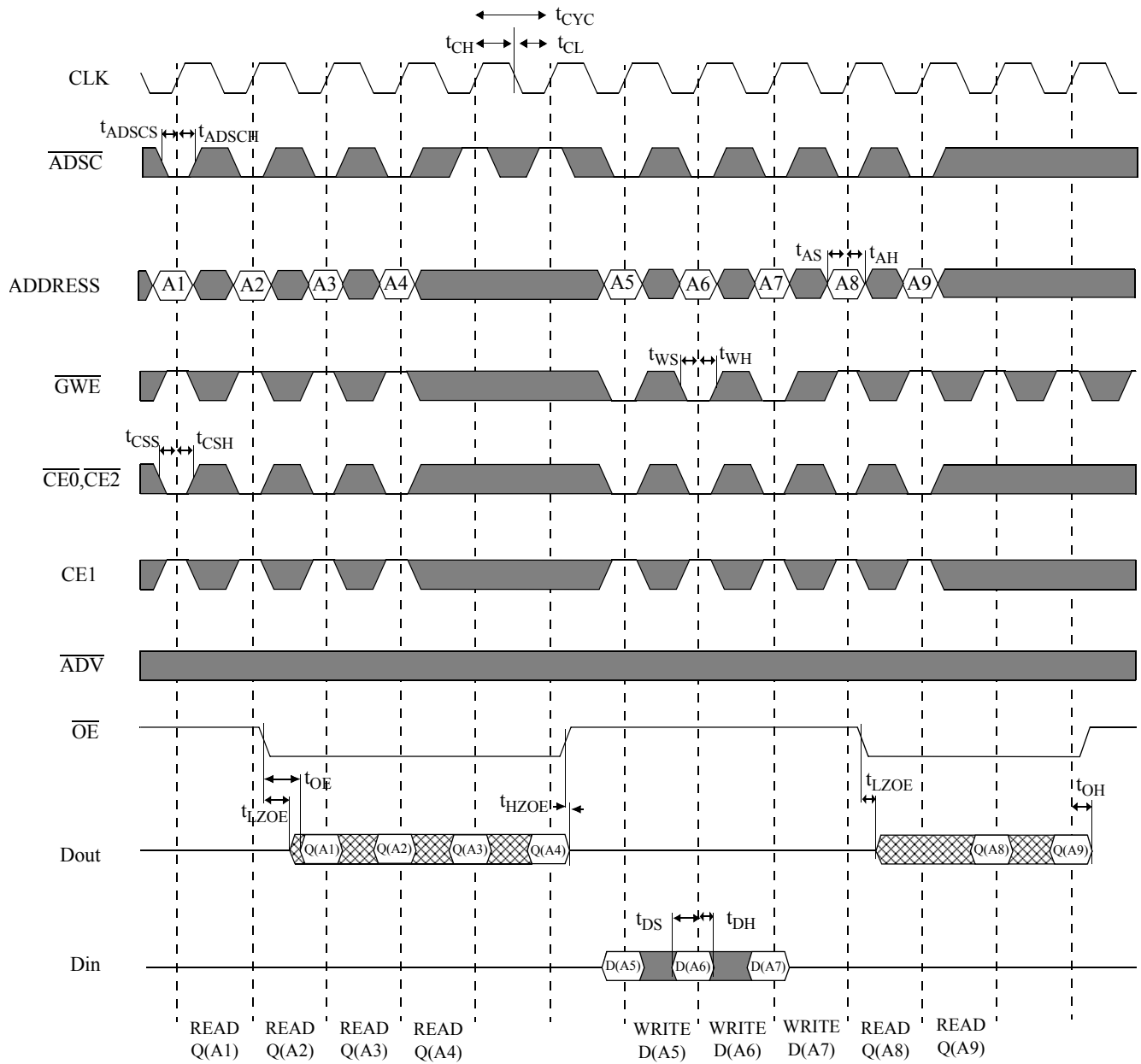
### Timing waveform of read/write cycle ( $\overline{\text{ADSP}}$ Controlled; $\overline{\text{ADSC}}$ High)



Note:  $\hat{Y}$  = XOR when  $\overline{\text{LB0}}$  = high/no connect;  $\hat{Y}$  = ADD when  $\overline{\text{LB0}}$  = low.



### Timing waveform of read/write cycle ( $\overline{\text{ADSC}}$ controlled, $\overline{\text{ADSP}} = \text{HIGH}$ )



[illegible]



## AC test conditions

- Output load: see Figure B, except for  $t_{LZC}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ ,  $t_{HZC}$ , see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

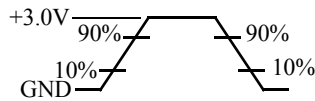


Figure A: Input waveform

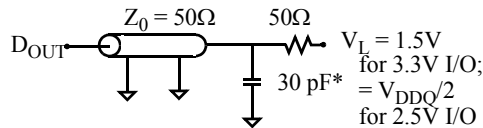


Figure B: Output load (A)

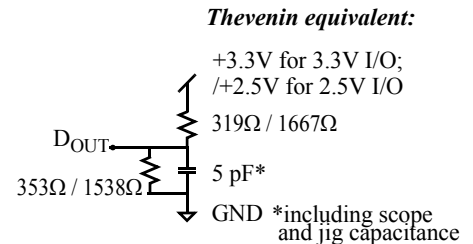


Figure C: Output load (B)

### Notes

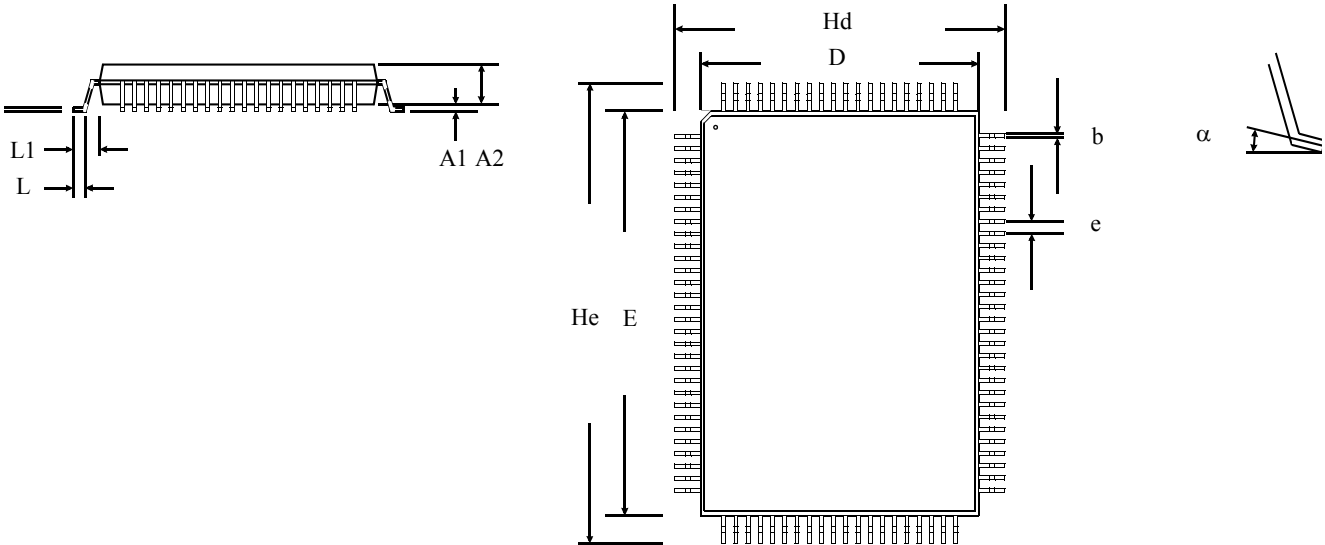
- 1 For test conditions, see *AC Test Conditions*, Figures A, B, C.
- 2 This parameter measured with output load condition in Figure C.
- 3 This parameter is sampled, but not 100% tested.
- 4  $t_{HZOE}$  is less than  $t_{LZOE}$ ; and  $t_{HZC}$  is less than  $t_{LZC}$  at any given temperature and voltage.
- 5  $t_{CH}$  measured as HIGH above  $V_{IH}$  and  $t_{CL}$  measured as LOW below  $V_{IL}$ .
- 6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
- 7 Write refers to  $\overline{GWE}$ ,  $\overline{BWE}$ ,  $BW[a,b]$ .
- 8 Chip select refers to  $\overline{CE0}$ ,  $CE1$ ,  $\overline{CE2}$





Package Dimensions

100-pin quad flat pack (TQFP)



	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.85	16.15
He	21.80	22.20
L	0.45	0.75
L1	1.00 nominal	
$\alpha$	0°	7°
Dimensions in millimeters		



### Ordering information

Package	Width	-200	-166	-133
TQFP	x18	AS7C33128PFD18B-200TQC	AS7C33128PFD18B-166TQC	AS7C33128PFD18B-133TQC
TQFP	x18	AS7C33128PFD18B-200TQI	AS7C33128PFD18B-166TQI	AS7C33128PFD18B-133TQI

Note

Add suffix 'N' to the above part numbers for lead free parts (Ex AS7C33128PFD18B-166TQCN)

### Part numbering guide

AS7C	33	128	PF	D	18	B	-XXX	TQ	C/I	X
1	2	3	4	5	6	7	8	9	10	11

1. Alliance Semiconductor SRAM Prefix
2. Operating voltage: 33 = 3.3V
3. Organization: 128 = 128K
4. Pipeline mode
5. Deselect: D = Double cycle deselect
6. Organization: 18 = x18
7. Production version: B = product revision
8. Clock speed (MHz)
9. Package type: TQ = TQFP
10. Operating temperature: C = Commercial (0° C to 70° C); I = Industrial (-40° C to 85° C)
11. N=Lead Free Part



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Document Version: v.1.2

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