



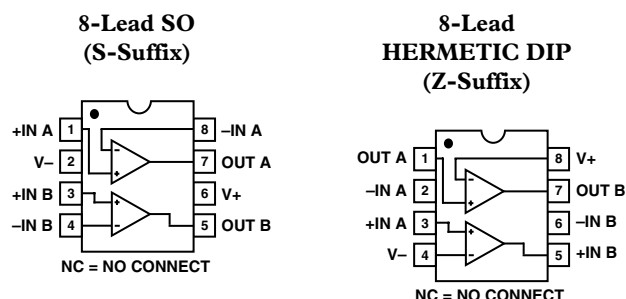
# Dual Low Power Operational Amplifier, Single or Dual Supply

## OP221

### FEATURES

Excellent TC<sub>Vos</sub> Match, 2  $\mu\text{V}/^\circ\text{C}$  Max  
Low Input Offset Voltage, 150  $\mu\text{V}$  Max  
Low Supply Current, 550  $\mu\text{A}$  Max  
Single Supply Operation, 5 V to 30 V  
Low Input Offset Voltage Drift, 0.75  $\mu\text{V}/^\circ\text{C}$   
High Open-Loop Gain, 1500 V/mV Min  
High PSRR, 3  $\mu\text{V}/\text{V}$   
Wide Common-Mode Voltage  
Range,  $V_-$  to within 1.5 V of  $V_+$   
Pin Compatible with 1458, LM158, LM2904  
Available in Die Form

### PIN CONNECTIONS



### GENERAL DESCRIPTION

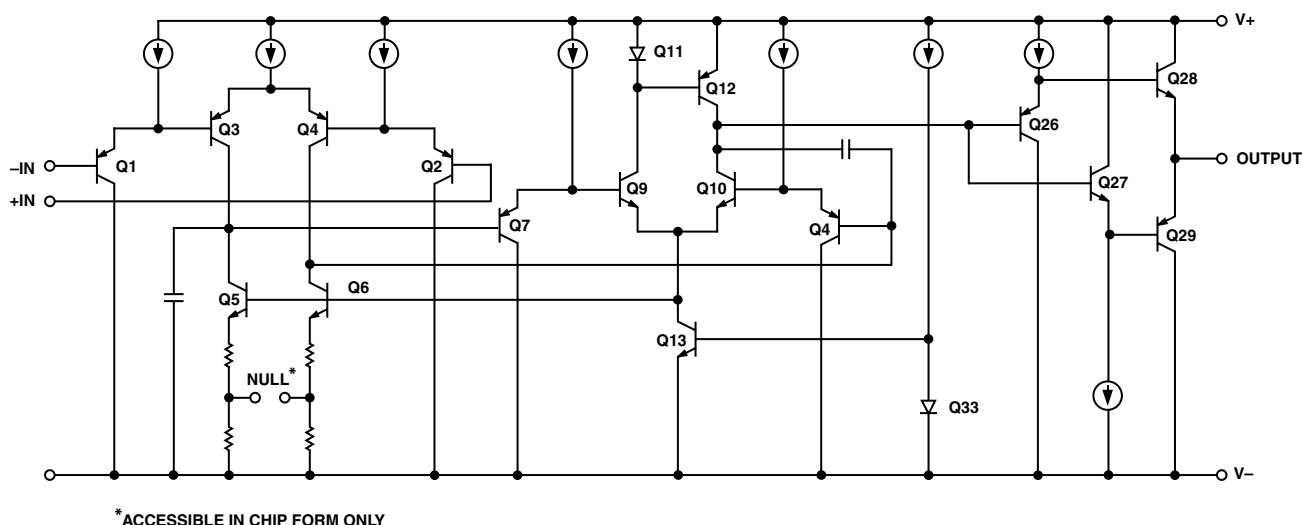
The OP221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP221 make it well-suited for operation from batteries or unregulated power supplies.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels

provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

### SIMPLIFIED SCHEMATIC



REV. A

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# OP221—SPECIFICATIONS (Electrical Characteristics at $V_S = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	OP221A/E			OP221G			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$		75	150		250	500		$\mu\text{V}$
Input Offset Current	$I_{OS}$	$V_{CM} = 0$	0.5	3		1.5	7		nA
Input Bias Current	$I_B$	$V_{CM} = 0$	55	100		70	120		nA
Input Voltage Range	IVR	$V_+ = 5\text{ V}$ , $V_- = 0\text{ V}$ (Note 2) $V_S = \pm 15\text{ V}$	0/3.5 -15/13.5			0/3.5 -15/13.5			V
Common-Mode Rejection Ratio	CMRR	$V_+ = -5\text{ V}$ , $V_- = 0\text{ V}$ $0\text{ V} \leq V_{CM} \leq 3.5\text{ V}$ $V_S = \pm 15\text{ V}$	90	100		75	85		dB
		$-15\text{ V} \leq V_{CM} \leq 13.5\text{ V}$	95	100		80	90		
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$		3	10		32	100	$\mu\text{V/V}$
		$V_- = 0\text{ V}$ , $V_+ = 5\text{ V}$ to $30\text{ V}$		6	18		57	180	
Large-Signal Voltage Gain	Avo	$V_S = \pm 15\text{ V}$ , $R_L = 10\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	1500			800			V/mV
Output Voltage Swing	$V_O$	$V_+ = 5\text{ V}$ , $V_- = 0\text{ V}$ $R_L = 10\text{ k}\Omega$	0.7/4.1			0.8/4			V
		$V_S = 15\text{ V}$ , $R_L = 10\text{ k}\Omega$	$\pm 13.8$			$\pm 13.5$			
Slew Rate	SR	$R_L = 10\text{ k}\Omega$ (Note 1)	0.2	0.3		0.2	0.3		V/ $\mu\text{S}$
Bandwidth	BW		600			600			kHz
Supply Current (Both Amplifiers)	$I_{SY}$	$V_S = \pm 2.5\text{ V}$ , No Load		450	550		550	650	$\mu\text{A}$
		$V_S = \pm 15\text{ V}$ , No Load		600	800		850	900	

## NOTES

<sup>1</sup>Sample tested.

<sup>2</sup>Guaranteed by CMRR test limits.

# SPECIFICATIONS

(Electrical Characteristics at  $V_S = \pm 2.5\text{ V}$  to  $\pm 15\text{ V}$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  for OP221A,  $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for OP221E,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for OP221G, unless otherwise noted.)

Parameter	Symbol	Conditions	OP221A/E			OP221G			Unit
			Min	Typ	Max	Min	Typ	Max	
Average Input Offset Voltage	$TCV_{OS}$			0.75	1.5		2	3	$\mu\text{V}/^\circ\text{C}$
Input Offset Voltage	$V_{OS}$			150	300		400	700	$\mu\text{V}$
Input Offset Current	$I_{OS}$	$V_{CM} = 0$		1	5		2	10	nA
Input Bias Current	$I_B$	$V_{CM} = 0$		55	100		80	140	nA
Input Voltage Range	IVR	$V_+ = 5\text{ V}$ , $V_- = 0\text{ V}$ (Note 2) $V_S = \pm 15\text{ V}$	0/3.2 -15/13.2			0/3.2 -15/13.2			V
Common-Mode Rejection Ratio	CMRR	$V_+ = -5\text{ V}$ , $V_- = 0\text{ V}$ $0\text{ V} \leq V_{CM} \leq 3.5\text{ V}$ $V_S = \pm 15\text{ V}$	85	90		70	80		dB
		$-15\text{ V} \leq V_{CM} \leq 13.5\text{ V}$	90	95		75	85		
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$ $V_- = 0\text{ V}$ , $V_+ = 5\text{ V}$ to $30\text{ V}$		6 10	18 32		57 100	180 320	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	$A_{VO}$	$V_S = \pm 15\text{ V}$ , $R_L = 10\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	1000			600			V/mV
Output Voltage Swing	$V_O$	$V_+ = 5\text{ V}$ , $V_- = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ $V_S = 15\text{ V}$ , $R_L = 10\text{ k}\Omega$	0.8/3.8  $\pm 13.5$			0.9/3.7  13.2			V
Supply Current (Both Amplifiers)	$I_{SY}$	$V_S = \pm 2.5\text{ V}$ , No Load $V_S = \pm 15\text{ V}$ , No Load		500 700	650 900		600 950	750 1000	$\mu\text{A}$

## NOTES

<sup>1</sup>Sample tested.<sup>2</sup>Guaranteed by CMRR test limits.

## Matching Characteristics at $V_S = \pm 15\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	OP221A/E			OP221G			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage Match	$\Delta V_{OS}$			50	200		250	600	$\mu\text{V}$
Average Noninverting Bias Current	$I_{B+}$				80			120	nA
Noninverting Input Offset Current	$I_{OS+}$			2	5		4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta\text{CMRR}$	$V_{CM} = -15\text{ V}$ to $13.5\text{ V}$	92			72			dB
Power Supply Rejection Ratio Match (Note 1)	$\Delta\text{PSRR}$	$V_S = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$			14			140	$\mu\text{V}/\text{V}$

# OP221—SPECIFICATIONS

(Matching Characteristics at  $V_S = \pm 15\text{ V}$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  for OP221A,  $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for OP221E,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for OP221G, unless otherwise noted. Grades E and G are sample tested.)

Parameter	Symbol	Conditions	OP221A/E			OP221G			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage Match	$\Delta V_{OS}$			100	400		400	800	$\mu\text{V}$
Average Noninverting Bias Current	$I_{B+}$	$V_{CM} = 0$			100			140	nA
Input Offset Voltage Tracking	$IC\Delta V_{OS}$			1	2		3	5	$\mu\text{V}^\circ\text{C}$
Noninverting Input Offset Current	$I_{OS+}$	$V_{CM} = 0$		3	7		6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta\text{CMRR}$	$V_{CM} = -15\text{ V to } 13.2\text{ V}$	87	90		72	80		dB
Power Supply Rejection Ratio Match (Note 1)	$\Delta\text{PSRR}$				26		140	$\mu\text{V/V}$	

## NOTES

<sup>1</sup> $\Delta\text{CMRR}$  is  $20 \log_{10} V_{CM}/\Delta\text{CME}$ , where  $V_{CM}$  is the voltage applied to both noninverting inputs and  $\Delta\text{CME}$  is the difference in common-mode input-referred error.

<sup>2</sup> $\Delta\text{PSRR}$  is: Input-Referred Differential Error  
 $\Delta V_S$

**Wafer Test Limits at  $V_S = \pm 2.5\text{ V to } \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.**

Parameter	Symbol	Conditions	OP221N Limit	Unit
Input Offset Voltage	$V_{OS}$		200	$\mu\text{V Max}$
Input Offset Current	$I_{OS}$	$V_{CM} = 0$	3.5	nA Max
Input Bias Current	$I_B$	$V_{CM} = 0$	85	nA Max
Input Voltage Range	IVR	$V_+ = 5\text{ V}$ , $V_- = 0\text{ V}$ $V_S = \pm 15\text{ V}$	0/3.5 -15/13.5	V Min/Max V Min
Common-Mode Rejection Ratio	CMRR	$V_- = 0\text{ V}$ , $V_+ = 5\text{ V}$ , $0\text{ V} \leq V_{CM} \leq 3.5\text{ V}$ $V_S = \pm 15\text{ V}$ $-15\text{ V} \leq V_{CM} \leq 13.5\text{ V}$	88 93	dB Min
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V to } \pm 15\text{ V}$ $V_- = 0\text{ V}$ , $V_+ = 5\text{ V to } 30\text{ V}$	12.5 22.5	V/mV Min
Large-Signal Voltage Gain	Avo	$V_S = \pm 15\text{ V}$ $R_L = 10\text{ k}\Omega$	1500	V/mV Max
Output Voltage Swing	$V_O$	$V_+ = 5\text{ V}$ , $V_- = 0\text{ V}$ , $R_L = 10\text{ k}\Omega$ $V_S = 15\text{ V}$ , $R_L = 10\text{ k}\Omega$	0.7/4.1 $\pm 13.8$	V Min/Max V Min
Supply Current (Both Amplifiers)	$I_{SY}$	$V_S = \pm 2.5\text{ V}$ , No Load $V_S = \pm 15\text{ V}$ , No Load	560 810	$\mu\text{A Max}$

## NOTE

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 18$ V
Differential Input Voltage	30 V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	
OP221A	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
OP221E	$-25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
OP221G	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Lead Temperature (Soldering 60 sec)	$300^{\circ}\text{C}$
Junction Temperature ( $T_J$ )	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$

Package Type	$\theta_{JA}$ (Note 2)	$\theta_{JC}$	Unit
8-Lead Hermetic DIP (Z)	148	16	$^{\circ}\text{C}/\text{W}$
8-Lead Plastic DIP (P)	103	43	$^{\circ}\text{C}/\text{W}$
8-Lead SO (S)	158	43	$^{\circ}\text{C}/\text{W}$

## NOTES

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

<sup>2</sup> $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO, CerDip, and PDIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

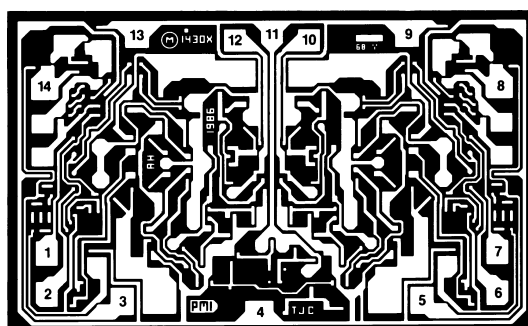
## ORDERING INFORMATION<sup>1,2</sup>

$T_A = +25^{\circ}\text{C}$ $V_{OS\text{ MAX}}$ ( $\mu\text{V}$ )	Packages		Operating Temperature Range	Package Options
	Cerdip 8-Lead	Plastic 8-Lead		
150	OP221AZ <sup>3</sup>		MIL	Q-8
150	OP221EZ <sup>3</sup>		IND	
300				
500				
500		OP221GP <sup>3</sup>	XIND	R-8
500		OP221GS	XIND	

<sup>1</sup>Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

<sup>2</sup>For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

<sup>3</sup>Not for new design, obsolete April 2002.



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4.  $V^-$
5. BALANCE (B)
6. INVERTING INPUT (B)
7. NONINVERTING INPUT (B)
8. BALANCE (B)
9.  $V^+$
10. OUT (B)
11.  $V^+$
12. OUT (A)
13.  $V^+$
14. BALANCE (A)

DIE SIZE 0.097 X 0.063 INCH, 6111 SQ. MILS  
(2.464 X 1.600 MM, 3.94 SQ. MM)

NOTE: ALL  $V^+$  PADS ARE INTERNALLY CONNECTED.

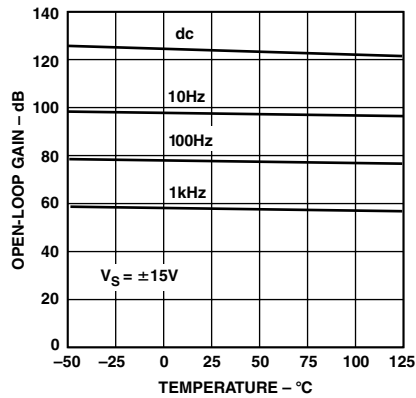
Figure 1. Dice Characteristics

## CAUTION

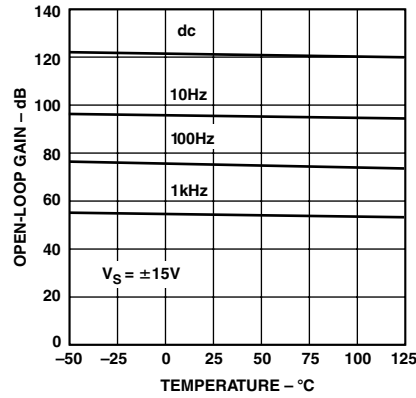
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP221 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



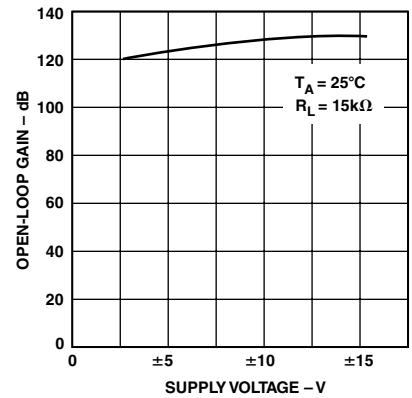
# Typical Performance Characteristics – OP221



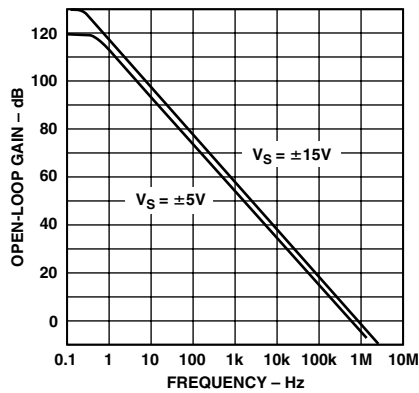
TPC 1. Open-Loop Gain at  $\pm 15$  V vs. Temperature



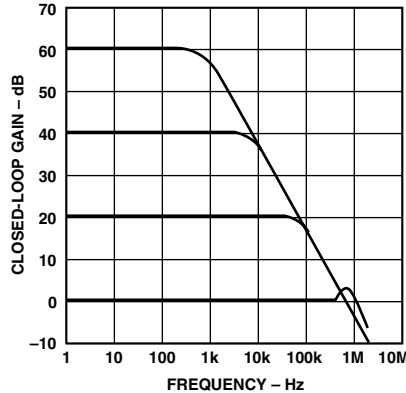
TPC 2. Open-Loop Gain at  $\pm 5$  V vs. Temperature



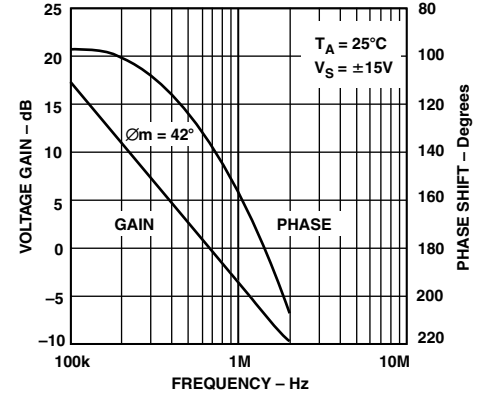
TPC 3. Open-Loop Gain at vs. Supply Voltage



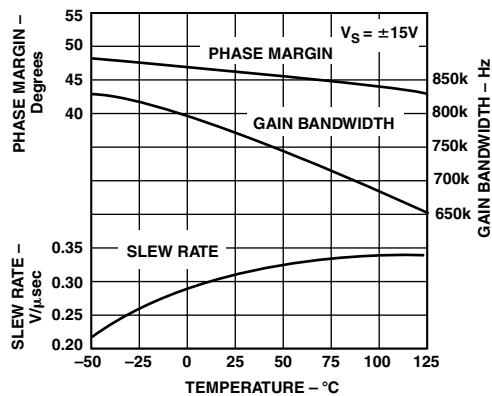
TPC 4. Open-Loop Gain at  $\pm 15$  V vs. Frequency



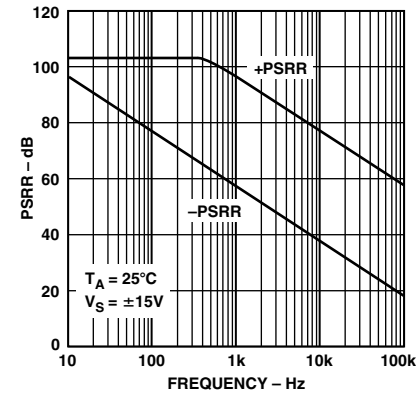
TPC 5. Closed-Loop Gain vs. Frequency



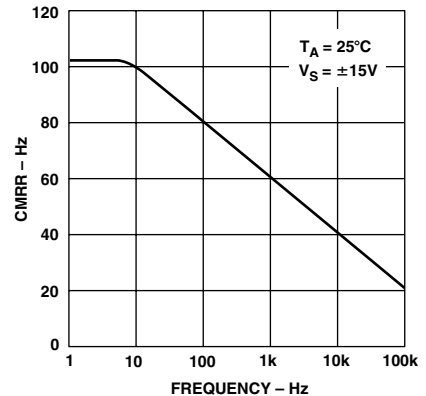
TPC 6. Gain and Phase Shift vs. Frequency



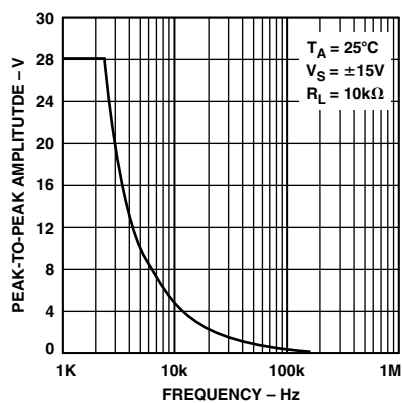
TPC 7. Phase Margin, Gain Bandwidth, and Slew Rate vs. Temperature



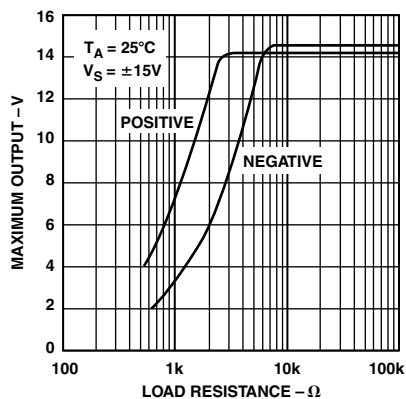
TPC 8. PSRR vs. Frequency



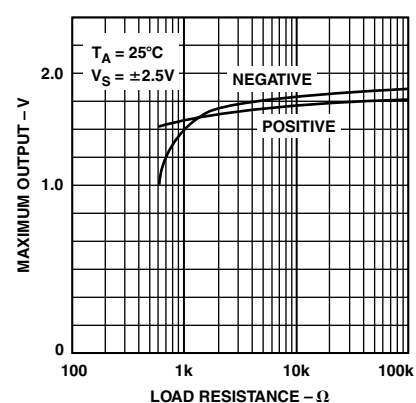
TPC 9. CMRR vs. Frequency



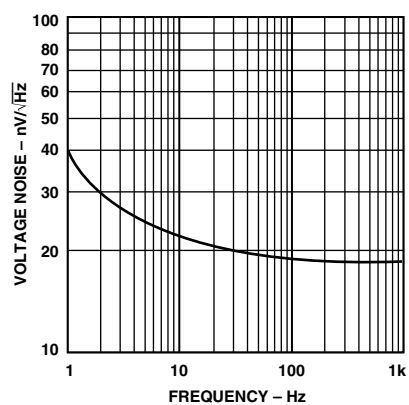
TPC 10. Maximum Output Swing vs. Frequency



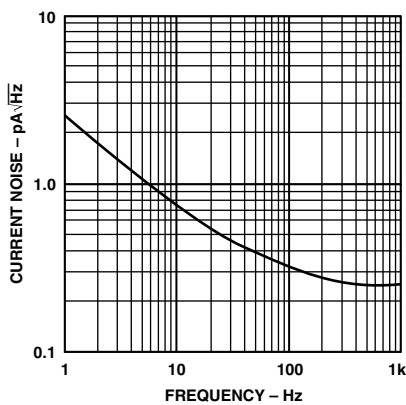
TPC 11. Maximum Output Voltage vs. Load Resistance



TPC 12. Maximum Output Voltage vs. Load Resistance



TPC 13. Voltage Noise Density vs. Frequency



TPC 13. Current Noise Density vs. Frequency

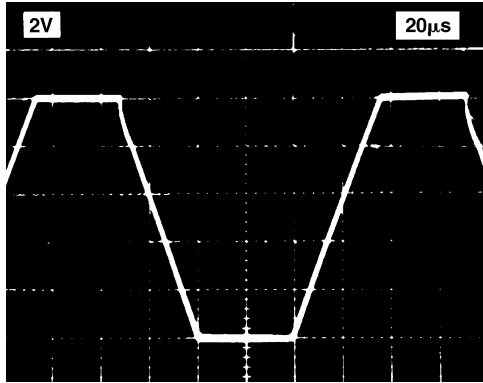


Figure 2a. Noninverting Step Response

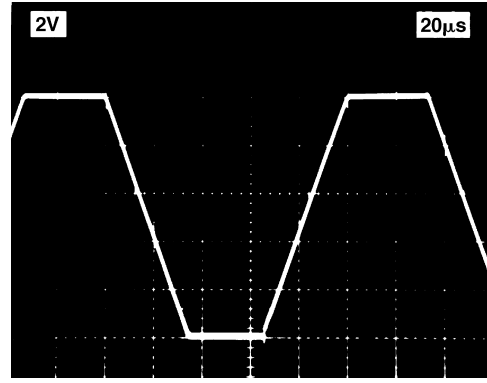


Figure 3a. Inverting Step Response

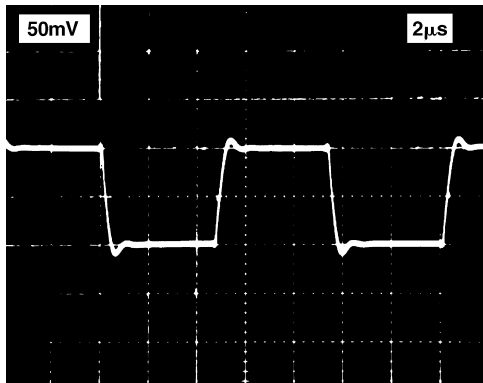


Figure 2b. Noninverting Step Response

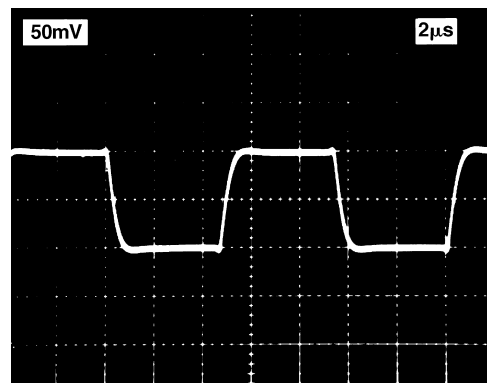


Figure 3b. Inverting Step Response

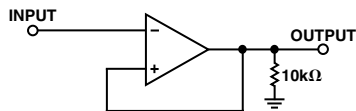


Figure 4. TBD.

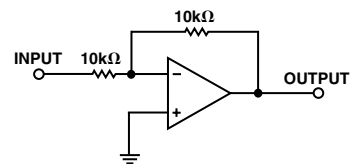


Figure 5. TBD.



## SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

### Advantages of Dual Monolithic Operational Amplifiers

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of dc errors in the individual amplifiers.

Reference to the circuit shown in Figure 6, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the difference (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters—offset voltage, offset voltage drift, inverting and noninverting bias currents, common mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operation amplifier circuits.

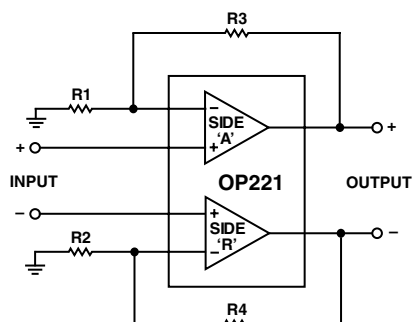


Figure 6. Differential-In, Differential-Out Amplifier

## INSTRUMENTATION AMPLIFIER APPLICATIONS

### Two-Op Amp Configuration

The two-op amp circuit (Figure 7) is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1. The high open-loop gain of the OP221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 (Ao1) causes undesired feedthrough of the common-mode input. For  $A_d/A_o \ll 1$ , the common-mode error (CME) at the output due to this effect is approximately  $(2 A_d/A_o1) \times V_{CM}$ . This circuit features independent adjustment of CMRR and differential gain.

### Three-Op Amp Configuration

The three-op amp circuit (Figure 8) has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 7. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

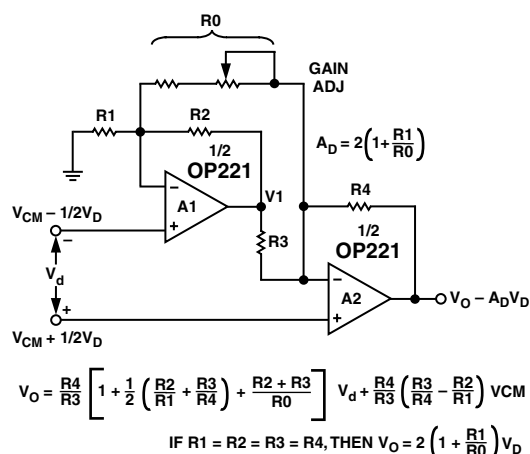


Figure 7. Two-Op Amp Circuit

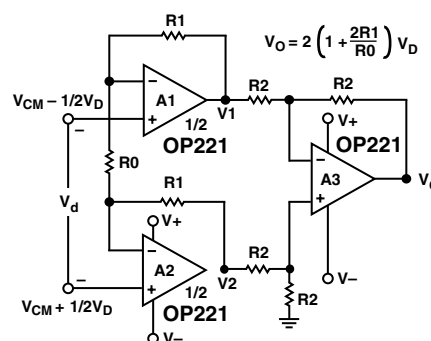


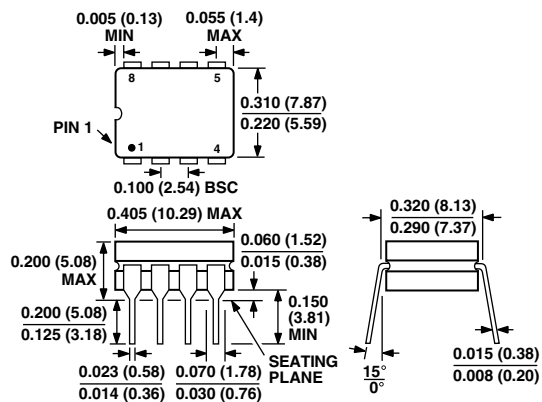
Figure 8. Three-Op Amp Circuit

# OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

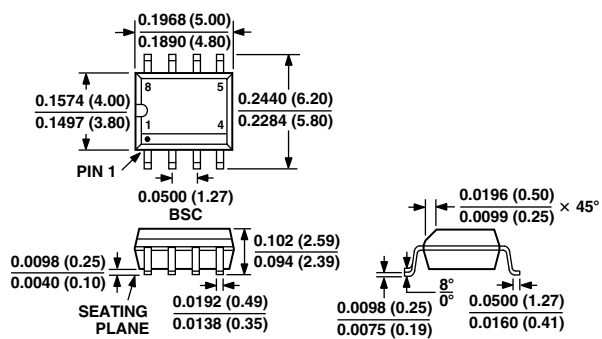
## 8-Lead CERDIP Package

(Q-8)



## 8-Lead SOIC Package

(R-8)



# Revision History

Location	Page
09/01—Data Sheet changed from REV. 0 to REV. A.	
Edits to PIN CONNECTIONS .....	1
Global deletion of references to OP221B and OP221C .....	2, 3, 4
Edits to WAFER TEST LIMITS .....	4
Edits to ABSOLUTE MAXIMUM RATINGS .....	5
Edits to ORDERING GUIDE .....	5
Edits to PACKAGE TYPE .....	5

