ZR38650

DATA SHEET

PROGRAMMABLE DIGITAL AUDIO PROCESSOR

FEATURES

- Full-Function Digital Audio Processor Hardware
  - 50 MIPS performance with multi-operation instructions
  - Large internal RAMs/ROM plus low-cost external memory
  - Wide selection of on-chip digital audio peripherals
  - Flexible interface for host or no-host operation
- Standard Software Functions in ROM
  - Dolby Digital AC-3, 5.1 channel and 2 channel decoding up to 640 Kbits per second
  - Dolby Pro Logic encoding and decoding
  - MPEG1 and MPEG2 two channel decoding with MPEG2 PES stream parsing, PTS decoding and SCR handling
- Downloadable *SiliconSoftware™* Functions
  - Tomorrow's ever-changing standards plus today's:
  - Aureal A3D, Dolby Virtual Surround, Harman VMAx
  - QSound QSurround™, Spatializer N-2-2™, Home THX
  - SRS TruSurround, Music Modes, Bass Management
- Flexible Input/Output
  - Serial and/or parallel data stream I/O
  - Serial SPI, serial Z2C or 8-bit parallel host interface
  - 3 serial input data ports and 4 serial data output ports
  - Formatted S/PDIF receiver with up to 96 kHz sample rate
  - Sample rates: 32 kHz, 44.1 kHz, 48 kHz or 96 kHz
  - Formatted S/PDIF AC-3 and MPEG transmitter output
- Low System Cost
  - Host-less operation with no glue chips
  - Separate internal PLLs for DSP core and audio I/O
  - No external RAM required for 5.1 Dolby AC-3/MPEG2
  - Wait-state generation for low-cost external memory
  - 144-pin Plastic Thin Quad Flat Pack (TQFP) package
  - 3.3 V supply with 5 V compatible I/O for low power

DESCRIPTION

The Zoran ZR38650 is a full-function, high performance programmable digital audio signal processor. It is today capable of real-time single-chip decoding of Dolby Digital AC-3 and MPEG2 digital surround algorithms with its standard ROM and *SiliconSoftware* functions. It is also today's best digital audio platform for meeting tomorrow's constantly evolving digital audio algorithm requirements. Using the proven ZR38000 architecture, it is the fourth generation audio processor made by Zoran.

Because of its programmable high performance and high level of integration, the ZR38650 is unusually flexible in meeting a wide range of system requirements at the lowest possible system cost. At the low end it can provide standard fixed decoding functions with only a DAC and an optical interface for the S/PDIF input in addition to the oscillator crystal. At the high end it can provide eight channels of output, analog input, long-delay memories, custom operating features and the ability to be upgraded with downloaded *SiliconSoftware* product enhancements. Yet all of this flexibility comes without design complexity. Highly configurable standard functions with a simple command structure minimize software development, while a full set of development tools are available for the highly-custom product developer.

The ZR38650 is suitable for primarily audio applications such as Audio/Visual home theater receivers, Digital Audio Broadcast (DAB), 3-D audio, six-channel speaker systems and Karaoke processors; primarily video applications like SDTV and HDTV stereo television receivers, digital cable and satellite TV set-top boxes; and multimedia applications with both audio and video like Multimedia PCs and the Digital Video Disk (DVD) players.

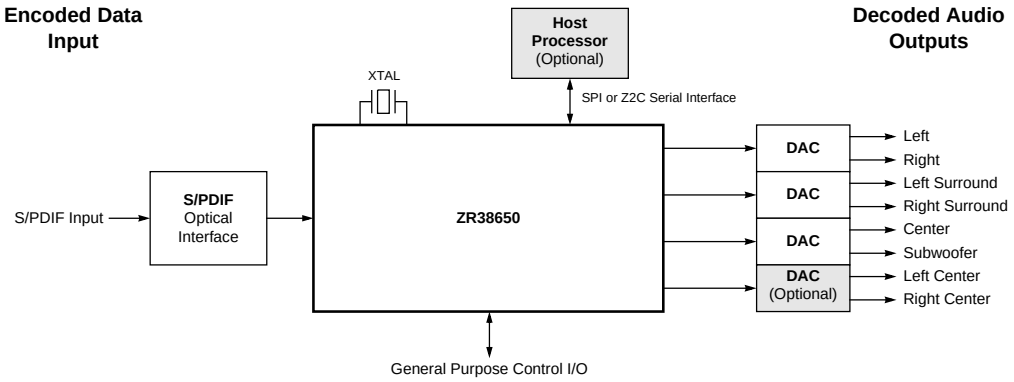


Figure 1. A Typical Low-Parts-Count ZR38650 System

GENERAL DESCRIPTION

The Zoran ZR38650 is the latest full-function digital audio processing member of the ZR38000 digital signal processor product line. It is especially configured with peripherals, I/O capability and software for digital audio. Today, quality digital audio starts with a primary decoding function and adds appropriate data stream protocols and interfaces with I/O configurations to match the application. The ZR38650 has these primary decode and protocol software functions and yet has program/data memory and processing cycles left for additional product-distinguishing features. The ZR38650 also has the necessary flexibility in system I/O and hardware configuration.

The ZR38650 is instruction-set compatible with the earlier ZR38600, but has a higher 50-MIPS processing rate. This gives the new faster 96-kHz sample rate S/PDIF decoding and increased processing cycles for additional functions. Larger internal program and data RAMs and ROM along with wide external memories accommodate today's rapidly changing needs for large complex algorithms. Other new hardware features are a programmable timer, a Z2C serial host interface and more support for the 24-bit I/O data formats.

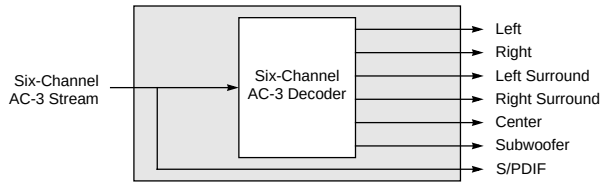
Functions

AC-3 and MPEG with variations are the primary decoding functions in use today. The ZR38650 has these and their associated test function with the required set-up, operation and system functions to make them usable in an end-user product. In addition, an ever increasing number of *SiliconSoftware* functions can add special enhancing and differentiating features to products.

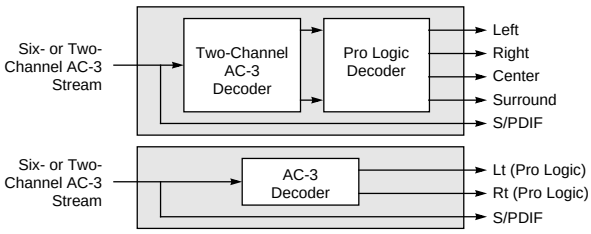
Primary Decoding and Test Functions

AC-3

The figure shows the simultaneous S/PDIF input and 5.1 channel DAC (Digital-to-Analog Converter) outputs of this primary digital audio function, the six-channel AC-3 decoder.

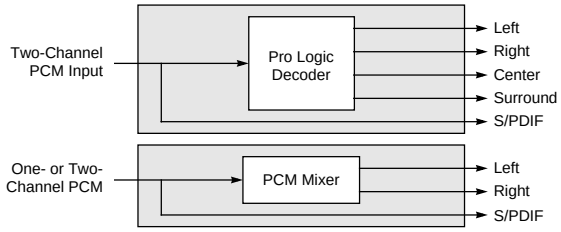


Or with four channels of Pro Logic output in either of two DAC forms: four channels directly or to an analog Pro Logic decoder.



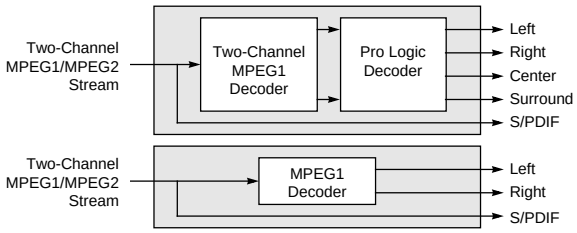
PCM + Pro Logic

With two-channel PCM inputs the choice of functions is four-channel Pro Logic decoding or two-channel stereo mixing, including upmixing from only one input channel to two.



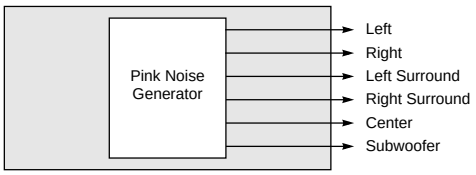
MPEG

The MPEG1 decoder accepts either MPEG1 or MPEG2 input streams and produces either Pro Logic DAC outputs or two-channel stereo in DAC form.



Pink Noise

A six-channel pink pseudo-random noise generator function is included for user testing of speaker balance in their listening space. Individual speakers can be enabled in any combination.



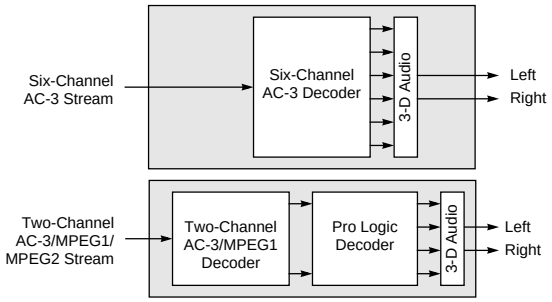
SiliconSoftware™ Functions

SiliconSoftware is a group of additional functions for the ZR38650 provided by Zoran or third-party suppliers that can add special features now or provide new functions in the future.

3-D Audio

Currently there are six providers of 3-D audio which gives the effect of a three-dimensional sound field with only two speakers. These functions are Aureal A3D, Dolby Virtual Surround, Harman VMAx, QSound QSurround™, Spatializer N-2-2™ and

SRS TruSurround. They work with either two- or six-channel inputs and the AC-3 or MPEG decoders.



Bass Management

Selected low-frequencies can be redirected to different speakers with Bass Management. Useful with all types of decoding to compensate for the types of speakers used.

DVD - Linear PCM

Special provisions are included for data formats and synchronization for AC-3/MPEG decoding with 3-D audio and bass management for Digital Video Disk (DVD) applications.

Hall Effects/Music Modes

Adds the natural acoustical effects of a performance environment to the original recording environment.

Home THX5.1

Theater THX for use in consumer home entertainment systems.

Karaoke Processing

Voice cancellation, pitch-shifting and echo and reverberation.

Custom Functions, Etc.

Product designers can always add custom functions and variations, often with very simple software additions.

Operation and Set-Up Functions

These control the simple start and stop operation of the decoding functions and determine the initial hardware operation and configuration.

System Functions

These functions control the real-time operation including interface transactions, program loading and in-circuit testing.

System Configurations

The ZR38650 is highly self-contained and can work with few external parts as shown in Figure 1. However it is very flexible in accommodating the needs of larger, higher performance systems. Figure 2 shows all of the possible options that are supported to make a complete system.

Hosts

The ZR38650 does not require a host microprocessor but if there is one in the system it may be used to advantage. Either the bit-serial SPI (Small Peripheral Interface) or Z2C interface, or a byte-wide parallel interface may be used.

Data Input/Output

The encoded digital input data stream can use a bit-serial or byte-parallel interface or S/PDIF receiver with the ZR38650 either a master or slave. Up to six-channels of analog signals can be input in bit-serial ADC (Analog-to-Digital Converter) formats in a master or slave mode.

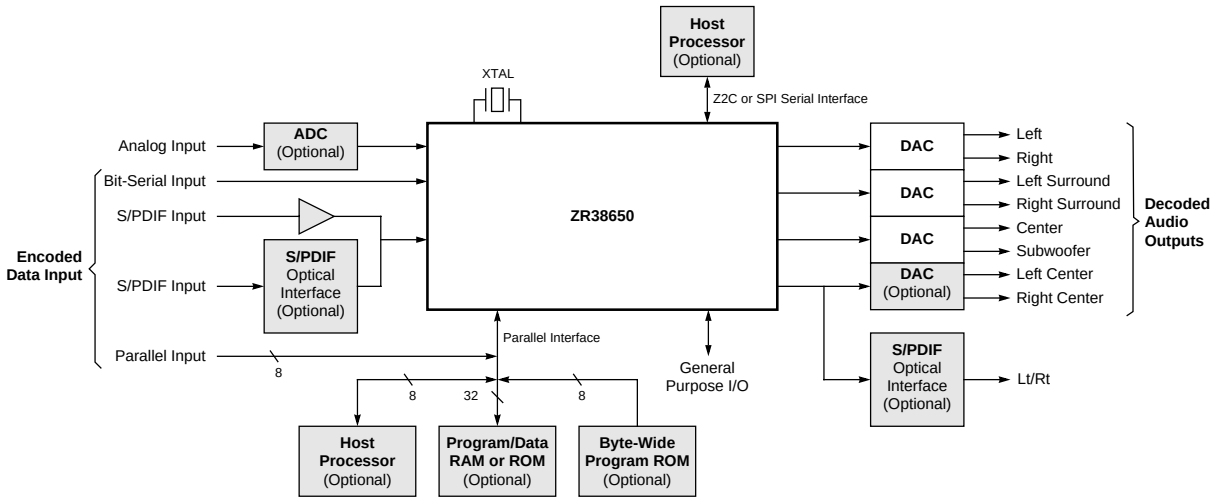


Figure 2. ZR38650 Composite System Block Diagram

Decoded audio outputs can be up to eight channels in bit-serial DAC formats or six encoded channels from the S/PDIF transmitter.

Memory

External memory is not normally needed but can be added for program and/or digital audio data. Additional byte-wide program storage gives different or additional functions when a host is not used and allows a choice of ROM technologies to be employed for future upgradability at minimum cost and parts count. Wider 32-bit program storage allows directly executing large functions without downloading. External data memory may be required for functions with long acoustical delays, input buffering or large data tables.

FUNCTIONAL DESCRIPTION

A more complete description of the ZR38650 software's operation and configurations and its hardware configurations follows.

Software - Operation

One of the major benefits of the ZR38650 is its ease of use for the system developer under a broad range of system requirements. Standard functions are easy to use, yet custom features can be added without falling back to custom software development with complicated real-time operating system considerations or detailed I/O protocols. This follows from the fact that all software functions are supplied with a common command and response sequence for use with a host or an API (Application Programming Interface) for calling from an internal program. And each provides for adding custom functions in not just one but a series of ways which depend upon the complexity of the custom function.

This is shown schematically in Figure 3 where the operation, set-up, primary, and *SiliconSoftware* functions are shown in the middle. Using the system utilities to maintain the communications with the host, the host can issue a sequence of commands with responses to control the ZR38650's operation. The utilities issue API calls to the functions. All of the software development can be limited to the host microprocessor even when feature types of variations in operation are based on getting information back from the ZR38650's operation.

Alternatively, the control information in the commands can be entered in a sequence of API calls issued from a custom program running internally on the ZR38650 processor. Now no host is required.

With either a host command/response stream or API calls, custom functions in native ZR38001 code can be added without losing the benefits of the ease of use in the common structure.

Table 1 is a summary of the commands and responses for the standard primary, operation and set-up functions. Note there are read and write commands to the ZR38650 and responses back from the ZR38650 to the host. Responses are due to commands during normal operations that are in progress or from certain specific commands with read commands following.

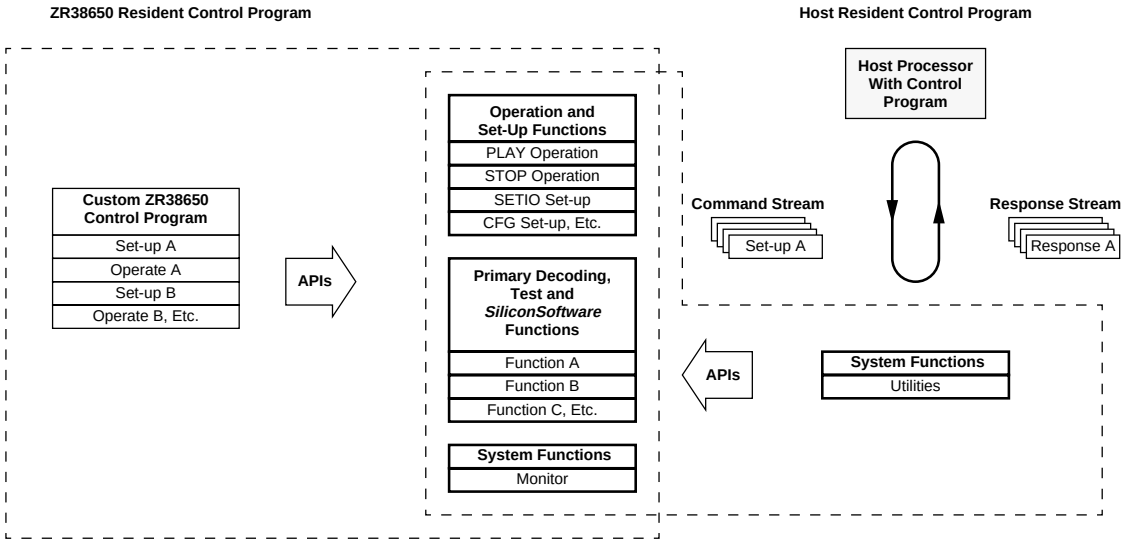


Figure 3. ZR38650 Operation Control: Commands from a Host or Calls from a ZR38650 Resident Program

Table 1: Standard Function Command and Response Summary

Class	Name	Description
Write Command		Commands to ZR38650 to perform a specific function
Primary Decoding And Test Functions	AC3	Select AC-3 or AC-3 + Pro Logic decoder function
	PCMPROL	Select PCM or Pro Logic decoder functions with PCM input and mixer function
	MPEG	Select MPEG or MPEG + Pro Logic decoder function
	PNG	Select pink noise generator function
	USER	Select user defined function
Operation Functions	PLAY	Resume selected function operation and unmute audio output
	MUTE	Mute audio output without stopping the selected operation
	UNMUTE	Restore muted audio output while continuing the selected operation
	STOP	Stop operation, retain data in input buffer and mute audio output
	STOPF	Stop operation, flush the data in the input buffer and mute audio output
	STAT	Return decoder status information using the READ command
	SPDIFSTAT	Return the S/PDIF input channel status
	GETPTC	Return the PTC and STC values for timing synchronization
	NOP	Not a command, does not affect operation. Will return a Progress response.
Set-Up Functions	PLLTAB	Set the PLL programmable registers
	PLLCFG	Define the PLL configuration
	CFG	Configure the ZR38650 I/O to the specific system hardware
	SETSTC	Set the system time clock and video delay
	VER	Return 32-bit ROM version number using the READ command
	BOOT	Load and execute the N parameter words of bootstrap program
	SPDIFCS	Write the S/PDIF output channel status
	PARAM	Define parameters for special functions
	INTRP	Interpret: load and execute four parameter words as a ZR38001 instruction
	SETIO	Set, test and return general purpose single-bit I/O registers
	POKE	Load N 32-bit words to the core processor RAM at the given start address
	PEEK	Read N 32-bit words from core processor RAM at the given start address
Read Command		Commands to ZR38650 to return Reply words to the host
	READ	Command to ZR38650 to return a Reply word after specific commands
Reply Response		Data words returned to the host as the result of sending specific commands followed by READ commands
	AC3STATR	Status and information about the AC-3 stream
	PCMPROLR	Status and information about the PCM or Pro Logic stream
	MPEGSTATR	Status and information about the MPEG stream
	PNGSTATR	Status and information about the PNG stream
	VERR	Four byte version number of ROM read by VER command
	SETIOR	Two words of GPIOC and GPIO registers
	PLLR	Two bits which indicate the PLL lock status
	PEEKR	N 32-bit words from core processor RAM specified by PEEK command
	SPDIFSTATR	S/PDIF input channel status
	GETPTCR	PTC and STC values of 32 bits each
Progress Response		Data words returned to host in the normal process of sending any command
	EXPECT	Expected number of parameter words still to be received from host
	ISTATUS	Interpreter status

Software - Functions

Primary Decoding and Test Functions

AC-3

The major modes of operation of the Dolby Digital AC-3 decoder function are summarized in Table 2. Choices are for input and output ports and their formats including operation with audio/video synchronization (AVS), constant or request driven PES packetized inputs and the linear PCM of DVD.

AC-3 input decoding rates are up to 640 kbits per second. Full selection can be made for speaker configuration, dynamic range compression, downmixing, delays, filtering and error concealment strategy. The Karaoke downmixing is also supported including with downloaded Karaoke coefficients.

PCM + Pro Logic

With two-channel PCM inputs, the choice of functions is four-channel Pro Logic decoding or two-channel stereo mixing. Selection can be made for speaker configuration, downmixing, delays and surround filtering.

MPEG

The MPEG1 decoder function accepts either MPEG1 or MPEG2 input streams and produces either Pro Logic or two-channel stereo outputs in DAC form. Selection can be made for speaker configuration, dynamic range compression, downmixing, delays and surround filtering.

Pink Noise

This is a six-channel pink (equal energy per constant proportional bandwidth) pseudo-random noise generator test function. It is for user testing of speaker balance in a listening space. The six individual speakers can be enabled in any combination at a single adjustable level, with or without a band-limiting filter.

SiliconSoftware™ Functions

3-D Audio

There are six third-party providers of 3-D audio using the ZR38650. This function gives the effect of a three-dimensional sound field with only two speakers. These certified functions are Aureal A3D, Dolby Virtual Surround, Harman VMAx, QSound QSurround™, Spatializer N-2-2™ and SRS TruSurround. They work with either two- or six-channel inputs and the AC-3, MPEG and Pro Logic decoders as shown in Table 3.

Bass Management

Depending upon the speakers used in a listening area, it can be desirable to alter the distribution of the bass frequencies between speakers. A choice of speaker configurations is provided and of low-pass cut-off frequencies for 80, 100 or 120 Hertz in the simplest form. The full function allows the low-pass and high-pass filter coefficients to be downloaded along with individual speaker sound levels.

Bass management works with either two- or six-channel inputs and the AC-3, MPEG and Pro Logic decoders. It does not work with 3-D audio although some 3-D audio functions include certain bass management features.

DVD - Linear PCM

In addition to the audio/video synchronization (AVS) and request driven PES packetized input features of the standard decode functions, this DVD function has 3-D audio capability and bass management. It works with two-, six- or eight-channel PCM inputs and the AC-3, MPEG and Pro Logic decoders.

Table 2: Primary Decoding and Test Function Options Summary

Primary Decoding Or Test Function	Input					Output		
	Data Stream	Serial Port A, S/PDIF, Parallel	AVS	MPEG2 PES Packetized	DVD PES Packetized	Function	Serial DAC Ports	S/PDIF Port G
AC3	6-Channel AC-3	SA, S/P, P	Yes	Yes	Yes	6-Channel AC-3	B,C,D	Input Stream
						2-Channel Pro Logic encoded	B	
	2-Channel AC-3	SA, S/P, P	Yes	Yes	Yes	4-Channel Pro Logic	B,C,D	
						2-Channel AC-3	B	
PCM + Pro Logic	2-Channel PCM	SA, S/P, P	No	No	No	4-Channel Pro Logic	B,C,D	Input Stream
						2-Channel PCM Mixed	B	
MPEG	MPEG1	SA, S/P, P	Yes	Yes	Yes	4-Channel Pro Logic	B,C,D	Input Stream
						2-Channel MPEG1	B	
	MPEG2	SA, S/P, P	Yes	Yes	Yes	4-Channel Pro Logic	B,C,D	
						2-Channel MPEG1	B	
PNG	-	-	-	-	-	6-Channel Pink Noise	B,C,D	-

Hall Effects/Music Modes

Short and long term delays and reverberation are added to multichannel PCM inputs with this function. Delay coefficients are downloaded to simulate various acoustical environments (concert halls, churches, stadiums, etc.)

Home THX5.1

This function, when used in a two-chip set connected in cascade, provides the sound of the Lucasfilm theater THX in the home listening environment. The input chips runs all of the standard decoding functions and passes its PCM outputs to the second chip for the THX5.1 processing which included full bass management, decorrelation, timbre matching and re-equalization and individually programmable channel delays.

Karaoke Processing

In addition to the Karaoke input mixing features of the standard decode functions, this is true Karaoke processing with voice cancellation, pitch shifting, voice echo and reverberation and bass management. External data memory may be required for this function.

Custom Functions, Etc.

The User function allows developers to easily add custom functions using their own native ZR38001 code, yet retain the ease of control of the command and response structure of the ZR38650.

Operation and Set-Up Functions

The operation functions, summarized in Table 1, are the real-time start and stop commands needed for system control once the primary decoding function has been selected. Also included are commands to get the input channel and decoding status to monitor on-going operation. The PTC and STC time clocks can also be monitored to insure audio and video synchronization.

The set-up functions configure both the hardware and software before operation starts or as major operational changes are made. Hardware configuration and initialization includes the phase-locked loops (PLLs), system clocks and the input/output (I/O). Software can be put in place through the host processor from its I/O or memory system. It may be in the form of custom commands and their parameters or directly executable native code for the core DSP processor.

Table 3: *SiliconSoftware* Function Options Summary

***SiliconSoftware* Function**		**Input**		**Output**		
		Serial Port A, E or F, S/PDIF, Parallel	**Standard Function Source**	**Function**	**Serial DAC Ports**	**S/PDIF Port G**
3-D Audio:	Aureal A3D	SA, S/P, P	AC-3, AC-3 + Pro Logic, PCM + Pro Logic, MPEG, MPEG + Pro Logic	2-Channel 3-D Audio	B	Input Stream
	Dolby Virtual Surround					
	Harman VMAx					
	QSound QSurround™					
	Spatializer N-2-2™					
	SRS TruSurround					
Bass Management		SA, S/P, P	All of the above	Redirect low frequencies to different speakers	B, C, D	Input Stream
DVD		SA, P	All of the above + 8-Channel PCM	Decoding, 3-D and bass management	B, C, D, G	Input Stream Unless 8-Ch. PCM
Hall Effects/Music Modes		SA, S/P, P	PCM	Add room effects	B, C, D	Input Stream
Home THX5.1	Decoding Chip	SA, S/P, P	AC-3, AC-3+Pro Logic, PCM+Pro Logic, MPEG, MPEG + Pro Logic	Two chip set decodes and produces THX outputs	B, C, D	Input Stream
	THX Processing Chip	SA, SE, SF			B, C, D	-
Karaoke Processing		S/P & SF or SA & SF	AC-3, PCM, MPEG	Voice cancellation, pitch shifting, echo and reverberation and bass management.	B, C, D	Input Stream

System Functions

The remaining portion of the standard ZR38650 functions that reside in every program ROM are the system functions, shown schematically in Figure 4.

Monitor

This is the simple real-time operating system mini-kernel used by all ZR38650 functions in normal operation.

Utilities

System utilities maintain operation of the various I/O interfaces that are shared between functions. These include the serial audio data ports, the serial SPI or Z2C host interface and the parallel host interface for commands and responses. The utilities also include the initial and reset bootstrap routine that determines the start-up ROM and executes its initialization process.

ICE Debug

For In-Circuit Emulation debugging using the ZR38000 Family Simulator, the monitor is used in a mode for single-step and breakpoint execution of programs.

Software - System Configurations

As a result of the ZR38650's ability to be configured from a low-cost, fixed-function device to a very flexible, full capability audio processor, there are many choices as to how the software is configured. These are related to the system hardware configuration. Important considerations are if a host is used, if only standard commands are to be used and what provisions are to be made for current and future upgrades. Table 4 summarizes the most common configurations and their relative benefits.

Figure 4 illustrates possible sources and residences of the software for different hardware configurations. Starting with the on-chip program ROM, it can be either the standard version or with custom functions as shown. Custom and *SiliconSoftware* functions can be available for downloading into the on-chip or external program/data RAM from three sources as indicated by the dashed arrows. If there is no host they must be loaded from the external byte-wide program ROM or executed directly from an external 32-bit ROM. With a host custom and *SiliconSoftware* functions may be loaded from the host's own non-volatile memory (ROM or flash EPROM typically) or through its I/O peripherals such as on-line links or movable memory media like floppy disks.

Hardware - System Configurations

All of the hardware shown in Figure 2, the composite system block diagram on page 3, is supported in the ZR38650. The choices for host, data input and output, and external memory are summarized in Table 5. Those that are supported by the standard functions with the standard commands are noted. Individual *SiliconSoftware* functions support additional configurations. For example, the Karaoke Processing supports the bit-serial ADC data input and the external data RAM required for pitch correction and voice reverberation.

Table 4: Software Configurations

Configuration		Description	Benefits
Host Operation Using Standard Commands	Internal Standard ROM with or without External RAM	Download internal/external program RAMs with *SiliconSoftware* from host for additional current and future functions.	Moderate flexibility for current and future functions with only host S/W development.
Host Operation Using Standard and Custom Commands and APIs	Internal Standard ROM with or without External RAM	Download internal/external program RAMs with *SiliconSoftware* from host for additional current, future and custom functions.	Maximum customization and flexibility for current and future functions.
	Internal Standard ROM with External Custom ROM	Download internal program RAM with *SiliconSoftware* from external ROM for current and custom functions or from host for future functions.	Maximum customization with moderate flexibility for current and future functions. Lower external memory size and costs.
	Internal Custom ROM	Download program RAM with *SiliconSoftware* from host for future functions.	Moderate customization with moderate flexibility for future functions. Minimum cost.
Stand Alone (No Host) Operation Using Standard and Custom Functions with APIs	Internal Standard ROM with External Custom ROM	Standard and custom functions with control through GPIO port.	Low cost, maximum customization. Broad choice of ROM technologies for flexibility for future.
	Internal Custom ROM	Standard and custom functions with control through GPIO port. No future flexibility without internal ROM non-recurring engineering (NRE) cost.	Lowest recurring cost with moderate customization.

Hosts

A host microprocessor is not required for the ZR38650's operation. A custom program, in either the internal ROM or an external ROM with the standard internal ROM, is sufficient. Control of the operation is then through the GPIO (General Purpose Input/Output) ports.

However, the greatest flexibility is available if a host is used. The least costly in external hardware is a serial host interface. The four-wire SPI (Small Peripheral Interface) or two-wire Z2C signals (see Table 6) connect directly to most low-cost microcontrollers. There is no speed penalty with a host serial interface and it leaves the parallel interface free for use with external memories.

The ZR38650's parallel interface can be used for a byte-wide connection to a microprocessor host along with byte-wide I/O with the standard command support. The full 32-bits of the parallel interface can be used for an I/O connection if called in the developer's software. Note that the parallel interface can not be used concurrently for the host and I/O while it is being used for external data or program memory.

Data Input/Output

The primary data input is the single-wire digital audio interface receiver. This conforms fully to S/PDIF, IEC-958, AES/EBU and EIAJ CP-340 consumer standards. All standard sampling rates are supported for raw or packetized bitstreams as well as the data driven master operation using the $\overline{\text{DREQ}}$ signal on the GPIO0 port. Serial port A or the byte-wide parallel interface may alternately be used for the channel bitstream as master or slave. The parallel interface also provides data driven master operation, but it can not be used concurrently with external memory in the system.

Up to six channels of bit-serial ADC data can be input as master or slave in a wide variety of industry formats when required by *SiliconSoftware* functions.

Up to eight channels of bit-serial DAC data can be output as master or slave in the same variety of industry formats including I^2S and EIAJ with word, frame and frameless synchronization. Ports B,C and D are used by standard 6-channel functions with Port G in addition for 8-channel *SiliconSoftware* functions. Otherwise Port G serves as a S/PDIF master transmitter.

External Memory

The 20 address and 32 data lines of the parallel port allow a wide choice of external memory for program and data storage if needed for *SiliconSoftware* functions or for future flexibility. Variable wait-states are supported for slower, lower cost memories. Not used concurrently with parallel host or I/O interfaces.

Hardware - Digital Audio Processor

The ZR38650 is composed of the interfaces, memories and system clocks that surround the ZR38001 DSP core shown in Figure 5. The individual signals of each of the interfaces and power supply connection are summarized in Table 6.

The figure illustrates the sharing of the serial output port G with the S/PDIF transmitter and the multiple functions of the parallel port for the external host, I/O and memories. Note from Table 6 how some of the otherwise unused 32-bit memory data lines are utilized for additional control when the parallel byte-wide interface is employed for the external host and I/O.

Using standard functions, three of the six GPIO signals are dedicated as a $\overline{\text{MUTE}}$ input, an I/O data request output, $\overline{\text{DREQ}}$, and an I/O error output, ERROR.

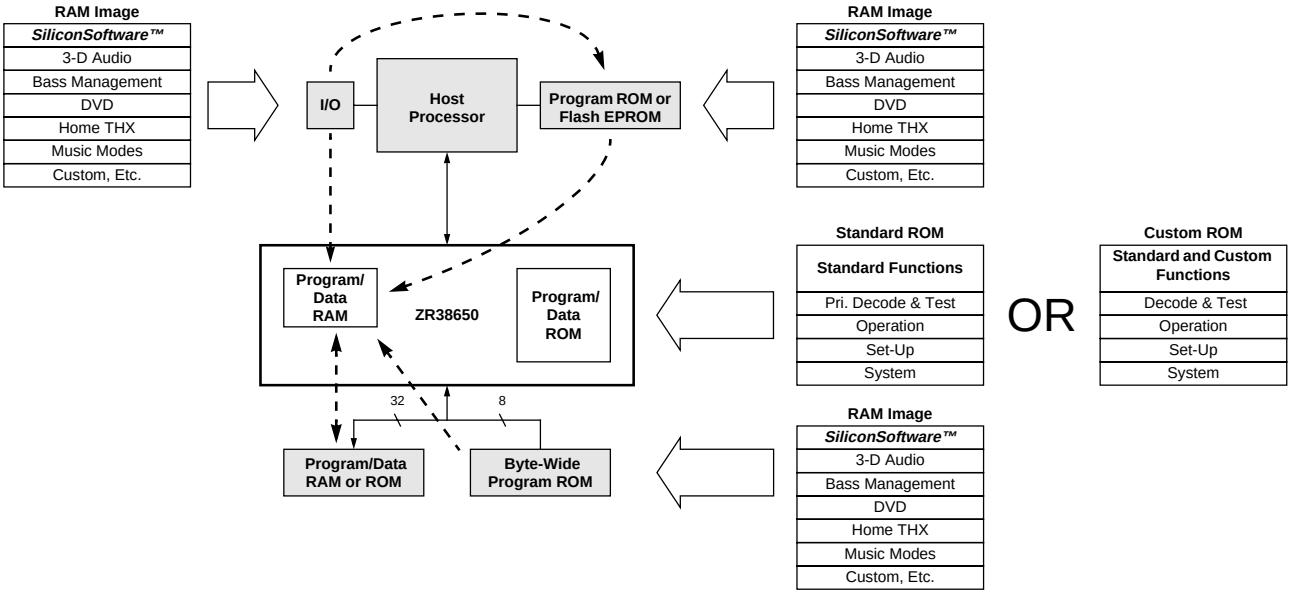


Figure 4. Software Memory Configurations

Table 5: System Hardware Configurations and Standard Command Support

Hardware Configuration		Hardware Configuration Description	Standard Command Support
Host	None	Custom program using parallel and/or GPIO interface for control.	None. Requires custom internal or external program ROM.
	Bit-serial Interface	Industry standard four-wire SPI duplex or two-wire Z2C half-duplex.	Yes.
	Parallel Interface	Byte-wide selectable for I/O and Commands. Not possible concurrent with external memory.	Yes.
Data Input	S/PDIF Channel	Standard single-wire receiver.	Yes.
	Bit-serial Channel	Serial Port A is a flexible slave or data driven master with $\overline{\text{DREQ}}$.	Yes.
	Parallel Channel	Byte-wide master, slave or data-driven master with $\overline{\text{DREQ}}$. Not possible concurrent with external memory.	Yes.
	ADC bit-serial	Up to six channels as a flexible master or slave.	No.
Data Output	DAC bit-serial	Up to eight channels on Ports B, C, D and G as flexible master or slave.	Yes for 6-channel ports B, C and D.
	S/PDIF Channel	Standard single-wire transmitter on Port G. Master only.	Yes, Port G.
External Memory	Program/Data ROM	8-, 16- or 32-bit for loading or 32-bit for execution.	Yes for execution or 8-bit only loading.
	Program/Data RAM	32-bit memory for executing large functions or 16 or 32 bits for large delay or table memory.	Not required for standard functions.

Internal memories are large: the 20-kwords of 32-bit program/data ROM is augmented with an addition 2-kwords of down-loadable RAM. The data only memory is a 10-kword RAM in the 20-bit data word precision.

The two programmable phase-locked-loops (PLLs), one for the DSP core (f_{DSP}) and one for the audio serial ports (f_{AUDIO}) allow independent selection of these two critical internal clock rates. This is particularly important when the ZR38650 system oscillator is not determined by its own external crystal, but rather from a predetermined system clock frequency. Having two PLLs lets the DSP core synchronously operate at its maximum 50 MIPS rate (f_{DSP} = 100 MHz) for processing while the serial I/O operates at the standard sample rates of 32, 44.1, 48 or 96 kHz, regardless of whether the predetermined system clock frequency is a common sub-multiple.

The power supply is 3.3 Volts for lower power consumption, yet all I/O signals are 5.0 Volt tolerant for use in 5.0-Volt systems.

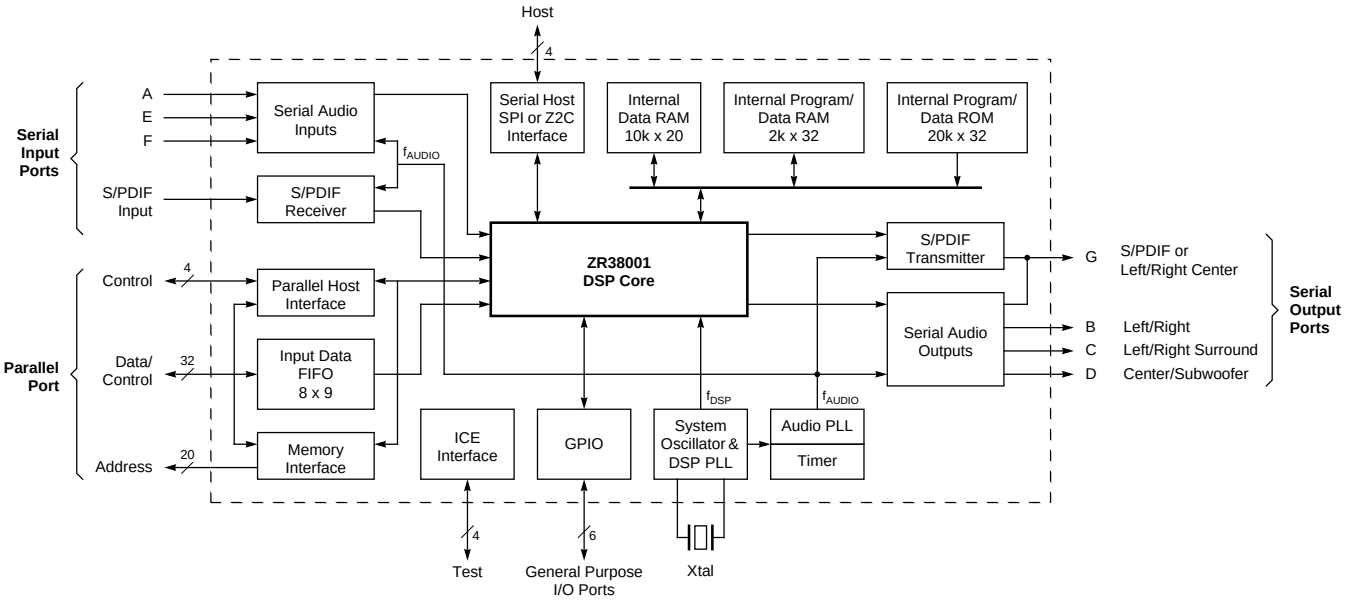


Figure 5. ZR38650 Simplified Block Diagram

Table 6: ZR38650 Signal Description Summary

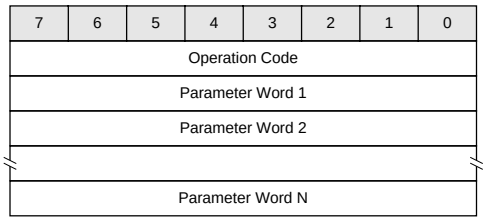
Name	Number	Type [1]	Description
Parallel Port (56)			
A[19:0]	20	O	Address bus of parallel port
D[31:15]	17	I/O	Data bus of parallel port when selected for external memory (P/$\overline{M}$ = 0)
D14/RDY	1	I/O or O	Data bus (P/$\overline{M}$ = 0) or Ready output signal of parallel port when selected for parallel I/O (P/$\overline{M}$ = 1)
D13/ C/$\overline{D}$	1	I/O or I	Data bus (P/$\overline{M}$ = 0) or Command/Data select input of parallel port when selected for parallel I/O (P/$\overline{M}$ = 1)
D12/ERR	1	I/O or I	Data bus (P/$\overline{M}$ = 0) or Error input signal of parallel port when selected for parallel I/O (P/$\overline{M}$ = 1)
D[11:4]/PP[7:0]	8	I/O	Data bus of parallel port when selected for external memory (P/$\overline{M}$ = 0) or Parallel Port I/O (P/$\overline{M}$ = 1)
D[3:0]	4	I/O	Data bus of parallel port when selected for external memory (P/$\overline{M}$ = 0)
$\overline{CS}$	1	I/O	Chip Select output for external memory or Chip Select input for parallel I/O
$\overline{RD}$	1	I/O	Read enable output for external memory or Read enable input for parallel I/O
$\overline{WR}$	1	I/O	Write enable output for external memory or Write enable input for parallel I/O
P/$\overline{M}$	1	I	Parallel I/O or Memory select for parallel port. Determined at time of $\overline{RESET}$.
Serial Ports (13)			
SPFRX	1	I	S/PDIF Receiver input port
SDA, SDE, SDF	3	I	Serial Data inputs. Ports A, E and F.
WSA/FSA	1	I/O	Word Select or Frame Synchronization for input ports. An output when a master, an input when a slave.
SCKA	1	I/O	Serial Clock for input ports. An output when a master, an input when a slave.
SDB	1	O	Serial left and right Data output. Port B. Also, at $\overline{RESET}$ defines SPI/$\overline{Z2C}$ for host serial interface.
SDC	1	O	Serial left and right surround Data output. Port C. Also, at $\overline{RESET}$ defines $\overline{Z2CADR[0]}$ of Z2C address.
SDD	1	O	Serial center and sub-woofer Data output. Port D. Also, at $\overline{RESET}$ defines $\overline{Z2CADR[1]}$ of Z2C address.
SDG/SPFTX	1	O	Serial Data output. Port G or S/PDIF Transmitter port. Also, at $\overline{RESET}$ defines the SCKP value.
WSB/FSB	1	I/O	Word Select or Frame Synchronization for output ports. An output when a master, an input when a slave.
SCKB	1	I/O	Serial Clock for output ports. An output when a master, an input when a slave.
SCKIN	1	I/O	Serial master Clock output or master clock Input for output ports
General Purpose Ports (6)			
$\overline{MUTE}$/GPIO5	1	I or I/O	Mute input signal or can be programmed as General Purpose Input/Output 5
GPIO[4:2]	3	I/O	Can be programmed as General Purpose Input/Output 4, 3 and 2
ERROR/GPIO1	1	O or I/O	Error output signal or can be programmed as General Purpose Input/Output 1
$\overline{DREQ}$/GPIO0	1	O or I/O	Data Request output signal or can be programmed as General Purpose Input/Output 0
Serial Host Interface (4)			
SI	1	I	Host Serial interface data Input. Also, at $\overline{RESET}$ defines Z2CADR[5] of Z2C address.
SO/SDA	1	I/O/T	SPI host Serial interface data Output or Serial Data for Z2C
SCK/SCL	1	I	SPI host Serial interface Clock input or Slave Clock input for Z2C
$\overline{SS}$	1	I	SPI host serial interface Slave Select input. Also, at $\overline{RESET}$ defines Z2CADR[4] of Z2C address.
ICE Interface (4)			
TDI, TCK, TMS	3	I	ICE Test interface Data Input, Clock input and Mode Select
TDO	1	O/T	ICE Test interface Data Output
System Interface (8)			
$\overline{INT}$	1	I	External Interrupt request input
$\overline{RESET}$	1	I	Reset input to start operation in known state
MMAP	1	I	Determines location on Memory Map of reset and interrupt block
XTI	1	I	External system clock Input or connection to external crystal, at frequency f_{XTI}
XTO	1	O	Output connection to external crystal
CLKOUT	1	O	Clock Output from the ZR38650 at frequency $f_{DSP}/2$
BYPASS	1	I	Bypass internal DSP core PLL to use external system clock input on XTI
FLTCAP	1	I	External Filter Capacitor connection for PLL. A value of 47nF is recommended.
Power (43)			
VDD	16	Power	+3.3 volt power supply
VDDA	1	Power	+3.3 volt power supply, Analog for PLL
GND	25	Power	Power supply Ground
GNDA	1	Power	Power supply Ground, Analog for PLL
Total (144) = Active (134) + No Connection (10)			

1. O = Output, I = Input, T = Tri-state in normal use. May be different at Reset time as shown in Table 23 on page 42.

STANDARD FUNCTIONS DESCRIPTION

The ZR38650 standard functions are selected and controlled by the commands and responses shown in Tables 7 and 8. These are the commands, parameters and responses sent and received by a microprocessor over the serial host interface or the parallel host interface when a parallel host is used. The Applications Program Interfaces (APIs) for the AC-3, Pro Logic, Pink Noise, etc. functions are similar. These APIs are used by a developers program executing on the core processor.

Transfers between a host and the ZR38650 with the SPI are full-duplex with the host being the master. For every command sent a word is received back from the ZR38650. Transfers with the parallel host interface or the serial Z2C interface are half-duplex with the host master. Then the host must initiate the read for the response after each command is sent. The commands are sent only from the host and are in the general form shown.

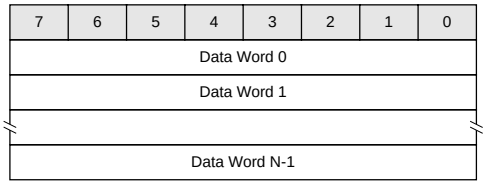


There are two classes of commands: those that Write to the decoder and those that Read back from the decoder. The Write commands may have parameter words in addition to the basic operation code. The Write commands are of three types as shown in Table 7: those that choose primary decoding and test functions (e.g., AC3), those that govern operation (e.g., STOP or PLAY) and those that set-up operation (e.g., CFG).

Table 7: Standard Function Command Summary (Host to ZR38650 Transfers)

Class	Name	Operation code (Hex)	Number of parameter words	Description
Write Command				Commands to ZR38650 to perform a specific function or operation
Primary Decoding And Test Functions	AC3	85	8	Select AC-3 and Pro Logic decoder function, either six- or two-channel output
	PCMPROL	86	8	Select PCM or Pro Logic decoder functions with PCM input and mixer function
	MPEG	87	8	Select MPEG or MPEG + Pro Logic decoder function
	PNG	83	8	Select pink noise generator function
	USER	88	8	Select user defined function
Operation Functions	PLAY	8A	0	Resume selected function operation and unmute audio output
	MUTE	8B	0	Mute audio output without stopping the selected operation
	UNMUTE	89	0	Restore muted audio output while continuing the selected operation
	STOP	8C	0	Stop operation, retain data in input buffer and mute audio output
	STOPF	8D	0	Stop operation, flush the data in the input buffer and mute audio output
	STAT	8E	0	Return decoder status information using the READ command
	SPDIFSTAT	8F	0	Return the S/PDIF input channel status
	GETPTC	9A	0	Return the PTC and STC values
	NOP	80	0	Not a command, does not affect operation. Will return a Progress response.
Set-Up Functions	PLLTAB	98	6	Set the PLL programmable registers
	PLLCFG	99	1	Define the PLL configuration
	CFG	82	8	Configure the ZR38650 I/O to the specific system hardware
	SETSTC	97	7	Set the system time clock and video delay
	VER	81	0	Return 32-bit ROM version number using the READ command
	BOOT	90	N	Load and execute the N parameter words of bootstrap program
	SPDIFCS	95	4	Write the S/PDIF output channel status
	PARAM	96	N	Define parameters for special functions
	INTRP	91	4	Interpret: load and execute four parameter words as a ZR38001 instruction
	SETIO	92	4	Set, test and return general purpose single-bit I/O registers
	POKE	93	7+4N	Load N 32-bit words to the core processor RAM at the given start address
	PEEK	94	7	Read N 32-bit words from core processor RAM at the given start address
Read Command				Commands to ZR38650 to return Reply words to the host
	READ	00	0	Command to ZR38650 to return a Reply word after specific commands

The words received back from the ZR38650 when the host initiates a transfer will be of the form:



The responses are of two types, a Reply to READ commands following specific Write commands or the Progress responses to each Write command. The Progress response is always the number of still expected parameters (EXPECT) and/or READs, followed by the response and interpreter status (ISTATUS).

All responses to commands sent on the SPI are delayed by two words as shown in the example of the SETIO command which has both parameter words (Para 1-4) and two Reply data words (SETIOR). Note that the initial ISTATUSes returned are a response to previous READs sent by the host. There are no delays on the parallel host interface or the serial Z2C interface in the normal alternating single-byte transmit/receive protocol.

Words sent from Host Time →

1	2	3	4	5	6	7	8	9	10
SETIO	Para1	Para2	Para3	Para4	READ	READ	READ	READ	READ

Words sent from ZR38650

		1	2	3	4	5	6	7	8
ISTATUS	ISTATUS	Exp1=5	Exp2=4	Exp3=3	Exp4=2	Exp5=1	SETIOR1	SETIOR2	ISTATUS

The second example below shows the response to the VER command. The EXPECT value tells the host how many bytes of information are returned by the command.

Words sent from Host Time →

1	2	3	4	5	6	7	8
VER	READ	READ	READ	READ	READ	READ	READ

Words sent from ZR38650

		1	2	3	4	5	6
ISTATUS	ISTATUS	EXPECT=4	A1	20	10	02	ISTATUS

See Table 9 on page 23 for a summary of the sequence of commands, parameters, reads, responses and status.

The following descriptions explain the ZR38650's standard functions as well as the specifics of the commands used and their responses. They are in the same order as Tables 7 and 8.

Note that the descriptions on the following pages are meant to be inclusive of all functions that are currently available on the ZR38650. Some functions require that additional code be downloaded into program RAM. Likewise, note that command parameter tables are all inclusive.

Individual program and ROM release documents should be consulted to determine the exact functionality for the ROM version and program release that is being used.

Table 8: Standard Function Response Summary (ZR38650 to Host Transfers)

Class	Name	Response operation code (Hex)	Number of data words	Description
Reply Response				Data words returned to the host as the result of sending specific commands followed by READ commands
Primary Decoding And Test Functions	AC3STATR	05	16	Status and information about the AC-3 stream
	PCMPROLR	04/06	8	Status and information about the PCM or Pro Logic stream
	MPEGSTATR	07	12	Status and information about the MPEG stream
	PNGSTATR	03	8	Status and information about the PNG stream
Set-Up Functions	VERR	-	4	Four byte version number of ROM read by VER command
	SETIOR	-	2	Two words of GPIOC and GPIO registers
	PLLR	-	1	Two bits which indicate the PLL lock status after a PLLCFG command
	PEEKR	-	4N	N 32-bit words from core processor RAM specified by PEEK command
Operation Functions	SPDIFSTATR	-	4	S/PDIF input channel status
	GETPTCR	-	8	PTC and STC values of 32 bits each
Progress Response				Data words returned to host in the normal process of sending any command
	EXPECT	-	1	Expected number of parameter words still to be received from host
	ISTATUS	-	1	Interpreter status

Function Commands

AC-3 Decoder + Pro Logic Function *AC3*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	1	0	1
Parameter 1	PRLG		SIF	0	COMP		DMM	
Parameter 2	SF	AB	BCFG		SW	OCFG		
Parameter 3	CDLY			SRDLY				
Parameter 4	HDYNRNG							
Parameter 5	LDYNRNG							
Parameter 6	DSN			0	KAR	RPC		
Parameter 7	PCMSFH							
Parameter 8	PCMSFL							

The AC-3 Decoder function includes normal six-channel AC-3 and the two-channel AC-3 with Pro Logic output. Selection is made in the command for speaker configuration, dynamic range compression, downmixing, delays and error concealment strategy.

PRLG	**Pro Logic** output: 0 = Off, 1 = On, 2 = Selected automatically based on input stream information.
SIF	**Serial Input Format**: 0 = Non-formatted, 1 = AC-3 S/PDIF protocol.
COMP	**Compression** and Dialog Normalization: 0 = Custom mode 0, 1 = Custom mode 1, 2 = Line mode (dialog normalization plus high level compression), 3 = RF modulation mode (peak level compression).
DMM	**Dual Mono Mode** output selection when the two input channels are unrelated: 0 = Stereo, 1 = Mono channel 0 to both, 2 = Mono channel 1 to both, 3 = Mono channels 0 and 1 summed and scaled to both.
SF	**Surround Filter** for Pro Logic: 0 = Filter enabled, 1 = Filter (LP+NR) disabled.
AB	**Auto-Balance** for Pro Logic output: 0 = On, 1 = Off.
BCFG	**Bass Redirection Configuration**: 0 = No redirection, 1 = Redirect left, center, right to subwoofer for Pro-logic. All channels to subwoofer for AC-3, 2 = Redirect center to subwoofer for Pro-logic. Center, left surround and right surround to subwoofer for AC-3, 3 = Reserved.
SW	**Subwoofer** output channel: 0 = Off, 1 = On.
OCFG	**Output Speaker Configuration** of Front/Surround number of speakers (for Pro Logic only OCFG 3-7 can be used): 0 = 2/0 Surround Compatible, 1 = 1/0, 2 = 2/0 Normal, 3 = 3/0, 4 = 2/1, 5 = 3/1, 6 = 2/2, 7 = 3/2. In 2/0 configurations, a mono input is directed to both output channels.
CDLY	**Center Delay** in one millisecond steps from zero to five.
SRDLY	**Surround Delay:** 0-15 = 0-15 ms for AC-3,15-30 ms for Pro Logic in one millisecond steps beyond 15 ms. 16 = zero delay for 3-D Sound.
HDYNRNG	**High Dynamic Range** scale factor controlling the depth of high-level compression. A two's complement fraction between 0.00 and 0.FE where 00 is no high-level compression and 7F is full compression.
LDYNRNG	**Low Dynamic Range** scale factor controlling the depth of low-level compression. A two's complement fraction between 0.00 and 0.FE where 00 is no low-level compression and 7F is full compression.
DSN	**Data Stream Number** for S/PDIF input. Selects which stream to decode. Range 0 -7. Normally zero.
KAR	**Karaoke** mode: 0 = Disabled, 1 = Enabled.
RPC	**Repeat Count** before muting. Maximum number of consecutive block repeats before muting output.
PCMSFH	**PCM Scale Factor High**. Output scale factor, 16-bit two's complement fraction between 0.0000 and 0. FFFE. The high byte. 0000 equals zero, 7FFF equals gain of one.
PCMSFL	**PCM Scale Factor Low**. Output scale factor low byte.

PCM + Pro Logic Decoder Function *PCMPROL*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	1	1	0
Parameter 1	0				DE		DMM	
Parameter 2	SF	AB	BCFG		SW	OCFG		
Parameter 3	CDLY			SRDLY				
Parameter 4	0							
Parameter 5	0							
Parameter 6	0							
Parameter 7	PCMSFH							
Parameter 8	PCMSFL							

The PCM or Pro Logic Decoder function decodes two-channel PCM into four-channel Pro Logic output or transfers to two-channel PCM output. Selection is made in the command for speaker configuration, scale factor, mixing and delay. The parameter descriptions are the same as for the AC3 command except for OCFG and with the addition of DE.

DE	**De-Emphasis filter:** 0 = Filter is disabled, 1 = Filter is enabled, 2 = Filter is enabled if pre-emphasis is defined in the channel status of the S/PDIF input stream.
OCFG	**Output Speaker Configuration** of Front/Surround number of speakers (for Pro Logic only OCFG 3-7 can be used): 0-2 = PCM, 3 = 3/0, 4 = 2/1, 5 = 3/1, 6 = 2/2, 7 = 3/2.

MPEG Decoder Function *MPEG*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	1	1	1
Parameter 1	PRLG		SIF	0	DE		DMM	
Parameter 2	SF	AB	BCFG		SW	OCFG		
Parameter 3	CDLY			SRDLY				
Parameter 4	0							
Parameter 5	0							
Parameter 6	DSN			0	0	0		
Parameter 7	PCMSFH							
Parameter 8	PCMSFL							

The MPEG function decodes MPEG1 or MPEG2 data streams into two-channel PCM output. The selection of MPEG1 or 2 is made automatically from the input stream. All parameters are the same as for the AC3 command except the following.

BCFG	**Bass Redirection Configuration:** 0 = No redirection, 1 = Redirect left and right to subwoofer, 2 & 3 = Reserved.
PRLG	**Pro Logic output:** 0 = Off, 1 = On, 2 & 3 = Reserved.
DE	**De-Emphasis filter:** 0 =Filter is disabled, 1 =Filter is enabled, 2 = Filter is enabled if pre-emphasis is defined in the MPEG stream.
OCFG	**Output Speaker Configuration.** Number of Front/Surround speakers. Valid configurations for MPEG only is 2/0 and MPEG + Pro Logic are OCFG = 3-7. 0 & 1 = Reserved, 2 = 2/0 Normal, 3 = 3/0, 4 = 2/1, 5 = 3/1, 6 = 2/2, 7 = 3/2. In 2/0 configurations, a mono input is directed to both output channels.

Pink Noise Generator Function *PNG*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	0	1	1
Parameter 1	0							
Parameter 2	0	BF	L	C	R	LS	RS	SW
Parameters 3-6	0							
Parameter 7	PCMSFH							
Parameter 8	PCMSFL							

The Pink Noise Generator function produces pseudo-random noise sequence outputs. Selection is made for output channel and scale factor. The parameter descriptions are the same as for AC-3 with the addition of the filter and output channels.

BF	**Bandpass Filter**. 0 = On, 1 = Off.
L	**Left** channel output. 0 = Off, 1 = On.
C	**Center** channel output. 0 = Off, 1 = On.
R	**Right** channel output. 0 = Off, 1 = On.
LS	**Left Surround** channel output. 0 = Off, 1 = On.
RS	**Right Surround** channel output. 0 = Off, 1 = On.
SW	**Subwoofer** channel output. 0 = Off, 1 = On.

User Function *USER*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	0	0	0
Parameter 1	Parameter Word 1							
Parameter 8	Parameter Word 8							

The USER function passes eight bytes of parameters to a user programmed function that has been downloaded.

Operation Commands

Resume Operation — *PLAY*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	0	1	0

The PLAY command resumes operation of the selected function and unmutes the output after a STOP or STOPF command.

Mute Operation — *MUTE*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	0	1	1

The MUTE command mutes the output without stopping the operation of the selected function.

Unmute Operation — *UNMUTE*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	0	0	1

The UNMUTE command restores the muted output while continuing the operation of the selected function.

Stop Operation — *STOP*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	1	0	0

The STOP command stops operation of the selected function if the input is request driven and it mutes the output. Data in the input buffer is preserved but new data is ignored.

Stop Operation and Flush — *STOPF*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	1	0	1

The STOPF command stops operation of the selected function if the input is request driven and it mutes the output. Data in the input buffer is flushed out and new data is ignored.

Return Status Information — *STAT*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	1	1	0

During operation, the STAT command allows the N words of decoder status information to be returned to the host by sending N READ commands.

Return S/PDIF Status Information — *SPDIFSTAT*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	1	1	1	1

The SPDIFSTAT command allows the S/PDIF receiver channel status information and SPRXSTT register value to be returned to the Host by sending four READ commands.

Return PTC Information — *GETPTC*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	1	0

The GETPTC command allows the PTC and STC (Presentation and System Time Clock) values be returned to the Host by sending eight READ commands.

No Operation — *NOP*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	0	0	0

A NOP is not a command and does not affect operation except to cause the ZR38650 to return a response word to the host.

Set-Up Commands

PLL Table — *PLLTAB*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	1	0	0	0
Parameter 1	0			AUDD [12:8]				
Parameter 2	AUDD [7:0]							
Parameter 3	0			AUDM [12:8]				
Parameter 4	AUDM [7:0]							
Parameter 5	0		DSPD					
Parameter 6	DSPM							

The PLLTAB command sets the PLL programmable registers. The audio clock frequency is:

$$f_{AUDIO} = f_{XTI} \times \frac{AUDM}{AUDD} \quad \text{where} \quad AUDD < \frac{f_{XTI}}{10kHz}$$

In master mode, the audio clock generates the serial port clocks, including the S/PDIF transmitter clock.

The DSP clock is:

$$f_{DSP} = f_{XTI} \times \frac{DSPM}{DSPD} \quad \text{where} \quad DSPD < \frac{f_{XTI}}{1MHz}$$

AUDM	**Audio PLL Multiplier:** 13-bit number
AUDD	**Audio PLL Divider:** 13-bit number
DSPM	**DSP PLL Multiplier:** 8-bit number
DSPD	**DSP PLL Divider:** 6-bit number

For example, if f_{XTI} = 24.576 MHz and f_{AUDIO} is 256x a sample rate of 48 kHz, then AUDM = 1 and AUDD = 2. For the fastest processor operation if f_{XTI} = 24.576 MHz, then f_{DSP} = 99.84 MHz if DSPM = 65 and DSPD = 16.

See the section OPERATION WITH COMMANDS on page 24 for a more complete description of these settings.

PLL Configuration *PLLCFG*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	1	0	0	1
Parameter 1	SR			F3	F1	F2	AS	DS

The PLLCFG command defines the PLL programmable configuration. It returns the current status of the PLL lock (PLLR).

PLLCFG must be given before a CFG command. The next serial host command must be delayed by at least 2000 DSP instruction cycles (40 microseconds at 50 MHz) following a change of F1-F3, AS, or DS fields.

SR	**Sampling Rate** of output: 0 = 48 kHz, 1 = 44.1 kHz, 2 = 32 kHz, 3 = 96 kHz.
F1	Determines input clock source for audio PLL: 0 = Internal oscillator or XTI input, 1 = S/PDIF mode using SPFRX.
F2	Determines audio clock f_{AUDIO} source: 0 = Audio PLL, 1 = Internal oscillator or XTI input at f_{XTI}.
F3	Determines master clock output frequency f_{SCKIN}: 0 = Audio clock frequency f_{AUDIO}, 1 = One-half audio clock frequency (f_{AUDIO}/2).
AS	**Audio PLL Set**: 0 = No action, 1 = Resets Audio PLL.
DS	**DSP PLL Set**: 0 = No action, 1 = Resets DSP core PLL

Set Configuration *CFG*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	0	1	0
Parameter 1	WFA	WFB	0	0	0	0	WAIT	
Parameter 2	PES	0	DVD	CB	MB	MA	0	0
Parameter 3	CPB	CPA	FRB			FRA		
Parameter 4	DRQ	0	MPE	EPE	0	0	ISP	OSP
Parameter 5	SEN	AVS	SPO	INW		OUTW		PDI
Parameter 6	SPAS							
Parameter 7	SPBS							
Parameter 8	0		FMB			FMA		

The CFG setup command determines the input, output and external memory configurations for the ZR38650.

WFA	**Word/Frame** synchronization for inputs: 0 = Frame, 1 = Word.
WFB	**Word/Frame** synchronization for outputs: 0 = Frame, 1 = Word.
WAIT	**Wait-state** cycles for external memory: 0 = None, 1 = One, 2 = Three, 3 = Seven.
PES	**PES** packetized input: 0 = Disabled, 1 = Enabled.
DVD	**DVD** mode: 0 = Disabled, 1 = Enabled.
CB	**Clock** source for outputs: 0 = SCKIN input pin, 1 = Internal, using the SPBS scaler with the Audio PLL or system clock.
MB	**Master** mode for output clocking: 0 = Slave, 1 = Master.
MA	**Master** mode for input clocking: 0 = Slave, 1 = Master.
CPB	Serial **Clock B Polarity**: 0 = Negative, 1 = Positive.
CPA	Serial **Clock A Polarity**: 0 = Negative, 1 = Positive.
FRB	**Frame** size (bits) for outputs: 0 = 16, 1 = 32, 2 = 64, 3 = 128, 4 = 192, 5 = 256, 6 = 193, 7 = 24. Normal value = 1.
FRA	**Frame** size (bits) for input: 0 = 16, 1 = 32, 2 = 64, 3 = 128, 4 = 192, 5 = 256, 6 = 193, 7 = 24. Normal value = 1.
DRQ	**Data Request** output pin $\overline{\text{DREQ}}$ (GPIO0): 0 = Disabled, 1 = Enabled.
MPE	**Mute Pin Enable**: 0 = Mute determined by host command, 1 = Mute determined by $\overline{\text{MUTE}}$ (GPIO5) input pin.
EPE	**Error Pin Enable** for ERROR output pin (GPIO1): 0 = Disabled, 1 = Enabled.
ISP	**Input Word Select Polarity**: 0 = Left is WS low, 1 = Left is WS high.
OSP	**Output Word Select Polarity**: 0 = Left is WS low, 1 = Left is WS high.
SEN	**S/PDIF** input selection: 0 = Input from SRA register, 1 = Input from S/PDIF receiver SPRXDAT register.
AVS	**Audio/Video Synchronization**: 0 = Disabled, 1 = Enabled.
SPO	**S/PDIF Output**: 0 = Disabled, 1 = Enabled.
INW	**Input Word**: 0 = 20 bits, 1 = 18 bits, 2 = 16 bits, 3 = 24 bits.
OUTW	**Output Word**: 0 = 20 bits, 1 = 18 bits, 2 = 16 bits, 3 = 24 bits.
PDI	**Parallel Data Interface** for data input stream: 0 = Serial, 1 = Parallel.
SPAS	Group A internal clock divider.
SPBS	Group B internal clock divider.
FMB	Format of serial ports group B: 0-5 = Delay bits, 6 = TDM mode, 7 = Right justified mode (maximum delay is 64).
FMA	Format of serial ports group A: 0-5 = Delay bits, 6 = TDM mode, 7 = Right justified mode (maximum delay is 64).

Set STC — *SETSTC*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	1	1	1
Parameter 1	0	AVS	SCU	0				
Parameter 2	STC [31:24]							
Parameter 3	STC [23:16]							
Parameter 4	STC [15:8]							
Parameter 5	STC [7:0]							
Parameter 6	VDY [15:8]							
Parameter 7	VDY [7:0]							

The SETSTC command sets the system time clock and video delay for A/V synchronization.

AVS	**Audio/Video Synchronization**: 0 = Passive synchronization, 1 = Active synchronization.
SCU	**System Clock Update:** 0 = When SU flag is set, 1 = Immediately.
STC	**System Time Clock:** A 32-bit number in units of 90 kHz.
VDY	**Video Delay**: A 16-bit two's-complement number in units of 90 kHz.

Return Version Number — *VER*

	7	6	5	4	3	2	1	0
Command	1	0	0	0	0	0	0	1

The VER command allows the four words of the ROM version number (VERR) to be returned to the host by sending four READ commands.

Load Program — *BOOT*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	0	0
Parameter 1	Program Word 0							
	//							
Parameter N	Program Word N-1							

The BOOT command allows serial loading and running of a program from the host. (The format is given in Appendix A of the PROCESSOR FUNCTIONAL DESCRIPTION and includes the start address, number of words and instructions). Execution transfers to the start address with no further action by the ROM resident executive.

S/PDIF Channel Status — *SPDIFCS*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	1	0	1
Parameter 1	0				SR			
Parameter 2	CC [7:0]							
Parameter 3	0				PE	C	P	0
Parameter 4	0							

This command defines the output status information for the S/PDIF transmitter. It must be sent before the function command is sent. The SPO bit in the CFG command enables the S/PDIF transmitter.

SR	**Sample Rate** of output: 0 = 44.1 kHz, 2 = 48 kHz, 3 = 32 kHz. All other values reserved.
CC	**Category Code**. The bit order in this parameter is reversed, i.e. bit 0 of IEC-958 Category Code is the rightmost bit.
PE	**Pre-Emphasis** when P = 0: 0 = None, 1 = 50/15 µs.
C	**Copyright** indication.
P	**PCM**: 0 = PCM encoded audio, 1 = Non-PCM encoded audio.

Special Function Parameter — *PARAM*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	1	1	0
Parameter 0	EXT							
Parameter 1	PAR_{12}							
Parameter 2	PAR_{11}							
Parameter 3	PAR_{10}							
Parameter 4	PAR_{22}							
Parameter 5	PAR_{21}							
....	....							

This command defines parameters for special functions that require more then 8 bytes of information. The specific meaning and value of the command parameters are determined by the function that is using it. Any number of parameters can be specified depending on the function. Each parameter contains three bytes which are stored as a single 24-bit word to memory (PAR_{12} is the most significant byte). If the destination memory is 20 bits the four most significant bits of PAR_{i2} are ignored.

EXT	**Opcode Extension:** 0-255 identification number.
PAR_{ij}	**Parameter** number: *i* = 1 through N parameter number, *j* = 2 through 0 byte index.

Interpret Instruction *INTRP*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	0	1
Parameter 1	Instruction [31:24]							
Parameter 2	Instruction [23:16]							
Parameter 3	Instruction [15:8]							
Parameter 4	Instruction [7:0]							

The INTRP set-up command allows loading and running of a single ZR38650 core processor instruction from the host. After the single execution, control transfers to the ROM resident executive with further commands possible from the host.

Set and Return I/O Registers *SETIO*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	1	0
Parameter 1	0		GPIOC MASK					
Parameter 2	0		GPIOC					
Parameter 3	0		GPIO MASK					
Parameter 4	0		GPIO					

The SETIO set-up command allows changing and reading the six single-bits of the general purpose I/O registers GPIO and GPIOC. For the bits set in the GPIO MASK field, the corresponding bits in the GPIO register will be updated to the values set in the GPIO field. The same is true for the GPIOC MASK field and GPIOC register and field. The SETIOR response returns the state of the two registers after the SETIO command.

GPIOC MASK	A set bit *i* of this GPIOC MASK field enables updating the bit *i* of the GPIOC register.
GPIOC	The value of bit *i* in the GPIOC register is updated to the value of bit *i* in this GPIOC field if bit *i* in the GPIOC MASK field is set. GPIOC[*i*] = 0 for an input, GPIOC[*i*] = 1 for an output.
GPIO MASK	A set bit *i* of this GPIO MASK field enables updating the bit *i* of the GPIO register.
GPIO	The value of bit *i* in the GPIO register is updated to the value of bit *i* in this GPIO field if bit *i* in the GPIO MASK field is set.

Load Memory Data *POKE*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	1	1
Parameters 1-3	Start Address [23:0]							
Parameters 4-7	Number of Words (N) [31:0]							
Parameter 8	Data Word 0 [31:24]							
	//							
Parameter 7+4N	Data Word N-1 [7:0]							

The POKE set-up command allows serial loading of data and program from the host to the ZR38650 memory. N 32-bit words are loaded at a 20-bit start address where bits [23:20] are ignored. After the loading, control transfers to the ROM resident executive with further commands possible from the host.

Return Memory Data *PEEK*

	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	1	0	0
Parameter 1	Start Address [23:16]							
Parameter 2	Start Address [15:8]							
Parameter 3	Start Address [7:0]							
Parameter 4	Number of Words (N) [31:24]							
Parameter 5	Number of Words (N) [23:16]							
Parameter 6	Number of Words (N) [15:8]							
Parameter 7	Number of Words (N) [7:0]							

The PEEK command allows serial reading of data and program from the ZR38650 memory to the host. N 32-bit words are read from a 20-bit start address where bits [23:20] are ignored and where N is a 20-bit number. 4N READ commands must be sent from the host to transfer all PEEKR reply data. After reading, control transfers to the ROM resident executive with other commands possible from the host.

Read Command

Read *READ*

	7	6	5	4	3	2	1	0
Command	0	0	0	0	0	0	0	0

The READ command returns a single Reply word to the host after the STAT, VER, SETIO, PLLCFG, PEEK, GETPTC, NOP or SPDIFSTAT commands have been issued. One or more READ commands must be issued after the above commands.

Reply Responses

The first word returned is always EXPECT, the number of expected status words, followed by the status words followed by the interpreter status ISTATUS.

AC3 Status Reply *AC3STATR*

This reply is a response to the STAT command during the AC3 function operation.

	7	6	5	4	3	2	1	0
Status Word 1	STATUS			05				
Status Word 2	RST		AC3DST			AC3IST		
Status Word 3	0							
Status Word 4	0							
Status Word 5	DIFT [15:8]							
Status Word 6	DIFT [7:0]							
Status Word 7	SR		IDR					EW
Status Word 8	0				EF	CCFG		
Status Word 9	BSID					BSM		
Status Word 10	CM		SM		DS		C	OR
Status Word 11	0			DN2				
Status Word 12	0			DN				
Status Word 13	LC2							
Status Word 14	LC							
Status Word 15	P2	RT2		ML2				
Status Word 16	P	RT		ML				

STATUS	**Global Status** of operation in progress: 0 = No errors, 1 = Updated status information is not yet available (a new command has been received and is being processed), 2 = Operation error (see Status word 2 for details).
RST	**Run Status:** 0 = Running, 1 = Stopped, 2 & 3 = Reserved.
AC3DST	**AC-3 Decode Status** returned by routine: 0 = No errors, 1 = Input status nonzero, last output block was repeated, 2 = Input status nonzero, outputs were muted, 3 = Unsupported bitstream identification revision, 4 = Unsupported number of channels in input stream, 5 = Unsupported number of input streams.
AC3IST	**AC-3 Frame Information Status** returned by routine: 0 = No errors, 1 = Invalid frame sync, 2 = Invalid sample rate, 3 = Invalid data rate, 4-6 = Reserved, 7 = Input underflow.
DIFT[15:0]	**Difference Time.** Signed difference between PTC and STC in units of the 90-kHz clock. For packetized inputs.
SR	**Sample Rate:** 0 = 48 kHz, 1 = 44.1 kHz, 2 = 32 kHz.
IDR	**Input Data Rate** in Kbits per second: 0 = 32, 1 = 40, 2 = 48, 3 = 56, 4 = 64, 5 = 80, 6 = 96, 7 = 112, 8 = 128, 9 = 160, 10 = 192, 11 = 224, 12 = 256, 13 = 320, 14 = 384, 15 = 448, 16 = 512, 17 = 576, 18 = 640.
EW	**Extra Word** packed: 0 = No, 1 = Yes for 44.1 kHz sample rate only.
EF	**Effects** channel for low frequency: 0 = No, 1 = Yes.
CCFG	**Coding Configuration**: 0 = Dual mono mode, 1 = 1/0, 2 = 2/0, 3 = 3/0, 4 = 2/1, 5 = 3/1, 6 = 2/2, 7 = 3/2.
BSID	**Bit-Stream Identification** number of five bits.
BSM	**Bit-Stream Mode**: 0 = Main audio service, 1 = Main audio service minus dialog, 2 = Associated service; visually impaired, 3 = Associated service; hearing impaired, 4 = Associated service; dialog, 5 = Associated service; commentary, 6 = Associated service; emergency flash.
CM	**Center Mix** level: 0 = -3 dB, 1 = -4.5 dB, 2 = -6 dB.
SM	**Surround Mix** level: 0 = -3 dB, 1 = -6 dB, 2 = None.
DS	**Dolby Surround** mode: 0 = No indication, 1 = Not Dolby Surround encoded, 2 = Dolby Surround encoded.
C	**Copyright:** 0 = Not copyright protected, 1 = Copyright protected.
OR	**Original:** 0 = Copy of an original bit-stream, 1 = Original bit-stream.
DN2	**Dialog Normalization for Channel 2** in dual mono.
DN	**Dialog Normalization** value for normal operation.
LC2	**Language Code for Channel 2** in dual mono.
LC	**Language Code** for normal operation.
P2	**Production information for Channel 2** in dual mono operation. 0 = Does not exist, 1 = Does exist.
RT2	**Room Type for Channel 2** in dual mono operation. 0 = Not indicated, 1 = Large, 2 = Small.
ML2	**Mix Level for Channel 2** in dual mono operation.
P	**Production** information in normal operation: 0 = Does not exist, 1 = Does exist.
RT	**Room Type** in normal operation: 0 = Not indicated, 1 = Large, 2 = Small.
ML	**Mix Level** value in normal operation.

PCMPROL Status Reply *PCMPROLR*

	7	6	5	4	3	2	1	0
Status Word 1	STATUS			04/06				
Status Word 2	RST		0					
Status Words 3-6	0							
Status Word 7	VERSION							
Status Word 8	0							

This reply is a response to the STAT command during the PCM or Pro Logic function operation. The status fields are the same as for AC3STATR except:

VERSION	Version number of the PCMPROL function.

MPEG Status Reply *MPEGSTATR*

	7	6	5	4	3	2	1	0
Status Word 1	STATUS				07			
Status Word 2	RST			0			MPGST	
Status Word 3	0							
Status Word 4	0							
Status Word 5	DIFT [15:8]							
Status Word 6	DIFT [7:0]							
Status Word 7	0				ID	LAY		PRT
Status Word 8	BR				SFR		PAD	PVR
Status Word 9	MODE			MEXT	CRP	ORG	EMPH	
Status Words 10-12	0							

This reply is a response to the STAT command during the MPEG function operation.

MPGST	**MPEG-1 Decode Status** returned by routine: 0 = No errors, 1 = Invalid frame sync, 2 = CRC error, 3 = Invalid sample rate, 4 = Invalid data rate, 5 = Input underflow.
ID	**Algorithm ID**: 0 = Reserved, 1 = MPEG.
LAY	**Layer** type: 0 = Reserved, 1 = Layer III, 2 = Layer II, 3 = Layer I.
PRT	**Protection** bit: 0 = CRC word present, 1 = No CRC word.
BR	**Bit-Rate** index (see ISO-MPEG document CD 11172-3, part 3).
SFR	**Sampling Frequency**: 0 = 44.1 kHz, 1 = 48 kHz, 2 = 32 kHz.
PAD	**Padding** bit.
PRV	**Private** bit.
MODE	**Encoding Mode:** 0 = Stereo, 1 = Joint-stereo, 2 = Dual channel, 3 = Single channel.
MEXT	**Mode Extension** (see ISO-MPEG document).
CPR	**Copyright**: 0 = None, 1 = Copyrighted.
ORG	**Original**/home: 0 = Copy, 1 = Original.
EMPH	**Emphasis**: 0 = None, 1 = 50/15 µs, 2 = Reserved, 3 = CCITT J.17.

PNG Status Reply *PNGSTATR*

	7	6	5	4	3	2	1	0
Status Word 1	STATUS			03				
Status Word 2	RST		0					
Status Words 3-6	0							
Status Word 7	VERSION							
Status Word 8	0							

This reply is a response to the STAT command during operation of the PNG function.

VERSION	Version number of the Pink Noise functions.

Version Number Reply *VERR*

	7	6	5	4	3	2	1	0
Data Word 0	ROM Version Number [31:24]							
Data Word 1	ROM Version Number [23:16]							
Data Word 2	ROM Version Number [15:8]							
Data Word 3	ROM Version Number [7:0]							

The VERR reply is a response to the VER command. It is four data words of the version number of the ROM resident executive transferred by using four READ commands.

Set I/O Register Reply *SETIOR*

	7	6	5	4	3	2	1	0
Status Word 1	0		GPIOC Register					
Status Word 2	0		GPIO Register					

The SETIOR reply is a response to the SETIO command. It is two data words with the most recent contents of the GPIO and GPIOC registers.

PLLCFG Reply *PLLR*

	7	6	5	4	3	2	1	0
Status Word 1	0						PA	PD

The PLLR reply is a response to a READ following the PLLCFG command. Returns one byte indicating the status of PLL locking.

PA	**PLL for Audio**: 0 = Not locked, 1 = Locked.
PD	**PLL for DSP** core: 0 = Not locked, 1 = Locked.

Data Memory Reply *PEEKR*

	7	6	5	4	3	2	1	0
Data Word 0	Memory Data Word 0 [31:24]							
	//							
Data Word N-1	Memory Data Word N-1 [7:0]							

The PEEKR reply is a response to the PEEK command. It is N data words with the contents of the specified ZR38650 memory locations that is transferred by 4N READ commands.

S/PDIF Status Reply *SPDIFSTATR*

	7	6	5	4	3	2	1	0
Status Word 1	0				SR			
Status Word 2	CC [7:0]							
Status Word 3	0				PE	C	P	0
Status Word 4	SPRXSTT [7:0]							

The SPDIFSTATR reply provides the following S/PDIF receiver status information in response to the SPDIFSTAT command:

SR	**Sample Rate** of input: 0 = 44.1 kHz, 2 = 48 kHz or 96 kHz, 3 = 32 kHz. All other values reserved.
CC	**Category Code**. The bit order in this parameter is bit-reversed from the standard IEC-958 Category Code where bit 0 is the left-most. Here bit 0 is the right-most bit.
PE	**Pre-Emphasis** when P = 0: 0 = None, 1 = 50/15 µs.
C	**Copyright** indication.
P	**PCM**: 0 = PCM encoded audio, 1 = Non-PCM encoded.
SPRXSTT	**S/PDIF Receiver Status.** Seven bits indicating L/R channel, loss of synchronization, beginning of a new block and errors for preamble, parity, biphase and invalid input.

GETPTC Reply *GETPTCR*

	7	6	5	4	3	2	1	0
Status Words 1-4	PTC [31:0]							
Status Words 5-8	STC [31:0]							

The GETPTCR reply is a response to eight READ commands following the GETPTC command.

PTC	**Presentation Time Clock.** Least significant 32 bits in units of 90 kHz. Most significant byte first.
STC	**System Time Clock.** Least significant 32 bits in units of 90 kHz. Most significant byte first.

Progress Responses

Expected Parameters Response *EXPECT*

	7	6	5	4	3	2	1	0
Status Word 1	Number of Expected Parameter Words							

EXPECT is a progress response to any command sent from the host. It is one data word returned to the host with the number of parameter words still expected by the ZR38650 at the time it was sent, or the number of words still to be returned by a reply response. It is not sent when the expected number is zero.

Interpreter Status Response *ISTATUS*

	7	6	5	4	3	2	1	0
Status Word 1	ISTATUS							

The last word returned by the device after receiving a Host command is a status word. The ISTATUS field flags any errors detected during decoding and interpretation of the host command.

ISTATUS	**Interpreter Status** (Hex): 80 = No errors, 81 = Invalid opcode, 82 = Invalid parameters, 83 = Not ready to accept new commands, 84 = Command overflow, 85 = Ready to accept new commands.

Note that the Host commands are executed only after all parameters have been received and correctly decoded. Therefore the status word does not show the outcome of the command execution, but only the result of command interpretation.

If the Host issues a new command before the previous one has been executed the device ignores the new command and returns ISTATUS = 83.

The Host command STAT can be used to get information on the current execution status of a function.

Table 9: Sequence Of Commands And Responses Summary

Class	Command - A Single Word	Number of Parameter Words P	Number of Read Words R	Response To Command + P+ R	Response To STAT Command + (S + 1) READs	Number of Status Words S	Command Description
Function	AC3	8	-	8 EXPECT + ISTATUS	EXPECT + AC3STATR + ISTATUS	16	AC-3 and Pro Logic decoder
	PCMPROL	8	-	8 EXPECT + ISTATUS	EXPECT + PCMPROLR + ISTATUS	8	PCM or Pro Logic decoder
	MPEG	8	-	8 EXPECT + ISTATUS	EXPECT + MPEGSTATR + ISTATUS	12	MPEG or MPEG + Pro Logic decoder
	PNG	8	-	8 EXPECT + ISTATUS	EXPECT + PNGSTATR + ISTATUS	8	Pink Noise Generator
	USER	8	-	8 EXPECT + ISTATUS	User Defined + ISTATUS	User Defined	User defined function
Operation	PLAY	0	-	ISTATUS	-	-	Resume operation
	MUTE	0	-	ISTATUS	-	-	Mute audio output
	UNMUTE	0	-	ISTATUS	-	-	Restore muted output
	STOP	0	-	ISTATUS	-	-	Stop operation
	STOPF	0	-	ISTATUS	-	-	Stop operation, flush data
	STAT	0	See under functions				Return decoder status
	SPDIFSTAT	0	4 + 1	EXPECT + SPDIFSTATR + ISTATUS	-	4	Return the S/PDIF input channel status
	GETPTC	0	8 + 1	EXPECT + GETPTCR + ISTATUS	-	8	Return the PTC value
	NOP	0		ISTATUS	-	-	No operation
Set-Up	PLLTAB	6	-	6 EXPECT + ISTATUS	-	-	Set the PLL tables
	PLLCFG	1	1	EXPECT + PLLR + ISTATUS	-	1	Define the PLL configuration
	CFG	8	-	8 EXPECT + ISTATUS	-	-	Configure the I/O
	SETSTC	7	-	7 EXPECT + ISTATUS	-	-	Set System Time Clock
	VER	0	4 + 1	EXPECT + VERR + ISTATUS	-	4	Return ROM version number
	BOOT	4N	-	4N EXPECT + ISTATUS	-	-	Load and execute N-word bootstrap program
	SPDIFCS	4	-	4 EXPECT + ISTATUS	-	-	Write the S/PDIF output channel status
	PARAM	1 + 3N	-	1 + 3N EXPECT + ISTATUS	-	-	Define N parameter data words for special functions
	INTRP	4	-	4 EXPECT + ISTATUS	-	-	Interpret parameters as ZR38001 instruction
	SETIO	4	-	2 EXPECT + SETIOR + ISTATUS	-	2	Set, test and return GPIO registers
	POKE	7 + 4N	-	7 + 4N EXPECT + ISTATUS	-	-	Load N core processor RAM locations
	PEEK	7	4N	7 EXPECT + PEEKR + ISTATUS	-	4N	Read N core processor RAM locations

OPERATION WITH COMMANDS

This section describes operation principles when using the command structure and its configuration choices.

Start-Up

After being reset by the system $\overline{\text{RESET}}$ signal, the ZR38650 will check for an external program ROM to load. Not finding this it will start execution from the internal ROM and await commands from the host. Normal host operation would confirm the ROM version number and then configure the ZR38650 to match the system and desired operation. The command configuration sequence PLLTAB, PLLCFG, CFG is mandatory and must precede any decoding function selection.

The PLL Configuration

Two phase-locked-loops (PLLs) allow independent selection of the core processor clock rate (f_{DSP}) and the serial digital audio clock rate (f_{AUDIO}) for a variety of system clock frequencies (f_{XTI}) and sources. Figure 6 shows the system oscillator, the two PLLs, the serial I/O divider chains and the interconnection selections. These are configured with the PLLTAB, PLLCFG and the CFG commands.

The DSPM and DSPD fields in the PLLTAB command (see page 16) determine the core processor clock rate to allow a choice between processing performance and lower power at lower clock rates. Table 10 shows some representative values for common system clock frequencies.

The AUDM and AUDD fields in the PLLTAB command determine the serial digital audio master clock rate for the I/O dividers. Table 11 shows some representative and recommended values for common sample rates and master clock multiples.

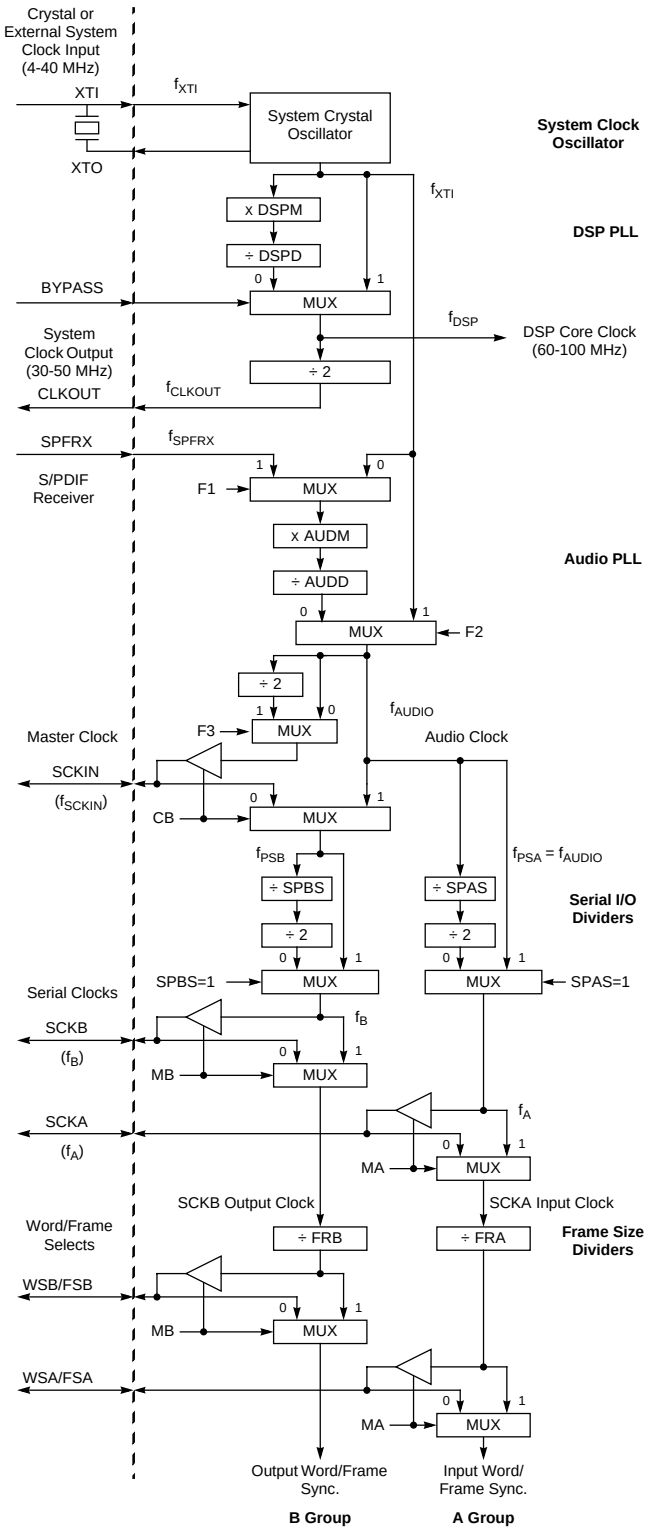


Figure 6. The System Clock Oscillator, The DSP PLL And The Audio PLL With Serial I/O Divider Chains

Table 10: Representative Values For DSPM And DSPD In The PLLTAB Command

System Clock Frequency f_{XTI}	Nominal Processor Core Clock Frequency f_{DSP}							
	66 MHz		72 MHz		80 MHz		100 MHz	
	DSPM/ DSPD	Actual f_{DSP}	DSPM/ DSPD	Actual f_{DSP}	DSPM/ DSPD	Actual f_{DSP}	DSPM/ DSPD	Actual f_{DSP}
12.288 MHz	27/5	66.35 MHz	41/7	72 MHz	13/2	79.9 MHz	65/8	99.8 MHz
16.9344 MHz	27/7	65.3 MHz	17/4	72 MHz	14/3	79 MHz	35/6	98.8 MHz
18.432 MHz	18/5	66.35 MHz	27/7	71 MHz	13/3	79.9 MHz	65/12	99.8 MHz
24.576 MHz	35/13	66.17 MHz	47/16	72.2 MHz	39/12	79.9 MHz	65/16	99.8 MHz
27.0 MHz	22/9	66.0 MHz	8/3	72.0 MHz	80/27	80.0 MHz	100/27	100.0 MHz
32.0 MHz	33/16	66.0 MHz	9/4	72.0 MHz	5/2	80.0 MHz	25/8	100.0 MHz

Table 11: Representative And Recommended* Values For AUDM/AUDD In The PLLTAB Command

System Clock Frequency f_{XTI}	Serial Audio Master Clock Frequency f_{AUDIO}				
	8.192 MHz (256 x 32 kHz)	11.2896 MHz (256 x 44.1 kHz)	12.288 MHz (256 x 48 kHz) (384 x 32 kHz)	16.9344 MHz (384 x 44.1 kHz)	18.432 MHz (384 x 48 kHz)
12.288 MHz	3/2*	147/160	1/1*	441/320	3/2*
16.9344 MHz	1280/2646	2/3*	640/882	1/1*	960/882
24.576 MHz	1/3*	294/640	1/2*	882/128	3/4*
27.0 MHz	1024/3375	784/1875	512/1125	392/625	256/375
32.0 MHz	32/125	441/1250	48/125*	1323/2500	72/125

Input/Output Configuration

The CFG configuration command (see page 17) and the SETIO command (see page 19) determine the digital input and output configuration.

Connections to the data stream input, the output DACs and the single-bit general purpose registers are made through the input/output ports. There are seven digital audio input and output ports (Port A, E and F are inputs and Ports B, C, D and G are outputs). There are six single-bit general purpose user defined I/O ports: GPIO[5:0].

Serial Ports

The bit-serial ports serve a variety of peripheral device conventions. Their operation is determined solely by the CFG configuration command. The input Port Group A (serial inputs A, E, F) and output Port Group B (serial outputs B, C, D and G) have separate clocking systems and may be individually selected with the ZR38650 acting as a master or a slave (Port F can be activated with the clocking systems of Port Group B). The system clock (f_{XTI}), the audio PLL locked to the system clock or the S/PDIF receiver can generate a master audio clock f_{AUDIO}. This can be used to generate the two internal input and output bit-rate clocks when they are masters. See Figure 6.

If input port group A is a master, SCKA is at a frequency $f_A = f_{PSA}/(2 \cdot SPAS)$ where f_{PSA} is the audio clock f_{AUDIO}. In the case where SPAS equals one, f_A is equal to f_{PSA}. The divider SPAS is a field in the CFG command. Likewise, when output port group B is master, SCKB is at a frequency $f_B = f_{PSB}/(2 \cdot SPBS)$ where f_{PSB} is the internal audio clock f_{AUDIO} or an external clock f_{SCKIN} received through the SCKIN pin. In the case where SPBS equals one, f_B is equal to f_{PSB}.The outputs are unique in that when operating as a master their clock outputs can also be derived from an externally supplied master clock input (SCKIN) with the programmable divider rate SPBS. This selection is made with the CB field in the CFG command. Some of these choices are summarized in Table 12.

Table 12: Serial Ports A & B Clocking Summary In The CFG And PLLCFG Commands

Function	Input Port Group A	Output Port Group B
Audio PLL source from S/PDIF or System Clock	F1	
Audio Clock source from Audio PLL or System Clock	F2	
External master clock input SCKIN pin (f_{SCKIN})	None	CB field = 0
Internal master clock ($f_{PSB} = f_{AUDIO}$) and Master external clock output pin	None	CB field = 1
Master or slave clocking mode	MA field	MB field
Internal 12-bit master clock scalers for SCKA and SCKB. LS 8-bit fields.	SPAS field ($f_A = f_{PS\ A}$/ [2•SPAS])	SPBS field ($f_B = f_{PSB}$ / [2•SPBS])
Bypass of clock scalers	$f_A = f_{PSA}$if SPAS=1	$f_B = f_{PSB}$ if SPBS=1
Data latched/sent out on rising/falling edge of clock	CPA = 0	CPB = 0
Data latched/sent out on falling/rising edge of clock	CPA = 1	CPB = 1

Table 13 shows some representative values for both SPBS and AUDM/AUDD for different output sample frequencies (f_S) and master clock multiples of the sample frequency. They are for the common choice of a system clock frequency of 24.576 MHz.

Table 13: Example SPBS And AUDM/AUDD Settings With A 24.576 MHz System Clock f_{XTI}

f_S	f_{AUDIO}	f_{AUDIO} (SCKIN Output)	AUDM/AUDD	SPBS	SCKB Output (64 f_s)
48 kHz	256 f_s	12.288 MHz	1/2	2	3.07 MHz
48 kHz	384 f_s	18.432 MHz	3/4	3	
48 kHz	512 f_s	24.576 MHz	1/1	4	
96 kHz	256 f_s	24.576 MHz	1/1	2	6.144 MHz

Serial Port Formats

Many choices are possible for the bit-serial port formats and word sizes. The five most commonly used formats are summarized in Table 15 along with the selectable word sizes. Waveforms for each are illustrated in Figures 7-11. Note the various frame durations indicated. Clocking for both master and slave operation is shown. The transitions marked are the edges where data changes when the ZR38650 is a master or where the data is sampled when it is a slave. Settings for the appropriate fields in the CFG command are also summarized.

Word select (WS) or frame synchronization (FS) is chosen with the WFA and WFB fields. The polarity of the WS signal is chosen with the ISP and OSP fields. Either polarity is acceptable on any of the word select formats. Through the FMA field the frameless input operation of Format 3 can be chosen. The input then is sampled every SCKA and an interrupt generated after 16 bits has been received. Note that when a master the FS signal shown is, in fact, generated and if FS is asserted when a slave it will re-synchronize the data as shown. This format may not be accepted by some function operating modes.

Digital Audio Receiver

The digital audio receiver function of the ZR38650 is fully compliant with the IEC-958, S/PDIF, AES/EBU and EIAJ CP-340 consumer mode interface standards. It will lock on to the incoming bitstream and extract the clock and data information. The data is supplied to the processor for decoding and the clock is multiplied to yield a 256x or 384x sample rate, as required by the DACs. This master clock signal is available on the SCKIN pin as an output.

For correct operation of the S/PDIF receiver the following initialization steps are required:

- The AUDD variable in the PLLTAB command should be set to approximately 128 x f_{XTI}, where f_{XTI} is the clock input frequency expressed in MHz (i.e. if f_{XTI} = 12.288 MHz, then AUDD equals the integer portion of 12.288 x 128 = 1572). AUDM should be set to 4 or 6, for 256x or 384x sample rate audio clock output, respectively.
- The F1 field in the PLLCFG command should be set to 1.
- The SEN field in the CFG command should be set to 1.

Other representative values for AUDM/AUDD, F3 and SPBS when using the S/PDIF receiver are given in Table 14 for various sample rates and master clock rates. They are for the common choice of a system clock frequency (f_{XTI}) of 24.576 MHz**.**

Table 14: Example SPBS, AUDM/AUDD and F3 Settings using the S/PDIF Receiver and a 24.576 MHz System Clock f_{XTI}

f_s	Master Clock	Master Clock f_{SCKIN}	F3	Audio Clock (f_{AUDIO})	AUDM/AUDD	SPBS	SCKB Output (64 f_s)
48 kHz	256 f_s	12.288 MHz	0	12.288 MHz	4/3416	2	3.072 MHz
44.1 kHz	384 f_s	16.9344 MHz	0	16.9344 MHz	6/3416	3	2.8224 MHz
32 kHz	256 f_s	8.192 MHz	0	8.192 MHz	4/3416	2	2.048 MHz
96 kHz	128 f_s	12.288 MHz	1	24.576 MHz	4/3416	2	6.144 Mhz

Digital Audio Transmitter

The digital audio transmitter of the ZR38650 is fully compatible with IEC-958, S/PDIF, AES/EBU and EAIJ CP-340 consumer mode standards. This function enables the transmission of digital audio bitstreams to an external decoder for processing in all modes of operation, i.e. AC-3, MPEG or PCM. The transmitter is enabled by setting the SPO bit in the CFG command. The Channel Status information required by IEC-958 should be supplied to the ZR38650 through the SPDIFCS command See the section S/PDIF Channel Status SPDIFCS on page 18. It is important to set the Channel Status bits for an external decoder to operate correctly. When the S/PDIF output is enabled, the fourth serial port SDG is disabled. Note that the output frame size must be 32 bits (FRB = 1) when using the S/PDIF output.

General Purpose Ports

There are six single-bit general purpose ports GPIO[5:0] normally configured as inputs at reset. GPIO5 is normally used as the $\overline{\text{MUTE}}$ input and GPIO0 as the $\overline{\text{DREQ}}$ output. GPIO1 is normally the ERROR output signal. GPIO[5:0] may be configured as user defined outputs by setting the GPIOC field in the SETIO command. Inputs pins, the ones that are defined as inputs from GPIO[5:0], are sampled and read from the GPIO register by the host with the SETIO command. At the same time it can set the state of the pins that are configured as output pins.

Decoder Operation

A typical decoder function selection command sequence would be:

AC3, UNMUTE...MUTE...PROL, UNMUTE...

where AC-3 is selected first, then followed by a switch to ProLogic at a later time. If the DRQ bit in command CFG is set, the command sequence must include a PLAY:

AC3, PLAY, UNMUTE...MUTE, STOP...MPEG, PLAY, UNMUTE....

Table 15: Input and Output Format Selections In The CFG Command

Format		Figure	CFG Configuration Command Fields				
			WFA or WFB Frame/Word	ISP or OSP Word Polarity	FMA or FMB Format	CPA or CPB Clock Polarity	INW or OUTW Input or Output Word Size
0	I^2S	7	1	0	1	0	16, 18, 20, 24 bits
1	EIAJ	8	1	1	7	0	16, 18, 20, 24 bits
2	Non-Delayed	9	1	0	0	0	16, 18, 20, 24 bits
3	Frameless	10	0	0	6	1	16 bits
4	Frame Sync	11	0	0	1	1	16, 18, 20, 24 bits

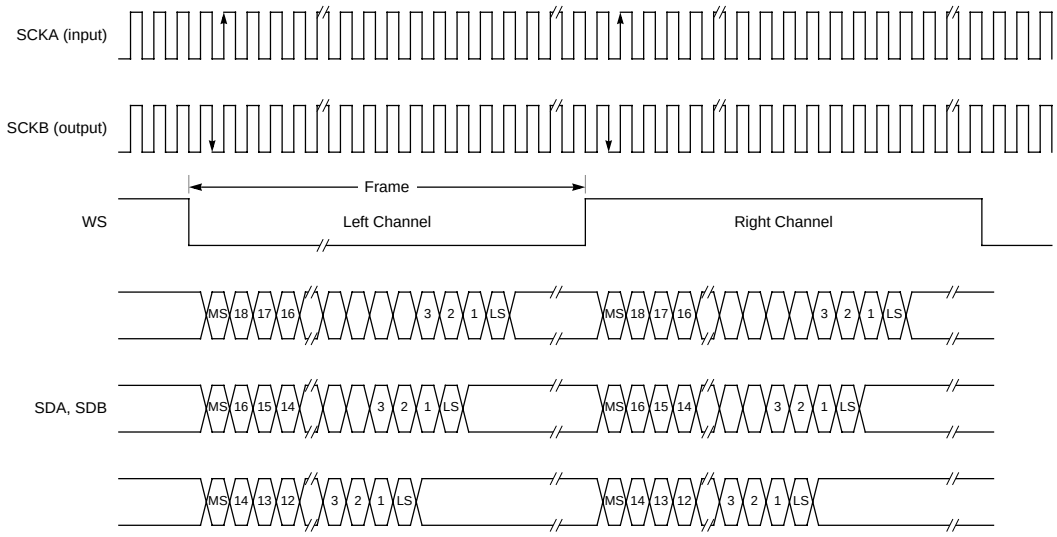


Figure 7. I^2S Input/Output - Format 0

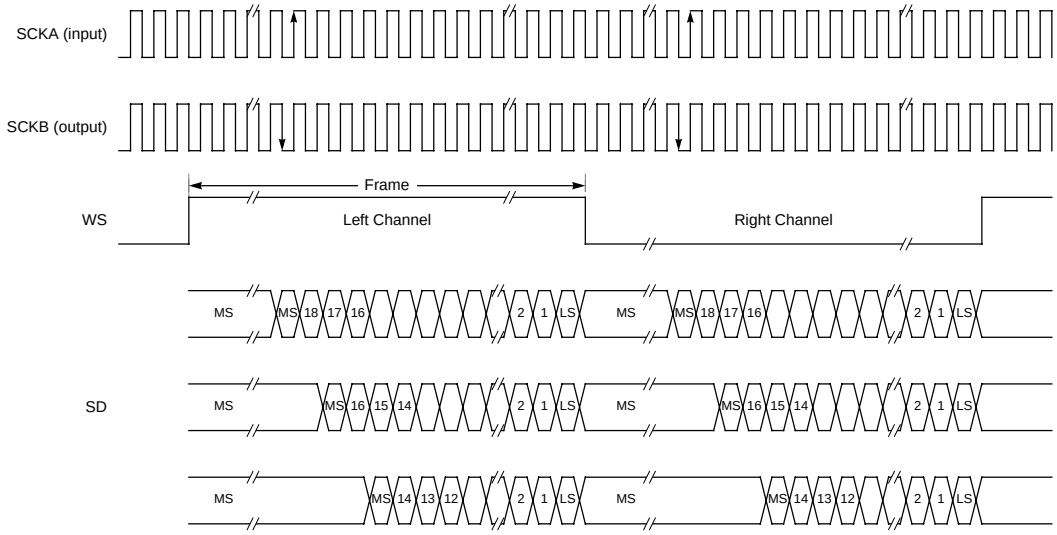


Figure 8. EIAJ Input/Output - Format 1

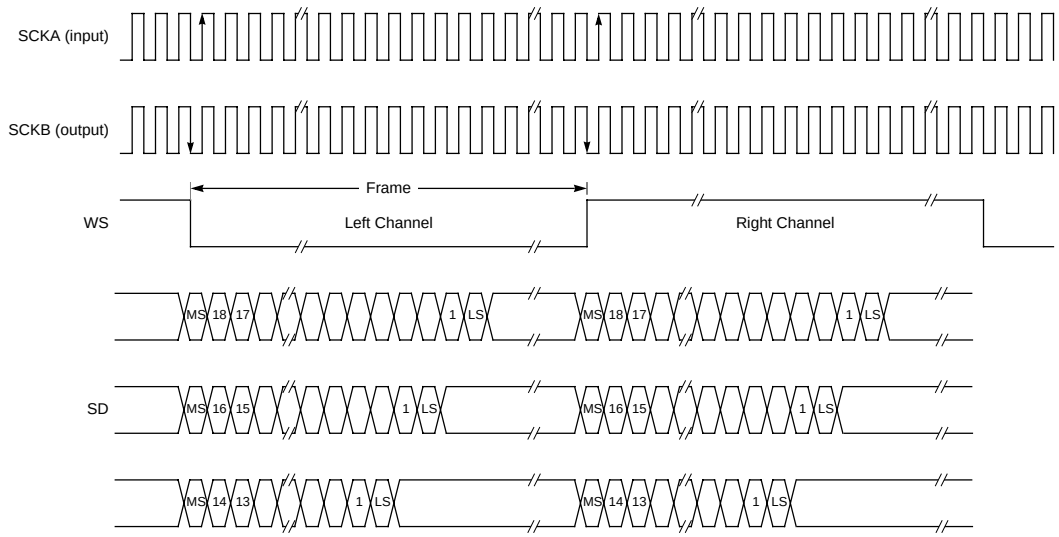


Figure 9. Non-Delayed Input/Output - Format 2

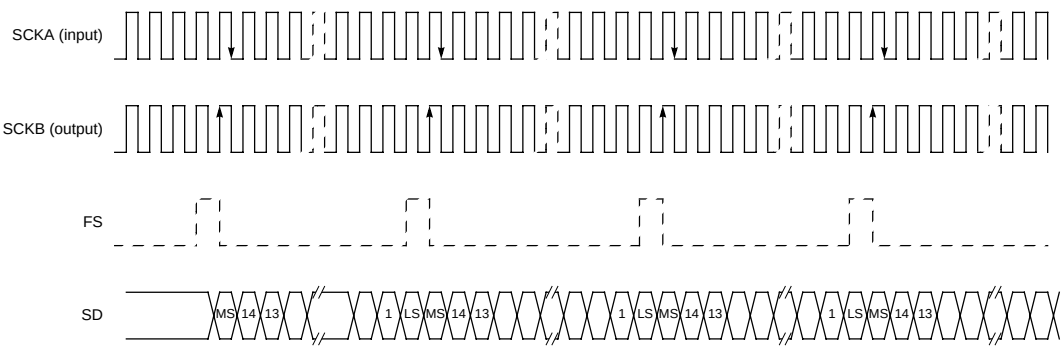


Figure 10. Frameless Input - Format 3

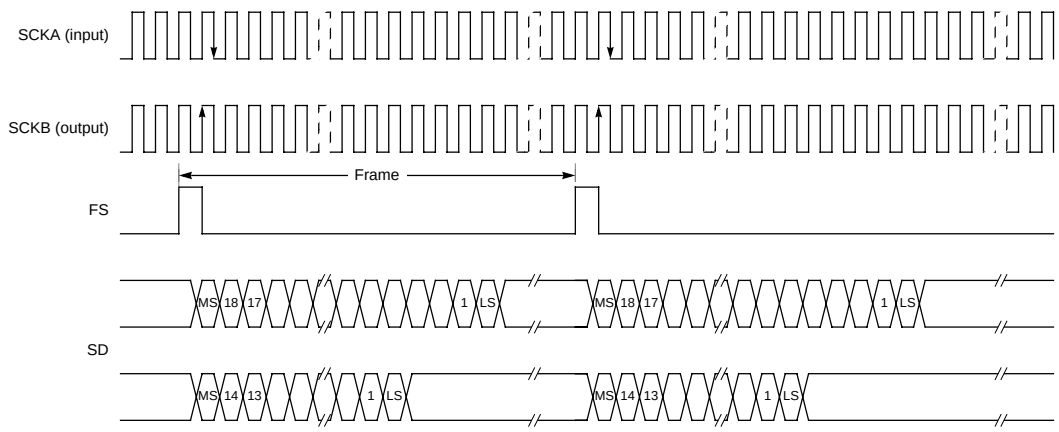


Figure 11. Frame Sync Input/Output - Format 4

PROCESSOR GENERAL DESCRIPTION

With its versatile internal architecture, general purpose instruction set and high speed, the ZR38650's core processor is also capable of executing many other types of algorithms for a wide variety of DSP applications. These algorithms can add differentiating product features to the basic audio decoding functions. With the ZR38650's state-of-the-art performance these additional features take little processing time or program memory.

A high level of performance is made possible by the 32-bit wide instruction set which allows the device to perform a large number of concurrent operations. For example, in a single instruction cycle the following operations can be performed:

- Fetch two source operands from registers, execute an arithmetic operation and store the result in a register.
- Update two data address pointers
- Perform two parallel data move operations
- Generate the next program address
- Fetch the next program instruction.

Individual bit and immediate data instructions along with the ZR38650's four-level zero-overhead loop and repeat instructions, produce very compact code. Most instructions execute in a single cycle.

The ZR38650 uses an internal clock rate of up to 100 MHz to achieve 50-million instructions per second (50-MIPS) performance. This allows accessing internal data memory twice per instruction cycle. An internal programmable phase-locked loop (PLL) multiplier/divider circuit permits any external crystal or input clock to be used (in the range of 12-50 MHz).

The ZR38650's optimized 20-bit (120 dB) data precision make it particularly well suited for compact disk-quality audio applications including audio equalization, special effects and audio mixing where the 16-bit data precision of conventional fixed-point DSPs is insufficient. Furthermore, by providing high performance support for block floating-point operations to extend dynamic range (including one cycle exponent detection and two cycle normalization), ZR38650-based systems are inherently more cost effective to implement than 24-bit precision fixed-point DSPs which expand dynamic range solely via extended data precision. High performance block floating-point is due to the ZR38650's bi-directional barrel shifter, a feature unavailable on most conventional 16- and 24-bit fixed-point DSPs.

To ease programming and increase speed, the ZR38650 architecture provides a general purpose data register file which can provide up to four source registers and two destination registers per instruction. A total of eight 20-bit data registers are provided, with two registers extended to 48-bits for use as accumulator registers with 8-bit overflow protection.

The ZR38650 also provides a dual address generator and register file capable of generating two independent addresses per instruction cycle. The address generator supports modulo and bit-reversed addressing, in addition to a complete set of pre- and post-modify addressing modes.

The ZR38650 has many built-in memory resources. A large 2k x 32-bit program/data RAM is available on-chip in additional to the mask programmable 20k x 32-bit ROM. The already large internal 10k x 20-bit data RAM along with program/data memory can be extended on the 32-bit external data bus and 20-bit memory address bus, with up to 1M words in a unified address space. Programmable wait-states accommodate lower-cost slow external memories and byte-wide configurations can be used for lower chip count if desired.

PROCESSOR FUNCTIONAL DESCRIPTION

Architectural Overview

Figure 12 shows the detailed functional units of the ZR38650 processor. The data path consists of the Arithmetic Unit, the portions of Memory used for data, and its associated Address Generation Unit. The control path is the Instruction Unit, the portions of Memory used for program, and its associated Program Sequence Unit. The remainder are the Input/Output Ports and the System Interface.

Data flow between data path units is over the single 20-bit Data Bus with a corresponding 20-bit Data Address Bus. Control flow is over the single 32-bit Program Data Bus with a corresponding 20-bit Program Address Bus. These dual data and address buses are multiplexed to single external buses for external memories. This simple space-efficient bus structure maintains high performance as each internal bus makes two transfers per instruction cycle and each unit is self-contained with its own local memory.

The high performance of the ZR38650 is apparent from the power of the data functional units with their attendant instructions and their being matched by the power of the control functional units and their instructions. Both are described in turn. Data and control paths are assured of working together in parallel because of the fast interconnecting bus structure and the wide-word instruction set controlling both. This view of the operation by function and instruction can confirm basic benchmark performance. In actual designs, the powerful assembler and simulator show the details of the pipelined operations and intermeshing of functions and transfers to assure balanced operation.

Arithmetic Unit

The arithmetic unit performs all data path operations in the processor, using a full-function ALU, a bi-directional barrel shifter and a 20 x 20-bit multiplier, all operating out of the multiport register file. The seven ports allow two transfers in or out of the

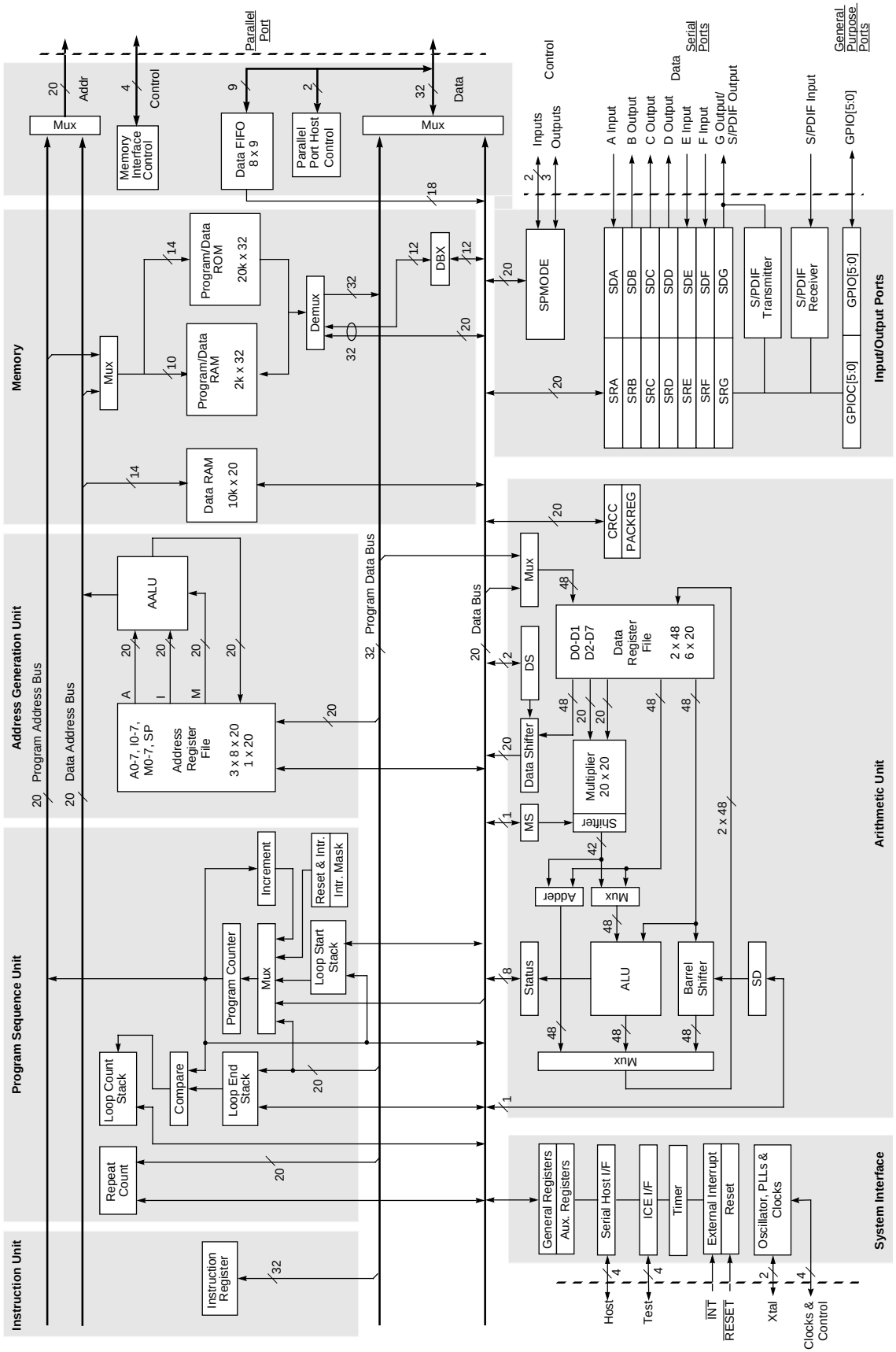


Figure 12. ZR38650 Detailed Block Diagram

register file from memory in parallel with a three operand multiplier and ALU operation, including storing the result, every instruction cycle.

In addition to the basic two's-complement arithmetic and logical operations, the 48-bit ALU also can find minimums and maximums, normalize, determine exponents for block floating-point, support multiple precisions and perform division primitives. A further refinement is a butterfly primitive that computes both a product sum and difference using an auxiliary adder. This fetching of four operands, doing a multiply, addition and subtraction and storing two results facilitates a very fast 4-cycle radix-2 FFT butterfly. ALU results set appropriate Status register bits in the System Interface, which has sticky bits for multiple precision and array computations. A large class of immediate data logical and arithmetic instructions free register space and reduce instruction count in the bit operations so common in communications coding applications.

The multiplier provides both signed and unsigned operations with an optional one-bit left shift on the output determined by the MS bit in the Mode register. This shift for fractional number alignment preserves the maximum 42 bits of shifted products. The 48-bit barrel shifter does both logical and arithmetic shifts; the SD bit in the Mode register allows a positive shift operator to be interpreted as either a left or a right direction shift. A third Data Shifter provides arithmetic shifts, rounding and limiting when transferring data from the register file onto the Data Bus. The shifting range of 1 bit to the right through to 2 bits to the left is determined by the DS bits in the Mode register.

Two of the eight registers of the register file (D0 & D1) are 48 bits, the remaining six are 20 bits and align as shown in Figure 13. In general all arithmetic unit operations are for implicit 20-bit operands with data being overflowed, limited, rounded or truncated accordingly for registers D2-D7. However when D0 or D1 are the source or destination, then the operations are such as to preserve the full 48-bit precision results in these registers. Likewise, transfers in and out of D0 & D1 with the data buses are extended or reduced based on their being 48-bit operands. These two registers usually serve as the high precision accumulators which are central to most signal processing algorithms. Any of the three fields can be explicitly addressed if the implicit operands are not the desired ones.

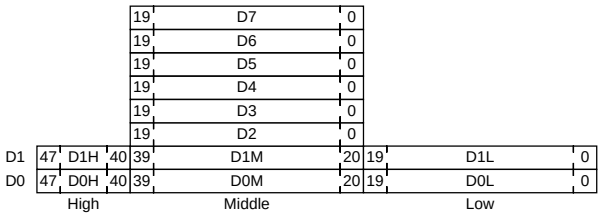


Figure 13. Data Register File

Address Generation Unit

Data operated on by the Arithmetic Unit is read from and restored to the Data Register File. Register file locations are directly addressed by register fields within the operate field of the instructions. For data transfers with the larger internal and external memories and registers, direct addressing can also be used, but indirect addressing by the Address Generation Unit is often faster and more program memory efficient. The Address Generator can sequentially produce two 20-bit addresses for the two bus transfers possible per cycle and post-modify the same two addresses in the same instruction cycle.

The indirect addresses generated can be linearly incremented or decremented, indexed, bit-reverse indexed or circular with an arbitrary modulus M. This is done in the Address Generation Unit by the Address ALU (AALU) and the Address Register File which is organized as in Figure 14. The next address is produced in a postmodify operation using the appropriate sum of the address register Ax with index register Ix and a compare with modulus register Mx. The five addressing modes in their assembler notation are:

(ax)	At the address in address register Ax with no postmodify operation
(ax)+	With a postincrement by one
(ax)-	With a postdecrement by one
(ax)+i	With a postincrement by the value in index register Ix
(ax)-i	With a postdecrement by the value in index register Ix

Note there is no indexing or circular addressing for the stack pointer SP. For M = Hex FFFFF the corresponding A register is incremented in a bit-reverse manner for doing the radix-2 FFT. For an N-point FFT the incrementing index register must be loaded with N/2.

The Address Register File is accessible on the Data Bus and can be used for general purpose registers. Further, they can be loaded with immediate data from the Program Data Bus.

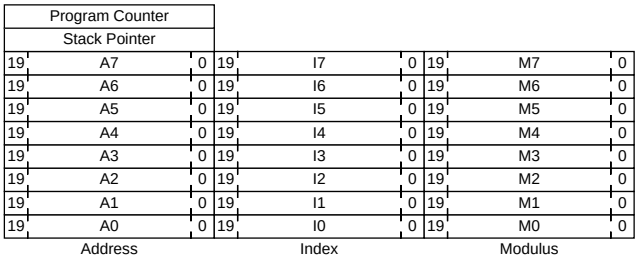


Figure 14. Data Register File

Memory

Internal

There are three internal on-chip memories, a 10k x 20-bit RAM, a 2k x 32-bit Program RAM and a 20k x 32-bit mask-program-

mable ROM. The 20-bit wide RAM is used exclusively as data memory, it transfers on the Data Bus and is addressed only from the Data Address Bus. It is always located in lowest memory address space starting at Hex 00000 up to 027FF. The other RAM and the ROM are 32-bits wide and can be used for both data and program memory. They are addressable by both the Program and Data Address Buses and are sources, and the RAM a destination, for transfers on both Data and Program Data Buses. When the Program RAM is written to the most significant 12 bits are loaded at the same time from the Data Bus Extension (DBX) register. When the Program RAM is read as data the DBX register is loaded with the most significant 12 bits of data. The DBX register can also be loaded or read as a general register with data in the least significant 12 bits.

The ROM is always at locations Hex E0000 to E4FFF in memory space on both Address Buses. The standard ZR38650 product has the ROM coded with the digital audio decoder functions and a bootstrap program for accepting commands from a host or loading an operating program into RAM from a byte-wide external ROM. Note that the external ROM data is on D[11-4]. The Program/Data RAM is always at locations Hex D0000 to D07FF in memory space on both Address Buses. It provides fast internal memory without the cost of a mask programmed internal ROM when the ZR38650 is used with an external byte-wide bootstrap ROM or host microcontroller.

All internal memories have a single port, but consistent with the buses, all can perform two complete operations per instruction cycle. The memories can operate in parallel provided buses are available. Each internal address bus has its own address space, but since the internal memories do not overlap and external memories share a common address bus, all memories can be considered to be in one address space as shown in Figure 15.

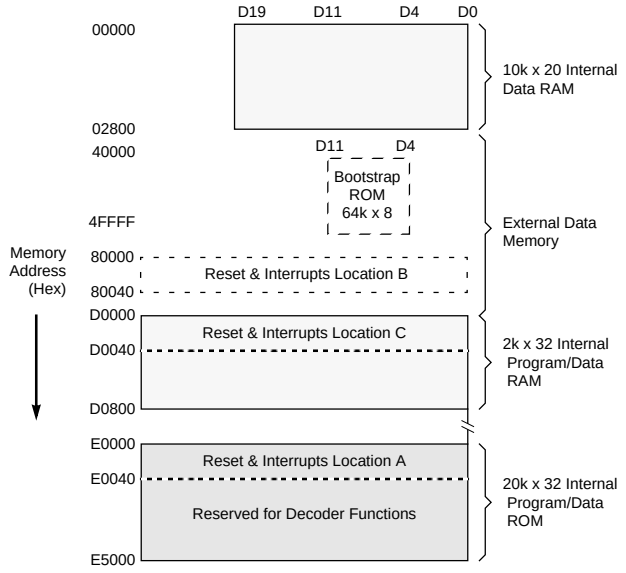


Figure 15. Program/Data Memory Map

External

Program/data memory is extended externally on the Parallel Port in the address spaces shown in Figure 15. Internal data buses are multiplexed into a single bus for external memory. Thus only one external data or instruction transfer can take place at a time. Also, only a single transfer can be made in each instruction cycle due to the slower external memories. This memory cycle-time can be lengthened by inserting wait-states to allow the use of lower-cost slow memories. The number of wait-states is determined by the CFG command so that external memory operations take one, three or seven instruction-cycle-times. The addresses shown are the internal 20-bit ones.

The optional external bootstrap ROM is 8-bits wide and connected to D[11-4]. Various widths of memory can be used for external RAM or ROM as required. The choices are 8, 16 or 32 bits. Data must be left justified on the data bus.

Reset and Interrupt Memory Locations

The reset and interrupt vectors occupy a reserved block of memory of 64 (Hex 40) locations. As shown in Figure 15 these can be located at the lowest portion of the on-chip 20k x 32-bit ROM or 2k x 32-bit RAM, or in external memory. This is selected by the MMAP pin and the MM and PM bits in the Mode Register as follows:

Table 16: Reset and Interrupt Start Locations

MMAP Pin	MM Bit	PM Bit	Reset & Interrupts Location	Start Address (Hex)
0	0	0	A - Internal ROM	E0000
0	1	0	B - External Memory	80000
1	X	0	B - External Memory	80000
X	X	1	C - Internal RAM	D0000

Program Sequence Unit

All processor operation is governed by the decoded instruction in the Instruction Register (IR). The control flow of the processor is the sequence of instructions that are presented to the IR. The Program Sequence Unit determines this flow by generating the program address to fetch instructions from program memory. This unit in the ZR38650 is a powerful address generator also, often producing a long sequence of operations with a minimum of program memory transfers. Examples of this are the RePeaT and LOOP instructions which allow repeated single and multiple instructions respectively with no instruction overhead. In addition to these instructions, major changes in the control flow are determined by the reset operation, interrupts, branches and subroutines to which the Program Sequence Unit responds.

Reset and Interrupt Operation

Operation of the processor starts with the system asserting the $\overline{\text{RESET}}$ pin. When $\overline{\text{RESET}}$ is asserted, the Mode Register is set to Hex 00038 and the Status register is set to Hex 00000. The serial port data registers are all cleared, as are the shift registers

Table 17: Reset and Interrupt Block Memory Map

Interrupt Number	Priority	Offset	Interrupt Type	Mask
0	1 (highest)	0x00	Reset Service Routine	no
1	2	0x04	ICE Interrupt Service Routine	no
2	3	0x08	Breakpoint Interrupt Service Routine	no
3	10	0x0C	HREG Interrupt Service Routine	yes
4	5	0x10	$\overline{\text{INT}}$ External Interrupt Service Routine	yes
5	6	0x14	Serial Port Group A Service Routine	yes
6		0x18	Reserved	
7	8	0x1C	Serial Port Group B Service Routine	yes
8		0x20	Reserved	
9	9	0x24	Serial Host Interrupt Service Routine	yes
10		0x28	Reserved	
11	7	0x2C	Audio Receiver Error Interrupt Service Routine	yes
12	4	0x30	Data FIFO Interrupt Service Routine	yes
13	11	0x34	Timer Service Routine	yes
14		0x38	Reserved	
15	16	0x3C	Jump to Software Interrupt Service Routine	no

for the output serial ports, and the serial port shift register pointers are reset. The modulus registers and the loop end registers are cleared. The program counter is set to Hex E0000 before unconditionally jumping to the beginning of the Reset and Interrupt block (shown in Table 17) to start executing the reset service routine. The complete service routine may be read from an external bootstrap device and in turn, executed.

Assertion of $\overline{\text{RESET}}$ does not affect the stack pointer, loop start register, loop and repeat count registers, address and index registers, internal RAM and the data registers.

The 15 hardware interrupts and the software Interrupt, have their corresponding vector addresses and the priority shown in Table 17. The priority reflects only the order of servicing when more than one request is pending, and does not determine whether or not a currently executing interrupt service routine will itself be interrupted. All interrupts are collectively disabled with the IE bit and individually enabled with their own mask bits in the auxiliary Interrupt Mask Register (IMR). Before an interrupt service routine is executed, the processor clears the IE bit to disable further interrupts and then pushes the return address and Status register contents on to the stack.

RePeaT and LOOP Instructions

The RePeaT instruction allows the single instruction that follows it to be repeated with no instruction overhead beyond the initial single RePeaT instruction. The Repeat Count (RC) register in the Program Sequence Unit allows up to 2^{20} repeated operations. Likewise, the LOOP instruction allows zero overhead for repeating multiple instruction sequences. The Loop Count (LC), the Loop Start (LS) and the Loop End (LE) registers implement this instruction. Loops may be nested up to four deep with these registers automatically being pushed on their individual stacks. The RC, LC, LS and LE can be a source or destination for general register data transfers, with each transfer in or out of the LE register being the appropriate push or pop operation respectively for their stacks.

Subroutines and Stack Operations

An operational stack is maintained in data memory to service context switches caused by changes in control flow. Interrupts as well as the PUSH, POP and Jump SubRoutine instruction macros use the stack. The Stack Pointer (SP) in the Address Generation Unit determines the stack location, usually in the internal Data or Program/Data RAM for highest speed.

Instruction Unit

Pipeline

Each instruction is fetched from program memory (either internal RAM or ROM), decoded in the Instruction register and finally executed. This three stage instruction pipeline takes a minimum of three instruction cycles, but is generally transparent to the user. The delayed branch instructions, however clearly exhibit this pipeline's delay. The pipeline is extended, in effect, whenever there is a requirement for multiple simultaneous accesses to a particular memory resource that cannot be resolved in a single cycle. This occurs, for example, when an instruction fetch and a dual data move all require access to the internal Program/Data RAM or ROM.

Instruction Set

Each of the instructions of the ZR38650 is a single word in length and except for program flow control instructions, all generally execute in a single cycle unless multiple external memory accesses are required. Much of the power of the processor lies in the parallel operations that go on within one instruction. Instructions are named for the dominant operation that executes, usually an Arithmetic Unit operation or a Program Sequence Unit operation. The instruction set names are summarized in Table 18 by the functional unit. Also listed are the instruction macros which the assembler generates from the basic instructions.

Table 18: Instruction Set Summary

Instructions				
Arithmetic Unit			Address Generation Unit	Program Sequence Unit
Arithmetic	Logic	Multiplier		
ABS	AND, ANDI	BFY	MOVE	Delayed Branch
ADD, ADDI	DEC	MADD		Conditional DB
ASHift, ASHI	INC	MNEG		Jump to SW Interrupt
CMP, CMPI	LSHift, LSHI	MSUB		LOOP
CMPA	OR, ORI	MUL, MULI		RePeaT
CMPZ	XOR, XORI	MULSU		
DIVS	NOP	MULUU		
DIVU	CLRBit			
MOVEMAX	SETBit			
MOVEMIN	TSTBit			
NEG				
NORM				
NORMMAX				
SUB				
MACROS				
CLeaR			POP	DO
			PUSH	Jump Conditional
				JuMP unconditional
				Jump SubRoutine
				ReTurn Interrupt
				ReTurn Subroutine

The instructions divide into eight classes or bit-pattern formats summarized in Table 19. It is here that the full power of the ZR38650 is most evident. The first three classes provide the full function of the Arithmetic Unit with its operate fields (Opcode and Operand), but also simultaneous parallel operations. The parallel operate fields (Parallel Opcode and Parallel Operand) specify single and double, direct and indirect transfers with the sources and destinations along with address generation modify operations. The Bit instructions are also parallel operations. The last five classes of instructions are for the large-field direct data transfers and program control.

For classes IV and V the possible source or destination register is a General Register. For parallel operations, the possible source and destination registers include the Auxiliary Registers as well as the General Registers.

Table 19: Instruction Class Summary Table

I. Single operand ALU operations with parallel transfer operations

Class Code	Op-code	Oper-and	Parallel Opcode	Parallel Operands

II. Two operand ALU operations with parallel transfer operations

Class	Opcode	Operands	Parallel Opcode	Parallel Operands

III. Three operand ALU operations with parallel transfer operations

Opcode	Operands	Parallel Opcode	Parallel Operands

IV. Load/Store direct

Class Code	Register	Address

V. Load Immediate

Class Code	Register	Data

VI. Conditional delayed branch

Class Code	Condition Code	Address

VII. Repeat immediate

Class Code	Data

VIII. Software jump to interrupt immediate

Class Code	Interrupt #

For parallel transfer operations there are the following six subclasses:

i	Register-to-register transfers, single
ii	Load register immediate (6-bits), single
iii	Register-to-memory transfers, single
iv	Memory-to-register transfers, single
v	Address modify, single and dual
vi	Single and dual transfers including memory-to-memory (through a register) and with optional address modify.

with the most powerful being the last which can do the following four types of sequential dual transfers:

First transfer	Second transfer
Data register to memory	Data register to memory
Data register to memory	Memory to data register
Memory to data register	Data register to memory
Memory to data register	Memory to data register

All memory references in this subclass are indirect and with possible address modification.

Input/Output Ports

Connections to external memory and peripherals are made through the input/output ports. There is a single 32-bit parallel data port, eight serial data ports and six single-bit general purpose I/O ports (GPIO). These last can be configured by the user as outputs or inputs.

Parallel Port

The ZR38650 parallel port works in two separate modes which are selected by the pin P/$\overline{M}$ at $\overline{RESET}$. It can work as a data parallel port which is used to load data, instructions and programs to the chip and read status and other information from the chip, or it may work as an external memory interface. The external memory interface consists of the 20-bit address bus A[19:0], the 32-bit bi-directional data bus D[31:0], and the control signals $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. The data parallel port interface consists of the 8-bit bi-directional data bus PP[7:0], and the control signals $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ERR, C/$\overline{D}$, RDY. The RDY, C/$\overline{D}$, and ERR signals are D[14:12] and PP[7:0] are D[11:4] also.

When controlling the external memory interface (P/$\overline{M}$ = 0), $\overline{CS}$ is asserted low whenever there is an access to external memory. $\overline{RD}$ is asserted during an external read cycle, and can be used as an output enable for memory. $\overline{WR}$ is asserted during an external write cycle and can be used as a write enable for memory.

The ZR38650 can generate wait-states for use with slow external memory using the WAIT field of the CFG command. In access cycles with wait-states, the timing relationship of the transitions of the memory interface signals remain the same as in a zero-wait cycle, but all are stretched by the specified number of instruction clock periods (1, 3 or 7).

During an instruction cycle in which there is no external data access, the $\overline{RD}$ and $\overline{WR}$ signals are not active. However, the address bus continues to be driven with the internal instruction fetch address.

When the parallel I/O interface is selected (P/$\overline{M}$ = 1), an internal FIFO is used to enable the host to write data in long bursts. The RDY output signal indicate when the FIFO is ready to receive more data (RDY = 1) or when the FIFO is almost full and not ready to accept data (RDY = 0). The ERR signal is an input to indicate for each data byte received if there is an error in the data. The C/$\overline{D}$ input signal distinguishes between input data and instructions or status which use the HREGIN/HREGOUT registers. When C/$\overline{D}$ = 1 transfers are a host command or reply status and therefore are written to the HREGIN register or read from the HREGOUT register. When C/$\overline{D}$ = 0 then all data from the host is written to the internal FIFO. $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are always inputs when P/$\overline{M}$ = 1. When $\overline{RESET}$ is asserted, the address and data buses and control signals $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are all set to a high-impedance state.

Serial DAC and ADC Ports

The serial ports are flexible on the ZR38650 to serve a wide variety of applications and peripheral devices. The three ADC inputs and four DAC outputs may be variously grouped to share two sets of common control signals, each being a master or a slave. Other selections are word or frame synchronization, frame size and either 16, 18, 20 or 24-bit word transfers. A master clock output which can be generated internally and two group programmable rate clocks. The I^2S format, the frame-less time-division-multiplex (TDM) format and the LSB justified frame of the EIAJ format are all supported.

Ports A, E, F are always ADC data inputs, while B, C, D are always DAC data outputs. Port G can be a DAC data output or the S/PDIF transmitter output. The ports may be configured in two groups with shared clocking: all inputs and all outputs, or as two groups with one of the inputs in the outputs group. This selection is made by the AB bit in the Mode register. The B group is unique in that when operating as a source to DACs, its clock outputs can also be derived from an externally supplied master clock input (SCKIN).

Transfers are on the positive- or negative-going edge of the bit-rate clocks (SCKA and SCKB) with the most significant bit being shifted first into or out of the double buffered shift registers. Word boundaries are signaled by a single-bit-duration frame signal (FSA and FSB) for each word or an alternating word signal (WSA and WSB) indicating left or right channel, even or odd word. The signal type is selected independently for each group as is the word length of 16, 18, 20 or 24 bits and the frame size of 16 to 256 bits per frame. The Word Select bits in the Status register reflect when the left or right channel is being transferred for each group. The WS/FS signals maybe advanced by one or more bit intervals for the non-I^2S format. Completed frame transfers for each group are indicated to the processor by a vectored interrupt when individually enabled. An exception is for TDM where there is an interrupt for each word within a frame.

Each group can be a source or a slave as selected in the auxiliary Serial Port Mode register. When a source, the clock rates are independently programmable sub-multiples of the internally generated master clock. The B group clocks can come from the external master clock input (SCKIN) as well. If this input is not used the pin may be selected as an output for the internally generated master clock.

S/PDIF Serial Ports

The SPFRX signal is the single-wire input to the S/PDIF digital audio receiver. In use, the Audio PLL locks on the incoming SPFRX bitstream to determine the audio master clock SCKIN and to recover the digital input data.

The serial output Port G is the single-wire S/PDIF digital audio transmitter output when not used as a DAC data output. Its SDG/SPFTX signal is used to output S/PDIF encoded data for decoding in other peripheral devices.

Table 20: ADC and DAC Serial Ports Function Summary

Function	A Group	B Group
Grouping: AB = 0	3 Inputs (A, E, F)	4 Outputs (B, C, D, G)
Grouping: AB = 1	2 Inputs (A, E)	1 Input (F), 4 Outputs (B, C, D, G)
Word size	16, 18, 20, 24 bits	16, 18, 20, 24 bits
Frame size (bits/frame)	16, 24, 32, 64, 128, 192, 193, 256	16, 24, 32, 64, 128, 192, 193, 256
Synchronization	Word or Frame	Word or Frame
Source and slave clocking modes	Yes	Yes
Latching on rising or falling edge of clock	Yes	Yes (when port F belongs to Port group B)
Transmitting data on rising or falling edge of clock	Yes	Yes
External master clock input	No	Yes
Internal master clock output	Yes	Yes
Internal clock scaler	12-bit Counter	12-bit Counter
I^2S format	Yes	Yes
TDM format	Yes	Yes
Left/Right justified formats	Yes	Yes

General Purpose Ports

Six single-bit general purpose ports may be individually selected as an input or output in the GPIOC auxiliary register. If configured as an input, its sampled state may be read in the GPIO general register, or if an output, its state may be set by writing to the GPIO register.

System Interface

The system interface consists of all external signal functions other than Input/Output Ports plus the general and auxiliary registers which are associated with functional units and I/O operation.

General Registers

In addition to the primary data flow and control flow of instructions between functional units on the two data buses, there is the secondary control flow between the general and auxiliary registers for initialization and maintenance of operation. The following general registers are all directly addressable on the Data Bus for register-to-register, memory-to-register or register-to-memory parallel transfers.

Table 21: The General Registers

Name	Bits	Description
D0-7	48	Data Registers 0-7
A0-1	20	Address Registers 0-7
M0-7	20	Modulus Registers 0-7
I0-7	20	Index Registers 0-7
D0L	20	Data Register 0 Low
D0M	20	Data Register 0 Middle
D0H	8	Data Register 0 High
SRG_SPF	20	S/PDIF Transmitter Data Register
D1L	20	Data Register 1 Low
D1M	20	Data Register 1 Middle
D1H	8	Data Register 1 High

Table 21: The General Registers (Continued)

Name	Bits	Description
RC	20	Repeat Count Register
LC	20	Loop Count Register. Stack of four.
LS	20	Loop Start Register. Stack of four.
LE	20	Loop End Register. Stack of four.
STATUS	20	Status Register
MODE	20	Mode Register
PC	20	Program Counter
SP	20	Stack Pointer
Z	20	Z Register for JSR and JSRQ
SRA	20	Serial Port A Data Register
SRB	20	Serial Port B Data Register
SRC	20	Serial Port C Data Register
SRD	20	Serial Port D Data Register
PACKREG	20	Pack Register
DBX	12	Data Bus Extension Register
DS	2	Data Shifter
IE	1	Interrupt Enable
SRE	20	Serial Port E Data Register
SRF	20	Serial Port F Data Register
GPIO	6	General Purpose I/O Data Register
WAIT	2	External Memory Wait-states

Some of the more important General Registers are described next in detail.

Mode Register

The Mode register is a source or destination register containing 18 fields that define the basic processor configuration. They tend to be set once at initialization and not change. The interrupt enable (IE), the wait-state selection (WAIT), and the register file data shifter (DS) bits that may change during processing are also individually addressable as registers. The IE, IM, AM and BM bits are also accessible in the Interrupt Mask Register (IMR). The Mode register is defined as shown below.

MODE

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IE	IM	AM	BM	0	0	PM	CRCR	WFA	WBA	AB	AW	BW	MM	WAIT		MS	DS		SD

IE	**Interrupt Enable** when set enables all unmasked interrupts. When cleared, disables all interrupts.
IM	**INT Mask** when set enables the external interrupt input.
AM	**A Mask** when set enables the A Group serial ports interrupt.
BM	**B Mask** when set enables the B Group serial ports interrupt.
PM	**Program Memory** selection. When set the Reset and Interrupt Block is located in internal RAM.
CRCR	**CRC R**eset register flag. A transition from '0' to '1' of this flag resets the CRCC register to zero in the next cycle. Cleared at $\overline{\text{RESET}}$.
WFA	**Word/Frame A** group serial port synchronization mode bit. Word synchronization when set, Frame synchronization when cleared.
WFB	**Word/Frame B** group serial port synchronization mode bit. Word synchronization when set, Frame synchronization when cleared.
AB	**A/B** groupings of serial ports. When set, A Group is ports A, E and B Group is ports B, C, D, F, G. When cleared, A group is port A, E, F and B Group is ports B, C, D & G.
AW	**A Word** precision. Together with the AW1 bit in the SPMODE register defines the precision of group A data words. For [AW,AW1]: 0,0 = 20 bit operation, 0,1 = 18 bit operation, 1,0 = 16 bit operation, 1,1 = 24 bit operation.
BW	**B Word** precision. Together with the BW1 bit in the SPMODE register defines the precision of group B data words. For [BW,BW1]: 0,0 = 20 bit operation, 0,1 = 18 bit operation, 1,0 = 16 bit operation, 1,1 = 24 bit operation.
MM	**Memory Map**. Together with the MMAP pin and PM bit determine the Reset and Interrupt Block start location. Cleared at $\overline{\text{RESET}}$.
WAIT	**Wait-state** selection for external memory. 0 = No wait-states, 1 = One wait-state, 2 = Three wait-states, 3 = Seven wait-states (a total of eight instruction cycles for an external memory operation).
MS	**Multiplier Shifter.** When set specifies 1-bit left arithmetic shift on multiplier output, when cleared there is no shifting.
DS	**Data Shifter** on transfers from the Data Register File to memory. 00 = No shift, 01 = Left shift by one, 10 = Left shift by two, 11 = Right shift by one.
SD	**Shift Direction** on the barrel shifter. When cleared a positive shift code corresponds to a left shift, when set a positive shift code corresponds to a right shift.

Status Register

The Status register is a source or destination register containing fields that reflect the state of the processor following each instruction cycle. They affect the conditional program control of the processor. The least significant 8 bits reflect arithmetic and logical operation results from the ALU, multiplier, barrel shifter or on transfers that involve scaling or limiting. The other eight involve word identification on the serial and host ports, status of the PLLs and configuration of the chip. The Status Register is defined below.

STATUS

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PLOCKA	P/$\overline{\text{M}}$	SIE	PLOCKD	0	HWR	WSA	WSB	Q	SS	SL	SV	V	C	N	Z

PLOCKA	**Audio PLL Lock Status**. Setting RSTAUD resets the audio PLL. This clears PLOCKA indicating that the audio PLL is not locked. When the audio PLL is locked on the acquired frequency it sets PLOCKA again. Read only.
P/$\overline{\text{M}}$	**Parallel port/Memory** status. The P/$\overline{\text{M}}$ status flag reflects this pin's state at $\overline{\text{RESET}}$ indicating whether the parallel port is configured for parallel I/O or memory. Read only.
SIE	**Store Interrupt Enable** status Flag. This flag stores the IE value in the mode register upon entering an interrupt processing sequence, simultaneously with resetting IE flag. Read only.
PLOCKD	**DSP PLL Lock Status**. Setting RSTDSP resets the DSP PLL This clears PLOCKD indicating that the PLL is not locked. When the DSP PLL is locked on the acquired frequency it sets PLOCKD again. Read only.
HWR	**Host Write** indicated the host interrupt is due to a write operation to the Host register. Read only.

WSA	**Word Select** A bit indicates Left channel data is being input if cleared or Right channel data if set, on the A Group serial ports.
WSB	**Word Select B** bit indicates Left channel data is being output if cleared or Right channel data if set, on the B Group serial ports.
Q	**Quotient** bit is used with the divide iteration instructions.
SS	**Sticky Scaling** bit is set if any data transferred through the Data Shifter has a magnitude of greater than 0.25. A typical use is to indicate the potential for overflow in the next pass of an FFT. It is cleared by a $\overline{\text{RESET}}$ or by an explicit instruction to clear it.
SL	**Sticky Limiting** bit is set whenever limiting takes place in the Arithmetic Unit or during a data transfer through the Data Shifter. It is cleared by a $\overline{\text{RESET}}$ or by an explicit instruction to clear it.
SV	**Sticky Overflow** bit is set whenever the Overflow bit is set except for the compare instructions. It is cleared by a $\overline{\text{RESET}}$ or by an explicit instruction to clear it.
V	**Overflow** bit is set if an overflow results from any operation in the Arithmetic Unit. Overflow is determined if any number can not be properly represented in its destination register.
C	**Carry** bit is set if a carry results from an addition or a borrow results from a subtraction in the ALU, or results from shifts in the barrel shifter of the Arithmetic Unit.
N	**Negative** bit is set if the most significant bit of the destination register is set, otherwise it is cleared.
Z	**Zero** bit is set if the entire result of an Arithmetic Unit operation in its destination register is zero.

DBX Register

The data bus extension register (DBX) is a 12-bit register that permits full use of the 32-bit internal memories for data. When reading data from 32-bit wide internal memory to a 20-bit register, the least significant 20 bits are loaded into the destination register. The most significant 12 bits are loaded into the DBX register. When writing data from a 20-bit register to the 32-bit internal RAM, the least significant 20 bits are driven by the specified source register, while the most significant 12 bits are driven by the DBX register. When the DBX is specified as the destination or source in a transfer, the least significant 12 bits are read into or loaded from the DBX.

Auxiliary Registers

In addition to the primary data flow and control flow of instructions between functional units on the two data buses, there is the secondary control flow with the general and auxiliary registers for initialization and maintenance operations. The auxiliary registers are accessed by register-to-register parallel transfers only.

Table 22: The Auxiliary Registers

Name	Bits	Description
HREGOUT	8	Host Register Output
HREGIN	8	Host Register Input (RO)
ISR	1	ICE host Status Register
IRR	20	ICE host Response Register
BKP1	20	Instruction address Breakpoint register 1
BKP2	20	Instruction address Breakpoint register 2
BKP3	20	Data address Breakpoint register 3
BCT1	20	Breakpoint 1 Counter
BCT2	20	Breakpoint 2 Counter
BCR	4	Breakpoint Control Register
BSR	3	Breakpoint Status Register
IMR	20	Interrupt Mask Register
GPIOC	6	General Purpose I/O Control register
SPMODE	20	Serial Ports Mode register
AUDM	13	Audio PLL Multiply register
SPAS	12	Serial Ports A group Scaler register
SPBS	12	Serial Ports B group Scaler register
SPITX/SCTX	8	Serial host Interface Transmit register, SPI/Z2C

Table 22: The Auxiliary Registers (Continued)

Name	Bits	Description
SPIRX/SCRX	8	Serial host Interface Receive register, SPI/Z2C (RO)
SPIMO-DE/SCMODE	2	Serial host Interface Mode register, SPI/Z2C
SPISTAT/SC STAT	7	Serial host Interface Status register, SPI or Z2C (RO)
SPDEL	12	Serial port bit Delay A and B
SPFAUD	7	S/PDIF transmitter auxiliary Audio register
SPFSTT	1	S/PDIF Transmitter Status register (RO)
SPFCHS	20	S/PDIF transmitter Channel Status register
DSPDM	14	DSP PLL Divide/Multiply register
AUDD	13	Audio PLL Divide register
ICR	13	ICE Command Register (RO)
IDR	20	ICE Data Register (RO)
TESTMODE	12	Test Mode data register
SPRXDAT	20	S/PDIF Receiver Data register (RO)
SPRXAUX	6	S/PDIF Receiver Auxiliary register (RO)
SPRXCHS	20	S/PDIF Receiver Channel Status (RO)
SPRXSTT	8	S/PDIF Receiver Status register (RO)
SPRXMODE	4	S/PDIF Receiver Mode register
CRCC	16	Cyclic Redundancy Check Code register
CLKMODE	7	Clock Mode register.
DFIFO	20	Parallel port Data FIFO register (RO)
DFFCNT	20	Parallel port Data FIFO counter (RO)
TIMER	18	Timer register
Z2CADR	7	Z2C Address

One of the more generally important Auxiliary Registers is described next in detail.

Serial Ports Mode Register

The Serial Ports Mode register is an auxiliary source or destination register containing fields that determine the serial ports operation and configuration. The fields are defined below.

SPMODE

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPFEN	0	0	0	0	BW1	AW1	CB	MB	MA	TB	TA	CPB	CPA	FRB			FRA		

SPFEN	**S/PDIF Output Enable**. Setting SPFEN enables Port G as the S/PDIF output. Clearing it makes Port G serial I/O.
BW1	**B Word** precision. Together with the BW bit in the MODE register defines the precision of group B data words. For [BW,BW1]: 0,0 = 20 bit operation, 0,1 = 18 bit operation, 1,0 = 16 bit operation, 1,1 = 24 bit operation.
AW1	**A Word** precision. Together with the AW bit in the MODE register defines the precision of group A data words. For [AW,AW1]: 0,0 = 20 bit operation, 0,1 = 18 bit operation, 1,0 = 16 bit operation, 1,1 = 24 bit operation.
CB	**Clock B** source. Selects the group B clock source. Setting CB selects the Audio PLL and SCKIN is an output. Clearing CB selects SCKIN as the group B clock.
MB	**Master B.** Setting MB makes group B outputs masters with SCKB an output. Clearing MB makes group B slaves with SCKB an input.
MA	**Master A.** Setting MA makes group A inputs masters with SCKA an output. Clearing MA makes group A slaves with SCKA an input.
TB	**TDM B.** Setting TB selects TDM (Time Division Multiplexing) mode for group B outputs with a frame size determined by the FRB field. Clearing TB disables the TDM mode.
TA	**TDM A.** Setting TA selects TDM (Time Division Multiplexing) mode for group A inputs with a frame size determined by the FRA field. Clearing TA disables the TDM mode.
CPB	**Clock Polarity B** determines the group B serial outputs clock polarity. When CPB is set, data is output with the rising edge of the clock. When CPB is cleared, data is output with the falling edge of the clock.
CPA	**Clock Polarity A** determines the group A serial inputs clock polarity. When CPA is set, data is input on the falling edge of the clock. When CPA is cleared, data is input on the rising edge of the clock.
FRB	**Frame B** size. Determines the frame size of the group B serial output ports in master mode: 0 = 16 bits, 1 = 32 bits, 2 = 64 bits, 3 = 128 bits, 4 = 192 bits, 5 = 256 bits, 6 = 193 bits, 7 = 24 bits.
FRA	**Frame A** size. Determines the frame size of the group A serial input ports in master mode: 0 = 16 bits, 1 = 32 bits, 2 = 64 bits, 3 = 128 bits, 4 = 192 bits, 5 = 256 bits, 6 = 193 bits, 7 = 24 bits.

Timer

The ZR38650 timer is an 18-bit programmable counter auxiliary register. Once loaded, it counts down at the instruction cycle rate of f_{CLKOUT} or $f_{DSP}/2$. At a count of one it issues an interrupt and reloads to continue counting the next interval.

Serial Host Interface

The serial host interface provides a low-cost, low-bandwidth interface to a host processor for down-loading RAM programs and basic operating commands. The ZR38650 always operates as a slave and transfers are internal program interrupt driven. There are the two industry standard signals and protocols supported, SPI (Serial Peripheral Interface) and Z2C (Zoran Two Conductor interface). Transfers are bit-serial with parallel eight-bit data registers. The standard function ROM can accept commands or down-load RAM program through the serial host interface if it does not find an external byte-wide EPROM at Reset time.

The serial host signals and protocol are determined by SPI/$\overline{Z2C}$, the state of the SDB pin at Reset. SPI/$\overline{Z2C}$ = 0 for Z2C if SDB is tied to a pull-down resistor. SPI/$\overline{Z2C}$ = 1 for SPI if SDB relies on the internal pull-up resistor or uses an external one. The shared interface signals are data input (SI), data output or slave data (SO/SDA), serial clock input (SCK/SCL) and slave select ($\overline{SS}$), where SDA and SCL are for the two-wire Z2C interface.

Four auxiliary registers receive data (SPIRX/SCRX), transmit data (SPITX/SCTX), govern operation (SPIMODE/SCMODE) and provide control flags (SPISTAT/SCSTAT) for the interrupt driven operation with the two protocols. An additional auxiliary register Z2CADR holds the seven-bit Z2C address determined at Reset from the SI, $\overline{SS}$, SDD and SDC pins for Z2CADR[5,4,1,0] respectively. Z2CADR[6,3,2] are always zero.

In SPI operation, transfers are full-duplex with a single byte transmitted to the host for every byte received. The polarity of the SCK clock is defined by the SCKP bit in the SPIMODE register which is determined by the state of SDG/SPFTX pin at Reset. When SCKP = 1 the output data on the SO signal changes after the falling edge of SCK and the input data on the SI line is sampled on the rising edge of SCK. When SCKP = 0 the output data on SO line changes after the rising edge of SCK and input data on the SI line is sampled on the falling edge of SCK. When $\overline{SS}$ is not asserted, the SCK line should be at the high level if SCKP = 1 and at the low level if SCKP = 0. The

SCKP bit in the SPIMODE register is set at Reset if the SDG/SPFTX pin is tied to a pull-up resistor, or cleared if the pin is pulled down.

In Z2C operation, byte transfers are half-duplex with the ZR38650 either a slave-receiver or slave-transmitter. Figure 16 shows a normal read operation by the host master. Normal operation is in the alternating single-byte transmit/receive protocol, but the transmit-only protocol can be used to speed program downloading. The 400 kbit/second fast mode transfer rate is supported as well as standard mode of 100 kbit/second.

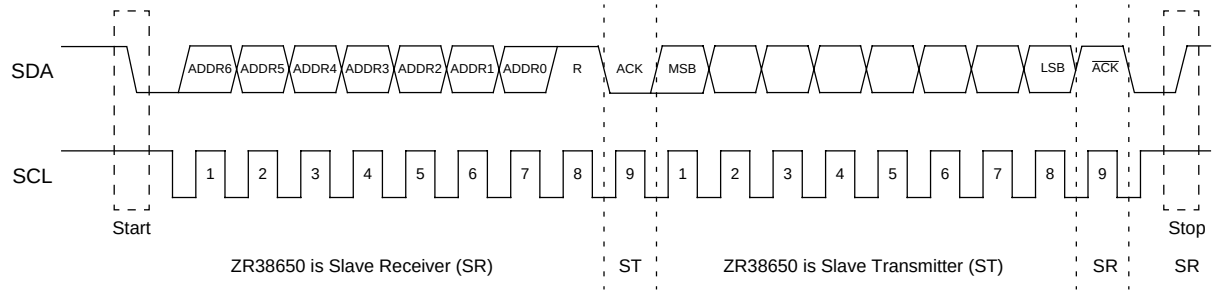


Figure 16. A Z2C Host Interface Read Operation by a Master Host

In Circuit Emulation Interface

The ZR38650's In Circuit Emulation (ICE) capability for both hardware and software debugging is provided through four test pins (TDI, TDO, TCK, TMS) using a standard JTAG interface. This interface is serviced by routines in the on-chip Program/Data ROM and the highest priority interrupt. This provides register and memory read and set commands for hardware debugging. Three breakpoint address-detection registers and two count registers with interrupt additionally provide for real-time program debugging capability in the ICE.

Reset and Initialization

The processor can be reset only by asserting the $\overline{\text{RESET}}$ signal input pin externally. On the initial power-up it must be asserted for a minimum of 160 clock cycles with proper supply voltage operating conditions. Operation starts 16 cycles after the rising edge. After power-up, any reset must be asserted for at least 16 clock cycles but less than 128 clock cycles if there is no need to reset the PLLs. If the user wishes to reset the PLLs the reset signal must be active for at least 160 clock cycles. Operation starts 16 cycles after the rising edge at the selected reset service routine location in memory. The processor will not, however, accept a serial host command and return a response until 200 instruction cycles have elapsed. In order for the decoder to operate correctly, the following sequence of commands should be supplied: PLLTAB, PLLCFG, CFG, AC-3 (if AC-3 mode is required) UNMUTE.

The states of pins after reset that are tri-state or can be either input or output are given in Table 23.

External Interrupts

The external interrupt input signal $\overline{\text{INT}}$ is edge-sensitive and must remain asserted for two clock cycles to set the internal INT flag. This flag is cleared as the interrupt service routine starts so that any new interrupt condition must allow $\overline{\text{INT}}$ to go high and then low again for another interrupt to be generated.

Oscillator and Clock Inputs

The XTI and XTO signals jointly supply the oscillator clock f_{XTI} either as an input from a TTL system clock or as the crystal connection to enable the internal oscillator. The maximum frequency f_{XTI} is 40 MHz and the minimum is 4 MHz. An internal phase-locked-loop (PLL) generates from this a DSP core clock f_{DSP}. This internal DSP clock can be in the range of 4-100 MHz. (For low f_{DSP} frequencies, care should be taken because the SPI data rate is slowed down proportionally). After $\overline{\text{RESET}}$ but before PLL lock, $f_{DSP} = f_{XTI}$.

The external clock is applied to XTI, while the external crystal connection is as shown in Figure 17. A parallel-resonant fundamental-mode crystal should be used with two 20-pF capacitors.

Signal Description Summary

Table 23 summarizes information about all pins on the ZR38650. During reset all T type pins are tri-state and I/O pins are inputs. Pin states immediately after reset are shown in the Reset State column. All unused input pins should be connected to V_{DD} if active low, or GND if active high unless internally pulled low. Unused tri-state pins should be resistively pulled-up to VDD. Unused outputs should be left unconnected.

Internal pull-downs are 50 µA maximum current sinks and pull-ups are 50 µA maximum current sources, both are connected only when configured as an input. The pull-downs on D[31:15] and D[3:0] are connected only when P/$\overline{M}$ = 1.

Table 23: ZR38650 Signal Description Summary

Signal Name	Number of Pins	Type [1]	Reset State [1]	Internally Pulled	Description
Parallel Port (56)					
A[19:0]	20	O/T	O	-	Address bus of parallel port
D[31:15]	17	I/O/T	I	Down [2]	Data bus of parallel port when selected for external memory (P/$\overline{M}$ = 0)
D14/RDY	1	I/O/T or O	I or O	-	Data bus (P/$\overline{M}$ = 0) or Ready output signal of parallel port when selected for parallel I/O (P/$\overline{M}$ = 1)
D13/ C/$\overline{D}$	1	I/O/T or I	I	-	Data bus (P/$\overline{M}$ = 0) or Command/Data select input of parallel port when selected for parallel I/O (P/$\overline{M}$ = 1)
D12/ERR	1	I/O/T or I	I	-	Data bus (P/$\overline{M}$ = 0) or Error input signal of parallel port when selected for parallel I/O (P/$\overline{M}$ = 1)
D[11:4]/PP[7:0]	8	I/O/T	I	-	Data bus of parallel port when selected for external memory (P/$\overline{M}$ = 0) or Parallel Port I/O (P/$\overline{M}$ = 1)
D[3:0]	4	I/O/T	I	Down [2]	Data bus of parallel port when selected for external memory (P/$\overline{M}$ = 0)
$\overline{CS}$	1	I/O/T	O or I	Up	Chip Select output for external memory or Chip Select input for parallel I/O
$\overline{RD}$	1	I/O/T	O or I	Up	Read enable output for external memory or Read enable input for parallel I/O
$\overline{WR}$	1	I/O/T	O or I	Up	Write enable output for external memory or Write enable input for parallel I/O
P/$\overline{M}$	1	I	I	-	Parallel I/O or Memory select for parallel port. Determined at time of $\overline{RESET}$.
Serial Ports (13)					
SPFRX	1	I	I	-	S/PDIF Receiver input port
SDA	1	I	I	-	Serial Data input. Port A.
SDE	1	I	I	-	Serial Data input. Port E.
SDF	1	I	I	-	Serial Data input. Port F.
WSA/FSA	1	I/O	I	Down	Word Select or Frame Synchronization for input ports. An output when a master, an input when a slave.
SCKA	1	I/O	I	Down	Serial Clock for input ports. An output when a master, an input when a slave.
SDB	1	O	O	Up	Serial left and right Data output. Port B. Also, at $\overline{RESET}$ defines SPI/$\overline{Z2C}$ for host serial interface.
SDC	1	O	O	Up	Serial left and right surround Data output. Port C. Also, at $\overline{RESET}$ defines $\overline{Z2CADR[0]}$ of Z2C address.
SDD	1	O	O	Up	Serial center and sub-woofer Data output. Port D. Also, at $\overline{RESET}$ defines $\overline{Z2CADR[1]}$ of Z2C address.
SDG/SPFTX	1	O	O	-	Serial Data output. Port G or S/PDIF Transmitter port. Also, at $\overline{RESET}$ defines the SCKP value.
WSB/FSB	1	I/O	I	Down	Word Select or Frame Synchronization for output ports. An output when a master, an input when a slave.
SCKB	1	I/O	I	Down	Serial Clock for output ports. An output when a master, an input when a slave.
SCKIN	1	I/O	I	-	Serial master Clock output or master clock Input for output ports

Table 23: ZR38650 Signal Description Summary (Continued)

Signal Name	Number of Pins	Type [1]	Reset State [1]	Internally Pulled	Description
General Purpose Ports (6)					
$\overline{\text{MUTE}}$/GPIO5	1	I or I/O	I	-	Mute input signal or can be programmed as General Purpose Input/Output 5
GPIO4	1	I/O	I	-	Can be programmed as General Purpose Input/Output 4
GPIO3	1	I/O	I	-	Can be programmed as General Purpose Input/Output 3
GPIO2	1	I/O	I	-	Can be programmed as General Purpose Input/Output 2
ERROR/GPIO1	1	I/O	I	-	Error output signal or can be programmed as General Purpose Input/Output 1
$\overline{\text{DREQ}}$/GPIO0	1	I/O	I	-	Data Request output signal or can be programmed as General Purpose Input/Output 0
Serial Host Interface (4)					
SI	1	I	I	-	Host Serial interface data Input. Also, at $\overline{\text{RESET}}$ defines Z2CADR[5] of Z2C address.
SO/SDA	1	I/O/T	T	-	SPI host Serial interface data Output or Serial Data for Z2C
SCK/SCL	1	I	I	-	SPI host Serial interface Clock input or Slave Clock input for Z2C
$\overline{\text{SS}}$	1	I	I	-	SPI host serial interface Slave Select input. Also, at $\overline{\text{RESET}}$ defines Z2CADR[4] of Z2C address.
ICE Interface (4)					
TDI	1	I	I	-	ICE Test interface Data Input
TDO	1	O/T	T	-	ICE Test interface Data Output
TCK	1	I	I	-	ICE Test interface Clock input
TMS	1	I	I	-	ICE Test interface Mode Select
System Interface (8)					
$\overline{\text{INT}}$	1	I	I	-	External Interrupt request input
$\overline{\text{RESET}}$	1	I	I	-	Reset input to start operation in known state
MMAP	1	I	I	Down	Determines location on Memory Map of reset and interrupt block
XTI	1	I	I	-	External system clock Input or connection to external crystal, at frequency f_{XTI}
XTO	1	O	-	-	Output connection to external crystal
CLKOUT	1	O	O	-	Clock Output from the ZR38650 at frequency $f_{DSP}/2$
BYPASS	1	I	I	-	Bypass internal DSP core PLL to use external system clock input on XTI
FLTCAP	1	I	-	-	External Filter Capacitor connection for PLL. A value of 47nF is recommended.
Power (53)					
VDD	16	Power	-	-	+3.3 volt power supply
VDDA	1	Power	-	-	+3.3 volt power supply, Analog for PLL
GND	25	Power	-	-	Power supply Ground
GNDA	1	Power	-	-	Power supply Ground, Analog for PLL
nc	10	NC	-	-	No connection
Total (144)					

1. O = Output, I = Input, T = Tri-state.
2. When P/$\overline{\text{M}}$ = 1.

TYPICAL CONFIGURATIONS

Stand Alone (No Host)

Figure 17 shows a ZR38650 in a typical stand-alone configuration without a host microprocessor but with various optional external memories. For the lowest cost, only a byte-wide ROM need be used for loading a developer-written program that governs the decoder operation. The standard ZR38650 has a Reset bootstrap loading routine in its internal ROM that reads the program/data from the external byte-wide ROM at the address location Hex 40000. The boot-strap recognizes the external ROM rather than waiting for commands from a host that does not exist in this configuration.

An alternative is to use the optional 32-bit wide program/data ROM shown. With the MMAP pin pulled-up, reset execution will start directly from this external ROM at the address location Hex 8000 and can continue there with the developer-written program.

The optional program/data RAM can be used in any configuration, including with hosts, for additional 32-bit directly executable program (with data) memory space. If needed only for data then this RAM may be only 16 or 24 bits wide.

The compressed data stream is input through the internal S/PDIF receiver which also acts as a clock master for the output DACs. This master clock can be selected to be 256 x SR or 384 x SR. The internal clock divider on the ZR38650 generates the clocking for the three slave DACs that provide the six-channel audio output.

Note that the PLL capacitor connected to FLTCAP, and the bypass capacitors on VDDA, should all be mounted close to the ZR38650 package with short leads over the GNDA analog ground plane, using normal good design practice for high frequency mixed-signal circuits.

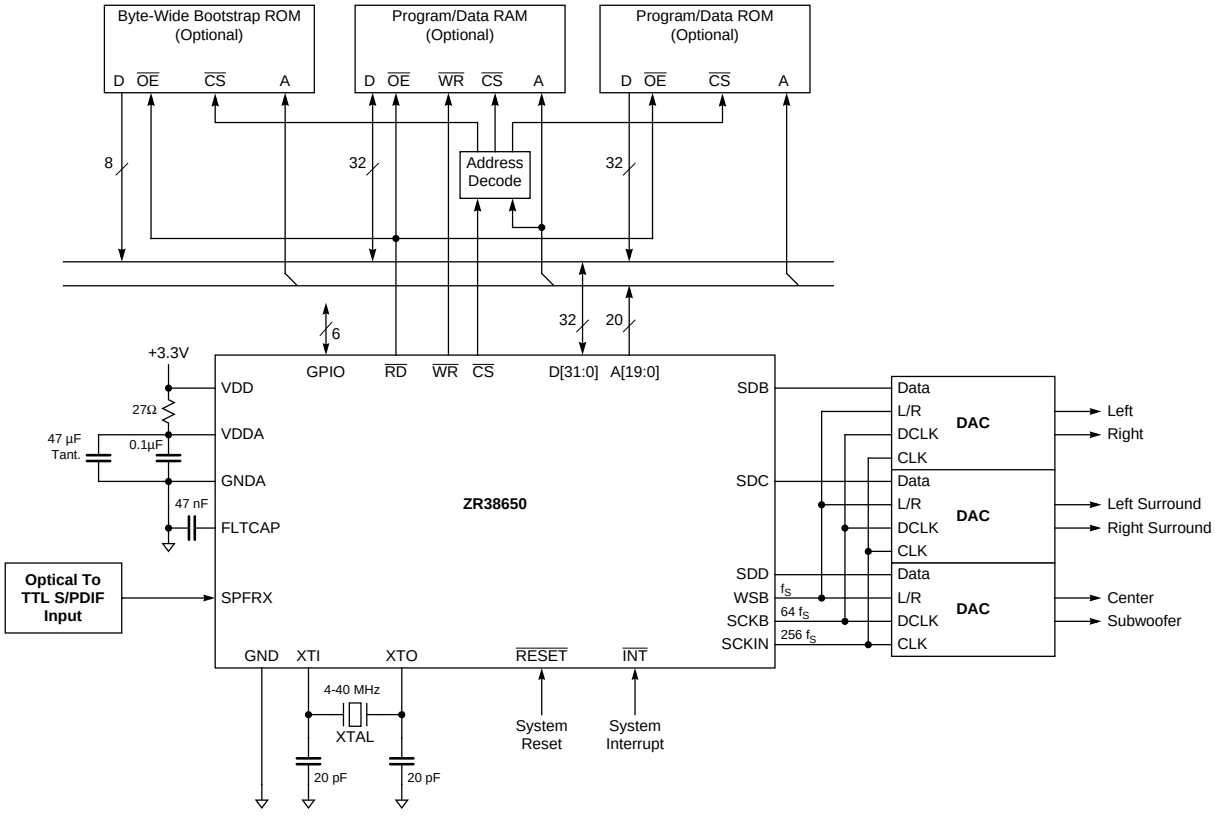


Figure 17. Typical ZR38650 Stand-Alone Configuration With External Memories

Serial Host And Serial Data

Figure 18 and Figure 19 show a ZR38650 in typical system configurations with a host controller. At Reset time the internal ROM bootstrap will check for the byte-wide external ROM. A resistive pull-up on any one data line D[11-4] assures that an external ROM will not be found. Not finding that, it will then expect to receive program commands from the host through the selected serial connection. Note the optional pull-up on SDB in Figure 18 to select the SPI and the pull-down for the Z2C in Figure 19. The resistive pull-ups/pull-downs on SI, $\overline{SS}$, SDC and SDD in Figure 19 determine the ZR38650's Z2C address at Reset time.

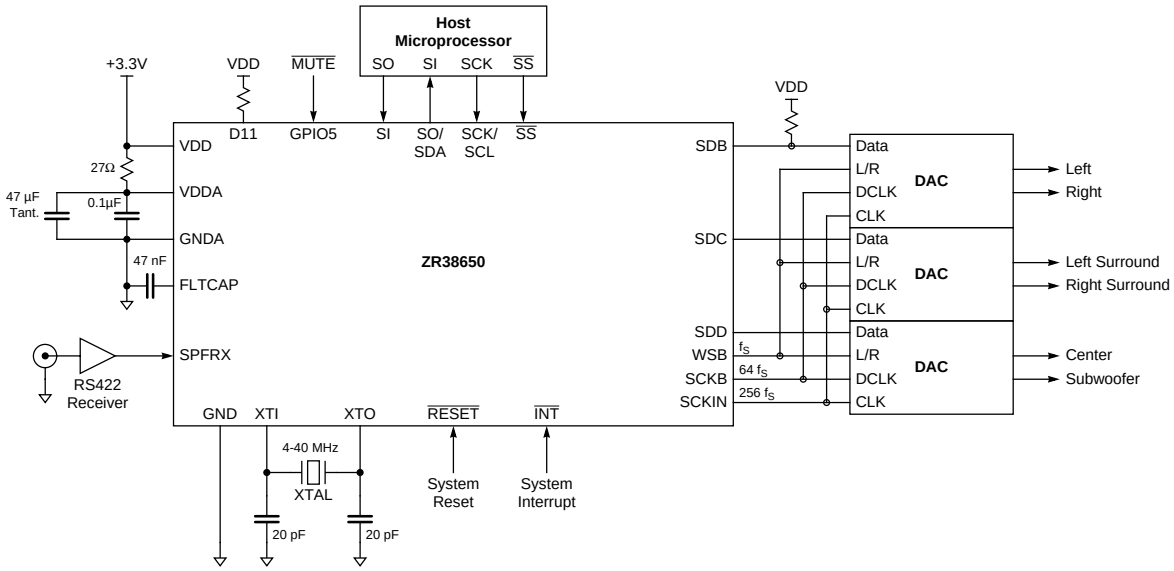


Figure 18. ZR38650 Typical Configuration With The SPI Serial Interface To A Host Controller

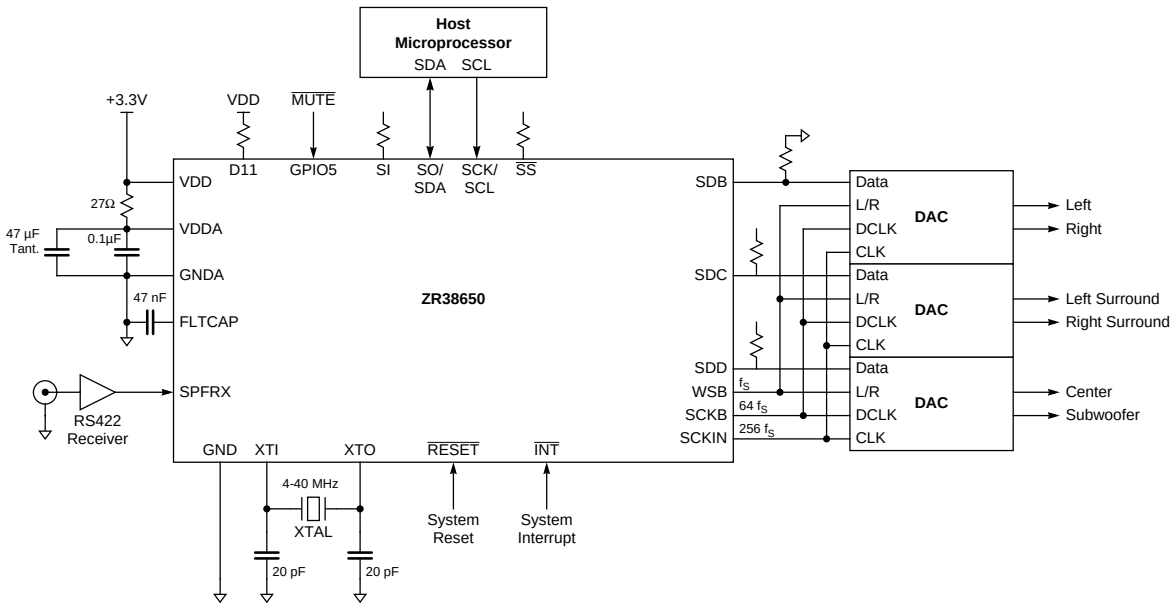


Figure 19. ZR38650 Typical Configuration With The Z2C Serial Interface To A Host Controller

Parallel Host And Parallel Data

Figure 20 shown the connections for using the parallel port as the interface to a host controller for both control with commands and for the parallel data stream input.

The ZR38650 appears in the controller's address space as three registers: an 8-bit read/write command/response register, a 9-bit data input write-only register and as a 3-bit read-only flag register. The flag register permits getting error messages from the ZR38650 (ERROR) and the $\overline{\text{DREQ}}$ and RDY bits are for programmed transfers when the ZR38650 is respectively a master or slave on the input data stream. Or the RDY signal may be used directly for a hardware I/O transfer as shown when the ZR38650 is a slave.

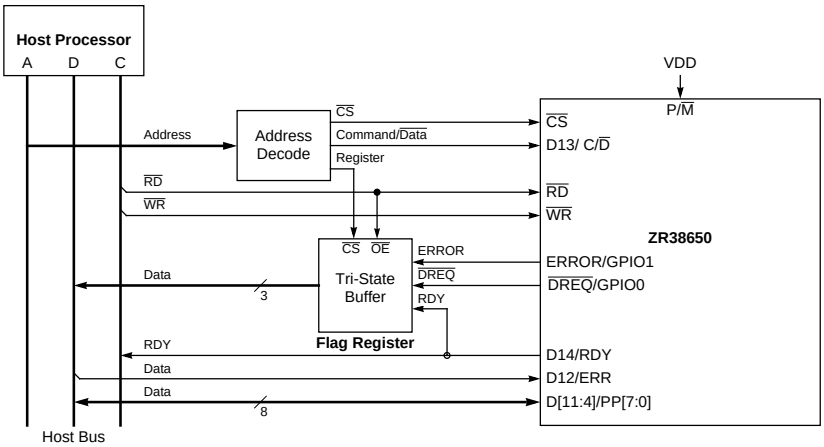


Figure 20. ZR38650 Connections With Parallel Port Interface To Host For Commands And Data Input

PRODUCT SUPPORT

Documentation

This Data Sheet is a summary description of the ZR38650's functional operation and command and response operation as well as electrical, timing and physical specifications. The complete source of information on its physical function and programmed operation including instruction set is the "ZR38650 Users Hardware Manual". Also available are the "ZR38000 Family Simulator User's Manual" and the "ZR38000 Family Assembler/Linker User's Manual."

The following Application Notes are currently available that contain additional design related information:

- "Designing with the ZR38600 Audio Processor"
- "Bass Redirection for the ZR38600 Audio Processor"
- "Audio Source Type Detection for the ZR38600 Audio Processor".

New Application Notes are added on a regular basis and are available from sales representatives.

Demonstration Board

The ZR38600 Demonstration Board is a stand-alone Dolby AC-3 and MPEG audio decoder. The demonstration board is equipped with three high-quality, stereo 20-bit DACs and one stereo 20-bit ADC for microphone or line input. The input bitstream is fed to the board in S/PDIF format. Both optical and coaxial interfaces are supported. Decoding and operation functions are selected via push buttons and a large LCD display is provided for status information. The demonstration board is equipped with a PC interface for controlling operation with the standard function commands and responses and for loading of custom programs. An ICE interface is also available on the board.

Software Development Kit

Two software development tools provide all that is necessary to write, assemble, link, simulate, and debug programs in native ZR38001 code for the ZR38650. They run on a Pentium PC under Microsoft Windows™ 95. The ZR38000 Family Assembler/Linker translates the assembly language code, including macros, to object code which can be linked with data files and other object code to generate a complete executable program file. The ZR38000 Family Simulator accurately executes the program file while permitting full displays of registers and memory along with single-step operation and breakpoints for debugging. Both are of modern design being highly interactive and with macro and symbolic naming support throughout.

The ZR38650 is software compatible with Zoran's previous generation ZR38000 family devices.

SPECIFICATIONS - ABSOLUTE MAXIMUM RATINGS

Storage Temperature..... -65 °C to +150 °C
Supply Voltage to Ground Potential Continuous ..... -0.5 V to +4.5 V
DC Voltage Applied to Outputs for High Impedance Output State..... -0.5 V to +5.5 V
DC Input Voltage ..... -0.5 V to 5.5 V
DC Output Current, into Outputs (not to exceed 200mA total)..... 20 mA/output
DC Input Current.....-10 mA to +3.0 mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

SPECIFICATIONS - OPERATING RANGE

Temperature.....$0°C \le T_A \le +70$ °C
Supply Voltage ..... $3.15\ V \le V_{CC} \le 3.45\ V$

SPECIFICATIONS - DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–	5.5	V	
V_{OL}	Output Low Voltage	–	–	0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4	–	–	V	I_{OH} = 0.4 mA
I_{CC}	Power Supply Current	–	300	350	mA	f_{CLKOUT} = 50 MHz, V_{CC} = 3.45 V
I_{LI}	Input Leakage Current	--	--	±10	µA	
I_{PUI}	Input Internal Pull-up Current Source			50	µA	
I_{PDI}	Input Internal Pull-down Current Sink			50	µA	
I_{LO}	Output Leakage Current	--	--	±10	µA	
C_{IN}	Input Capacitance	–	–	10	pF	
C_{IO}	I/O and Output Capacitance	–	–	10	pF	

During AC testing, inputs are driven at 0.4 V and 2.4 V levels. Unless otherwise specified, switching times are measured from the 1.5 V level of DCLK to the 0.8 V or 2.0 V levels at the input/output.

Figure 21. AC Testing Input, Output

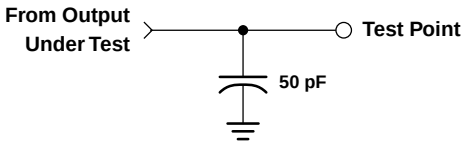


Figure 22. Normal AC Test Load

SPECIFICATIONS - AC CHARACTERISTICS

Memory Read (f_{CLKOUT} = 50 MHz)

Parameter			Min	Max	Units	Notes
Output Timing	1	Read cycle duration	25	–	ns	[1]
	2	Address hold from $\overline{RD}$ rising edge	1	–	ns	
	3	Address setup to $\overline{RD}$ falling edge	2	–	ns	
	4	$\overline{RD}$ pulse duration	11	–	ns	[1]
	5	$\overline{RD}$ after $\overline{RD}$ recovery time	6	–	ns	
	6	$\overline{WR}$ after $\overline{RD}$ recovery time	6		ns	
Input Timing	7	Data in hold from $\overline{RD}$ rising edge	0	–	ns	
	8	$\overline{RD}$ low to data valid	–	4	ns	
	9	Address stable, $\overline{CS}$ low to data valid	–	7	ns	[1]

1. These specifications are for zero wait-state operation. For operation with wait states, add 1 or 7 external clock periods, as appropriate.

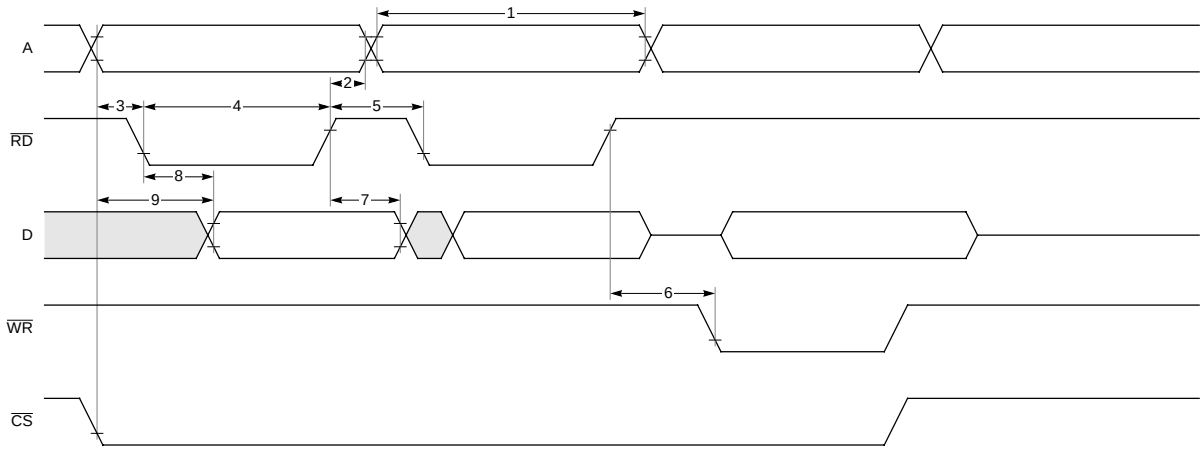


Figure 23. Memory Read

Memory Write (f_{CLKOUT} = 50 MHz)

Parameter (Output Timing)		Min	Max	Units	Notes
10	Write cycle duration	25	–	ns	[1]
11	Address setup to $\overline{WR}$ falling edge	2	–	ns	
12	$\overline{WR}$ pulse duration	11	–	ns	[1]
13	Address hold from $\overline{WR}$ rising edge	1	–	ns	
14	Data out setup to $\overline{WR}$ rising edge	6	–	ns	[1]
15	Data out hold from $\overline{WR}$ rising edge	1	–	ns	
16	$\overline{WR}$ low to data out enabled	3	–	ns	
17	$\overline{WR}$ after $\overline{WR}$ recovery time	6	–	ns	
18	$\overline{RD}$ after $\overline{WR}$ recovery time	6	–	ns	
19	Data disable to $\overline{RD}$ after $\overline{WR}$	4	–	ns	
20	$\overline{WR}$ falling edge to data valid		5	ns	
21	Address valid to $\overline{WR}$ rising edge	13		ns	

1. These specifications are for zero wait-state operation. For operation with wait states, add 1 or 7 internal clock periods, as appropriate.

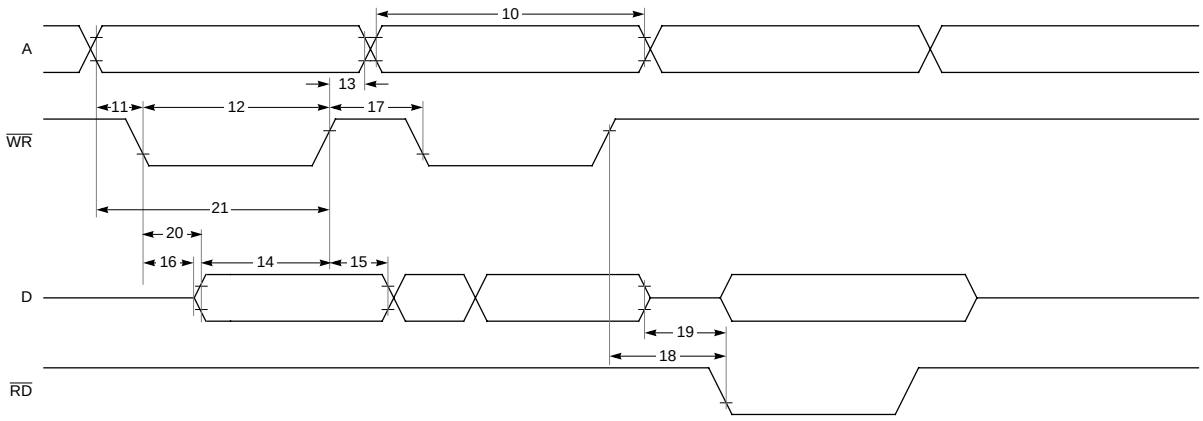


Figure 24. Memory Write

A-Group Serial Ports (Frame Sync Mode)

Parameter			Min	Max	Units	Notes
Input Timing	22	SCKA high duration	t_{CLKOUT}	–	ns	Slave Mode (MA = 0)
	23	SCKA low duration	t_{CLKOUT}	–	ns	Slave Mode (MA = 0)
	24	FSA setup time to SCKA falling edge	15	–	ns	Slave Mode (MA = 0)
	25	FSA hold time from SCKA falling edge	15	–	ns	Slave Mode (MA = 0)
	26	SDA, SDE, SDF setup time to SCKA falling edge	15	–	ns	
	27	SDA, SDE, SDF hold time from SCKA falling edge	15	–	ns	
Output Timing	29	FSA output delay from SCKA rising edge	–	25	ns	Master Mode (MA = 1)
	30	SCKA period	8 t_{CLKOUT}	4096 t_{CLKOUT}	ns	Master Mode (MA = 1)

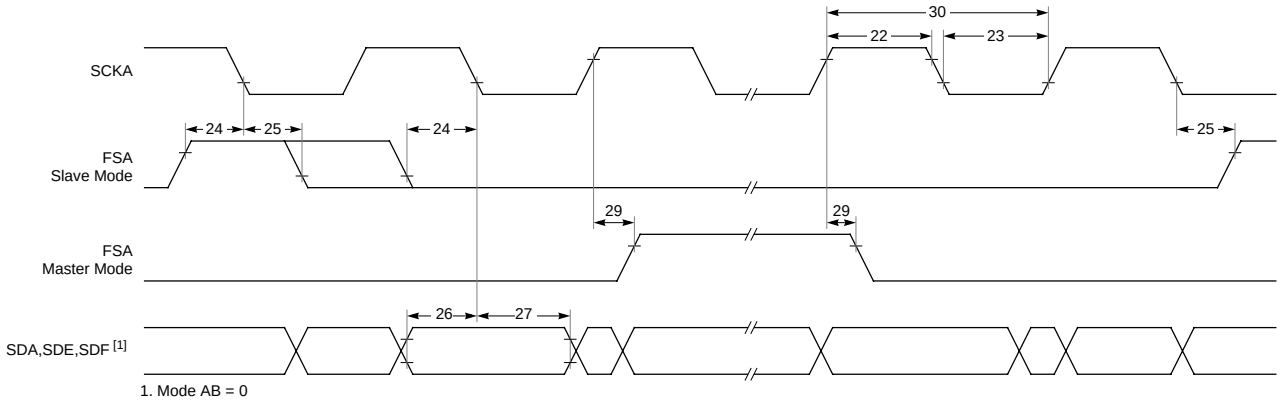


Figure 25. A-Group Serial Ports (Frame Sync Mode)

A-Group Serial Ports (Word Select Mode)

Parameter			Min	Max	Units	Notes
Input Timing	22	SCKA high duration	t_{CLKOUT}	–	ns	Slave Mode (MA = 0)
	23	SCKA low duration	t_{CLKOUT}	–	ns	Slave Mode (MA = 0)
	31	WSA setup time to SCKA rising edge	15	–	ns	Slave Mode (MA = 0)
	32	WSA hold time from SCKA rising edge	15	–	ns	Slave Mode (MA = 0)
	33	SDA, SDE, SDF setup time to SCKA rising edge	15	–	ns	
	36	SDA, SDE, SDF hold time from SCKA rising edge	15	–	ns	
Output Timing	30	SCKA period	8 t_{CLKOUT}	4096 t_{CLKOUT}	ns	Master Mode (MA = 1)
	73	WSA output delay from SCKA falling edge	–	25	ns	Master Mode (MA = 1)

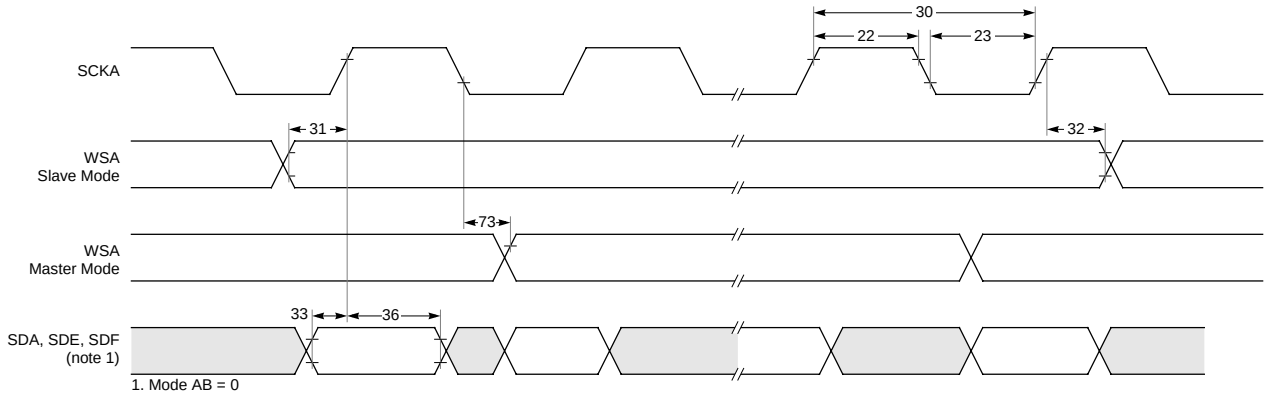


Figure 26. A-Group Serial Ports (Word Select Mode)

B-Group Serial Ports (Frame Sync Mode)

Parameter			Min	Max	Units	Notes
Input Timing	41	SCKIN low duration	t_{CLKOUT}	–	ns	CB = 0
	42	SCKIN high duration	t_{CLKOUT}	–	ns	CB = 0
	75	SCKB high duration	t_{CLKOUT}	–	ns	Slave Mode (MB = 0)
	76	SCKB low duration	t_{CLKOUT}	–	ns	Slave Mode (MB = 0)
	48	SDF setup time to SCKB falling edge	15	–	ns	Mode AB = 1, CPB = 1
	49	SDF hold time from SCKB falling edge	15	–	ns	Mode AB = 1, CPB = 1
	78	FSB setup time to SCKB falling edge	15	–	ns	Slave Mode (MB = 0), CPB = 1
	79	FSB hold time from SCKB falling edge	15	–	ns	Slave Mode (MB = 0), CPB = 1
Output Timing	40	SCKIN period (t_{SCKIN})	t_{CLKOUT}		ns	CB = 1
	43	SCKB period	t_{SCKIN}	8192 t_{SCKIN}	ns	Master Mode (MB = 1), CB = 0
			t_{AUDIO}	8192 t_{AUDIO}	ns	Master Mode (MB = 1), CB = 1
	44	FSB delay from SCKB rising edge	–	25	ns	Master Mode (MB = 1)
	45	SDB, SDC delay from SCKB rising edge	–	25	ns	

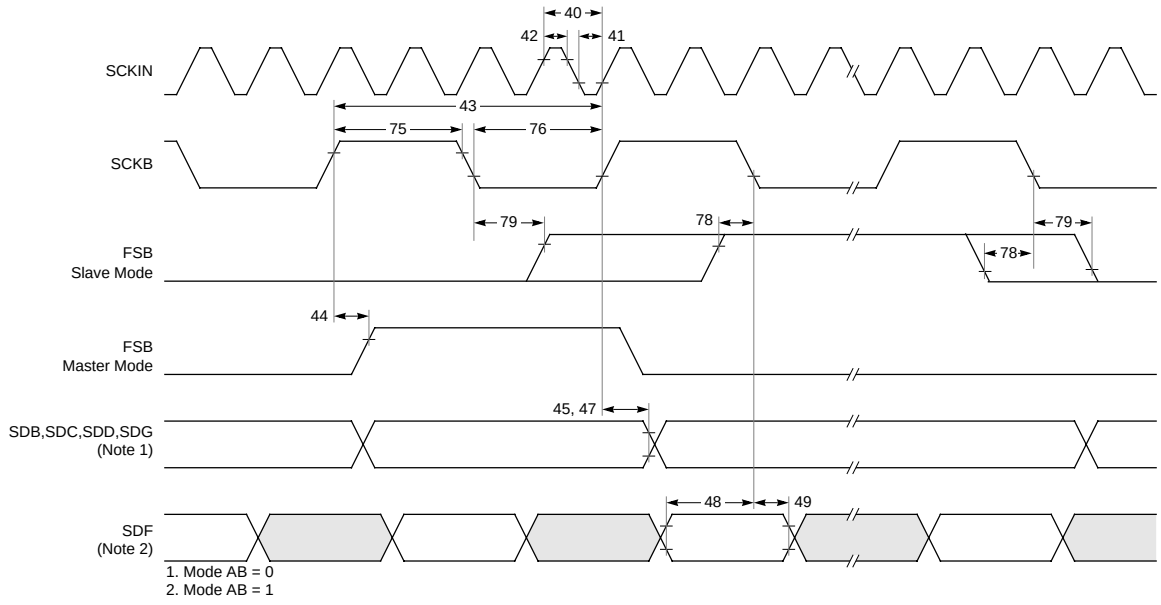


Figure 27. B-Group Serial Ports (Frame Sync Mode)

B-Group Serial Ports (Word Select Mode)

Parameter			Min	Max	Units	Notes
Input Timing	50	SDF setup time to SCKB rising edge	15	–	ns	Mode AB = 1
	51	SDF hold time from SCKB rising edge	15	–	ns	Mode AB= 1
	52	WSB setup to SCKB rising edge	15	–	ns	Slave Mode (MB = 0)
	53	WSB hold from SCKB rising edge	15	–	ns	Slave Mode (MB = 0)
Output Timing	80	WSB delay from SCKB falling edge	–	25	ns	Master Mode (MB = 1)
	81	SDB, SDC, SDD delay from SCKB falling edge	–	25	ns	

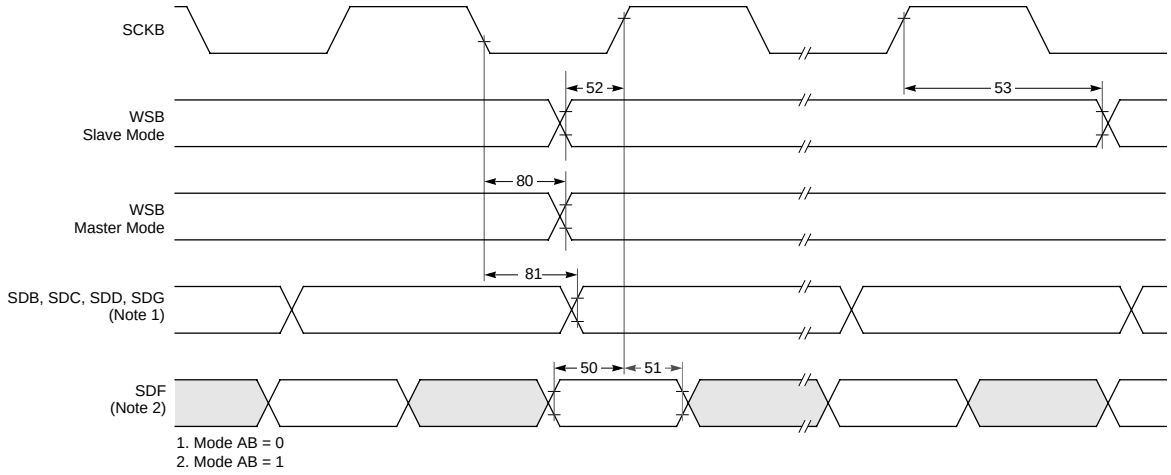


Figure 28. B-Group Serial Ports (Word Select Mode)

Parallel Host Interface Timing

Characteristics		Min	Max	Units	Notes
99	$\overline{RD}$, $\overline{WR}$ high time	2 t_{CLKOUT}		ns	
100	$\overline{RD}$, $\overline{WR}$ low time	2 t_{CLKOUT}		ns	
101	$\overline{RD}$, $\overline{WR}$ cycle time	3 t_{CLKOUT}		ns	
102	Data hold time from $\overline{WR}$ high	3	–	ns	
103	Data setup time to $\overline{WR}$ high	11	–	ns	Write cycle
104	Data out delay from $\overline{RD}$ low	–	30	ns	Read cycle
105	$\overline{CS}$ setup to falling edge of $\overline{RD}$, $\overline{WR}$	0		ns	
106	$\overline{CS}$ hold from rising edge of $\overline{RD}$, $\overline{WR}$	1		ns	
107	$\overline{CS}$ low to $\overline{CS}$ low	30		ns	
108	$\overline{WR}$ to $\overline{RD}$, $\overline{RD}$ to $\overline{WR}$ timing	60			
109	Data hold time from rising edge of $\overline{RD}$	16		ns	
110	RDY delay time		2 t_{CLKOUT}	ns	

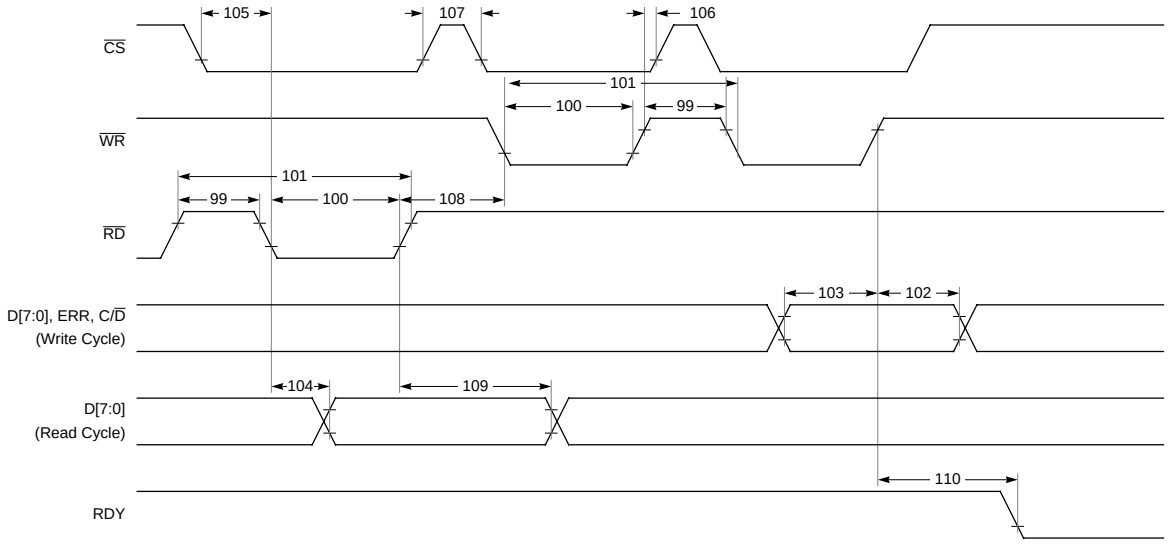


Figure 29. Parallel Host Interface Timing

Z2C Serial Host Interface Timing

Parameter		Min	Max	Units	Notes
201	SCL/SCK clock period	2.5	–	µs	
202	SCL/SCK clock high duration	0.6	–	µs	
203	SCL/SCK clock low duration	1.3	–	µs	
204	START condition setup time	0.6	–	µs	
205	START condition hold time	0.6	–	µs	
206	Data setup time to SCL/SCK active edge	100	–	ns	
207	Data hold time from SCL/SCK active edge	0.0	–	ns	
208	Rise time of SCL/SCK and SDA/SO	–	300	ns	
209	Fall time of SCL/SCK and SDA/SO	–	300	ns	
210	STOP condition setup time	0.5	–	µs	
211	Free time between STOP and START condition	1.3	–	µs	

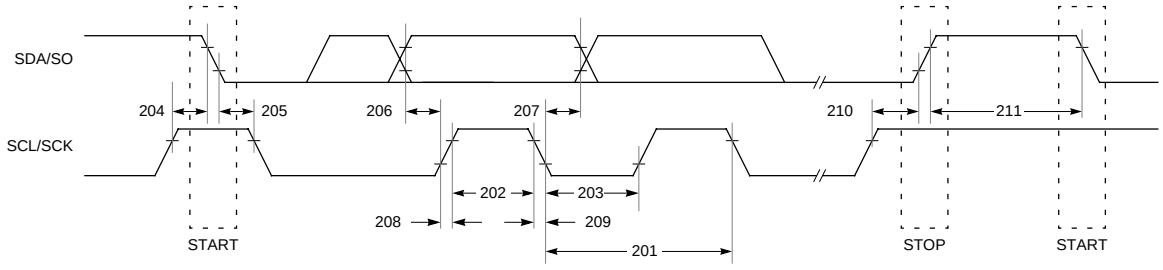


Figure 30. Z2C Serial Host Interface Timing

SPI Serial Host Interface Timing

Parameter		Min	Max	Units	Notes
111	SCK/SCL clock period	6 t_{CLKOUT}	–	ns	[1]
112	SCK/SCL clock high duration	3 t_{CLKOUT}	–	ns	
113	SCK/SCL clock low duration	3 t_{CLKOUT}	–	ns	
114	$\overline{SS}$ setup time to first SCK/SCL edge	10	–	ns	
115	$\overline{SS}$ hold time from last edge of SCK/SCL	10	–	ns	
116	SI setup time to SCK/SCL active edge	10	–	ns	
117	SI hold time from SCK/SCL active edge	10	–	ns	
118	$\overline{SS}$ negation to data Hi-Z	–	10	ns	
119	SO/SDA delay from SCK/SCL active edge	–	20	ns	

1. SCK polarity is controlled by field SCKP of register SPIMODE. The polarity shown in Figure 31 corresponds to SCKP=0.

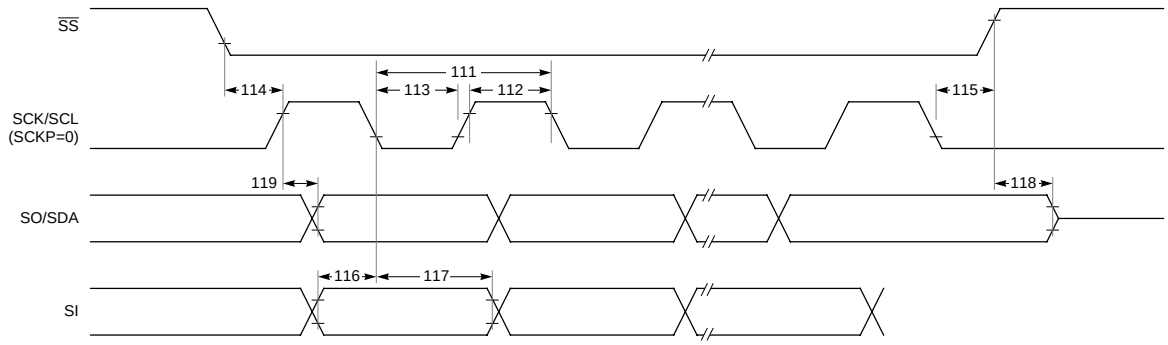


Figure 31. SPI Serial Host Interface Timing

External Clocks

	Parameter	Min	Max	Units	Notes
56	XTI period (t_{XTI})	25	250	ns	
57	XTI high duration	10		ns	
58	XTI low duration	10		ns	
55	CLKOUT period (t_{CLKOUT})	20	250	ns	

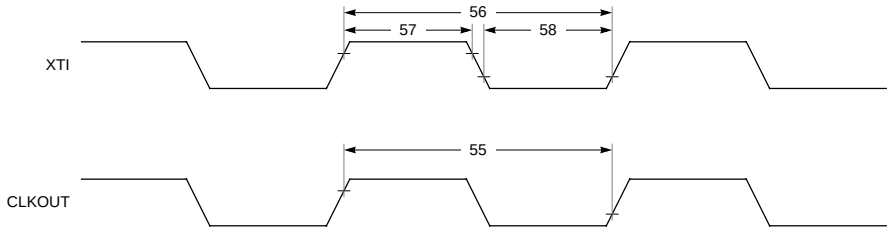


Figure 32. External Clocks

External Interrupt

	Parameter	Min	Max	Units	Notes
63	$\overline{INT}$ setup time	6		ns	[1]
64	$\overline{INT}$ hold time	5		ns	[1]
65	$\overline{INT}$ duration	2 t_{CLKOUT}		ns	

1. For testing only. Synchronous operation is not required.

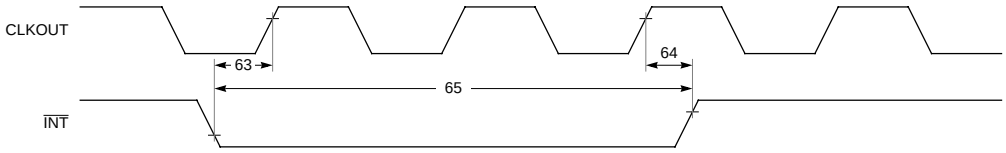


Figure 33. External Interrupt

Reset Timing

	Parameter	Min	Max	Units	Notes
59	$\overline{\text{RESET}}$ duration, warm reset	16 t_{XTI}	127 t_{XTI}	ns	
60	$\overline{\text{RESET}}$ duration, cold reset	200 t_{XTI}		ns	[1]
61	Memory bus enable after $\overline{\text{RESET}}$ rising edge, warm reset	t_{XTI} +10	2 t_{XTI} +15	ns	
62	Memory bus disable after $\overline{\text{RESET}}$ falling edge	t_{XTI} +10	2 t_{XTI} +15	ns	

1. Applies to the power-up sequence. The rising edge of $\overline{\text{RESET}}$ must occur after the crystal oscillator or external clock frequency and amplitude have stabilized. After the rising edge of a cold $\overline{\text{RESET}}$, 4096 clock cycles are required for initialization of the internal phase locked loop, during which the processor is inactive. Any subsequent reset pulse of 128 clocks or longer is interpreted as a cold reset and will start a new initialization of the phase locked loop.

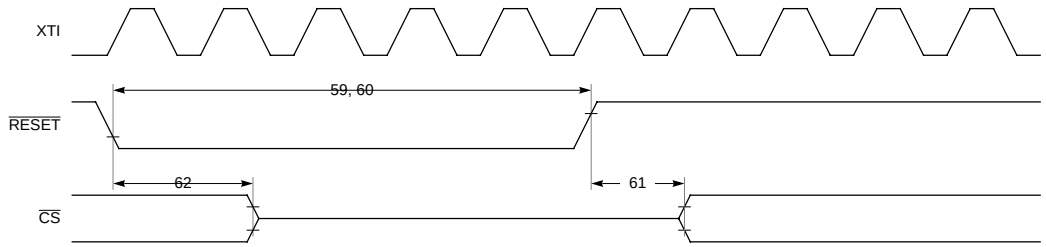


Figure 34. Warm/Cold Reset

ICE Interface Timing

	Parameter	Min	Max	Units	Notes
121	TCK clock period	4 t_{CLKOUT}	–	ns	
122	TCK clock high duration	2 t_{CLKOUT}	–	ns	
123	TCK clock low duration	2 t_{CLKOUT}	–	ns	
124	TDO negation to data Hi-Z	–	15	ns	
125	TDO delay from falling edge of TCK	–	15	ns	
126	TDI hold time from rising edge of TCK	10	–	ns	
127	TDI setup time to rising edge of TCK	10	–	ns	
128	TMS hold time from rising edge of TCK	10	–	ns	
129	TMS setup time to rising edge of TCK	10	–	ns	

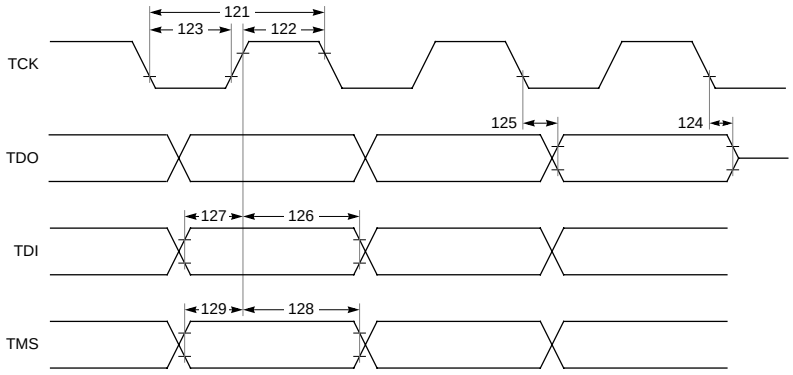


Figure 35. ICE Interface Timing

PINOUT INFORMATION

Table 24: 144-Pin TQFP Package Pin Assignment By Pin Number

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	GND	37	GND	73	GND	109	GND
2	nc	38	nc	74	nc	110	nc
3	GND	39	GND	75	GND	111	nc
4	$\overline{SS}$	40	D23	76	SDD	112	SDC
5	TMS	41	D22	77	VDD	113	D31
6	$\overline{INT}$	42	VDD	78	GPIO2	114	D30
7	D26	43	A11	79	D1	115	SDB
8	D25	44	D9/PP5	80	GPIO1	116	D29
9	VDD	45	D8/PP4	81	D0	117	D28
10	D14/RDY	46	SO/SDA	82	GPIO0	118	VDD
11	GND	47	D21	83	VDD	119	$\overline{RESET}$
12	A1	48	VDD	84	GND	120	SDA
13	A2	49	GND	85	BYPASS	121	VDD
14	A3	50	D20	86	SPFRX	122	SDE
15	VDD	51	GND	87	P/$\overline{M}$	123	TCK
16	D13/ C/$\overline{D}$	52	A12	88	XTO	124	SCK
17	GPIO5	53	TDO	89	XTI	125	TDI
18	D12/ERR	54	A13	90	MMAP	126	SI
19	D24	55	D7/PP3	91	GND	127	GND
20	A4	56	D6/PP2	92	GND	128	SCKA
21	VDD	57	A14	93	SCKIN	129	WSA/FSA
22	GPIO4	58	GND	94	VDD	130	VDD
23	GND	59	VDD	95	VDD	131	SDF
24	A5	60	A15	96	GND	132	GND
25	A6	61	D5/PP1	97	GNDA	133	D27
26	D11/PP7	62	D4/PP0	98	FLTCAP	134	WSB/FSB
27	GPIO3	63	VDD	99	VDDA	135	D17
28	VDD	64	A16	100	GND	136	SCKB
29	A7	65	$\overline{RD}$	101	CLKOUT	137	D16
30	A8	66	$\overline{WR}$	102	D19	138	SDG/SPFTX
31	D10/PP6	67	$\overline{CS}$	103	D18	139	D15
32	A9	68	D3	104	A17	140	VDD
33	A10	69	D2	105	A18	141	A0
34	nc	70	GND	106	A19	142	GND
35	nc	71	nc	107	nc	143	nc
36	GND	72	GND	108	GND	144	GND

Table 25: 144-Pin TQFP Package Pin Assignment By Alphabetical Signal Name

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
A0	141	D13/ C/$\overline{D}$	16	GND	84	SDB	115
A1	12	D14/RDY	10	GND	91	SDC	112
A2	13	D15	139	GND	92	$\overline{SDD}$	76
A3	14	D16	137	GND	96	SDE	122
A4	20	D17	135	GND	100	SDF	131
A5	24	D18	103	GND	108	SDG/SPFTX	138
A6	25	D19	102	GND	109	SI	126
A7	29	D20	50	GND	127	SO/SDA	46
A8	30	D21	47	GND	132	SPFRX	86
A9	32	D22	41	GND	142	$\overline{SS}$	4
A10	33	D23	40	GND	144	TCK	123
A11	43	D24	19	GNDA	97	TDI	125
A12	52	D25	8	GPIO2	78	TDO	53
A13	54	D26	7	GPIO3	27	TMS	5
A14	57	D27	133	GPIO4	22	VDD	9
A15	60	D28	117	$\overline{INT}$	6	VDD	15
A16	64	D29	116	MMAP	90	VDD	21
A17	104	D30	114	$\overline{MUTE}$/GPIO5	17	VDD	28
A18	105	D31	113	nc	2	VDD	42
A19	106	$\overline{DREQ}$/GPIO0	82	nc	34	VDD	48
BYPASS	85	ERROR/GPIO1	80	nc	35	VDD	59
CLKOUT	101	FLTCAP	98	nc	38	VDD	63
$\overline{CS}$	67	GND	1	nc	71	VDD	77
D0	81	GND	3	nc	74	VDD	83
D1	79	GND	11	nc	107	VDD	94
D2	69	GND	23	nc	110	VDD	95
D3	68	GND	36	nc	111	VDD	118
D4/PP0	62	GND	37	nc	143	VDD	121
D5/PP1	61	GND	39	P/$\overline{M}$	87	VDD	130
D6/PP2	56	GND	49	$\overline{RD}$	65	VDD	140
D7/PP3	55	GND	51	$\overline{RESET}$	119	VDDA	99
D8/PP4	45	GND	58	SCK/SCL	124	$\overline{WR}$	66
D9/PP5	44	GND	70	SCKA	128	WSA/FSA	129
D10/PP6	31	GND	72	SCKB	136	WSB/FSB	134
D11/PP7	26	GND	73	SCKIN	93	XTI	89
D12/ERR	18	GND	75	SDA	120	XTO	88

Table 26: 144-Pin TQFP Package Pin Assignment By Functional Signal Name

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
Parallel Port (56)							
A19	106	A5	24	D23	40	D9/PP5	44
A18	105	A4	20	D22	41	D8/PP4	45
A17	104	A3	14	D21	47	D7/PP3	55
A16	64	A2	13	D20	50	D6/PP2	56
A15	60	A1	12	D19	102	D5/PP1	61
A14	57	A0	141	D18	103	D4/PP0	62
A13	54	D31	113	D17	135	D3	68
A12	52	D30	114	D16	137	D2	69
A11	43	D29	116	D15	139	D1	79
A10	33	D28	117	D14/RDY	10	D0	81
A9	32	D27	133	D13/ C/$\overline{D}$	16	$\overline{CS}$	67
A8	30	D26	7	D12/ERR	18	$\overline{RD}$	65
A7	29	D25	8	D11/PP7	26	$\overline{WR}$	66
A6	25	D24	19	D10/PP6	31	P/$\overline{M}$	87
Serial Ports (13)							
SPFRX	86	WSA/FSA	129	SDD	76	SCKIN	93
SDA	120	SCKA	128	SDG/SPFTX	138		
SDE	122	SDB	115	WSB/FSB	134		
SDF	131	SDC	112	SCKB	136		
General Purpose Ports (6)							
$\overline{MUTE}$/GPIO5	17	GPIO3	27	ERROR/GPIO1	80		
GPIO4	22	GPIO2	78	$\overline{DREQ}$/GPIO0	82		
Serial Host Interface (4)							
SI	126	SO/SDA	46	SCK/SCL	124	$\overline{SS}$	4
ICE Interface (4)							
TDI	125	TDO	53	TCK	123	TMS	5
System Interface (8)							
$\overline{INT}$	6	MMAP	90	XTO	88	BYPASS	85
$\overline{RESET}$	119	XTI	89	CLKOUT	101	FLTCAP	98
Power (43)							
VDD	9	VDD	95	GND	37	GND	92
VDD	15	VDD	118	GND	39	GND	96
VDD	21	VDD	121	GND	49	GND	100
VDD	28	VDD	130	GND	51	GND	108
VDD	42	VDD	140	GND	58	GND	109
VDD	48	VDDA	99	GND	70	GND	127
VDD	59	GND	1	GND	72	GND	132
VDD	63	GND	3	GND	73	GND	142
VDD	77	GND	11	GND	75	GND	144
VDD	83	GND	23	GND	84	GNDA	97
VDD	94	GND	36	GND	91		
No Connection (10)							
nc	2	nc	38	nc	107	nc	143
nc	34	nc	71	nc	110		
nc	35	nc	74	nc	111		

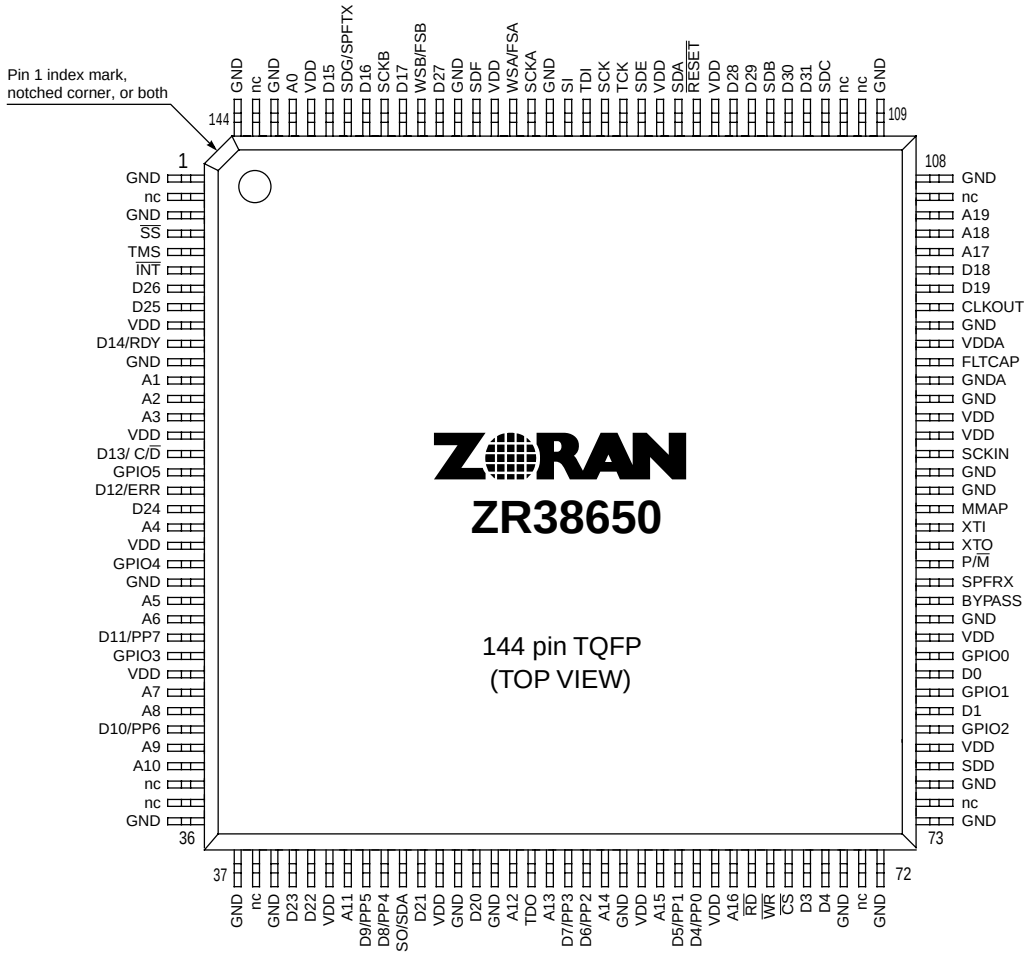


Figure 36. ZR38650 Pin Out Diagram

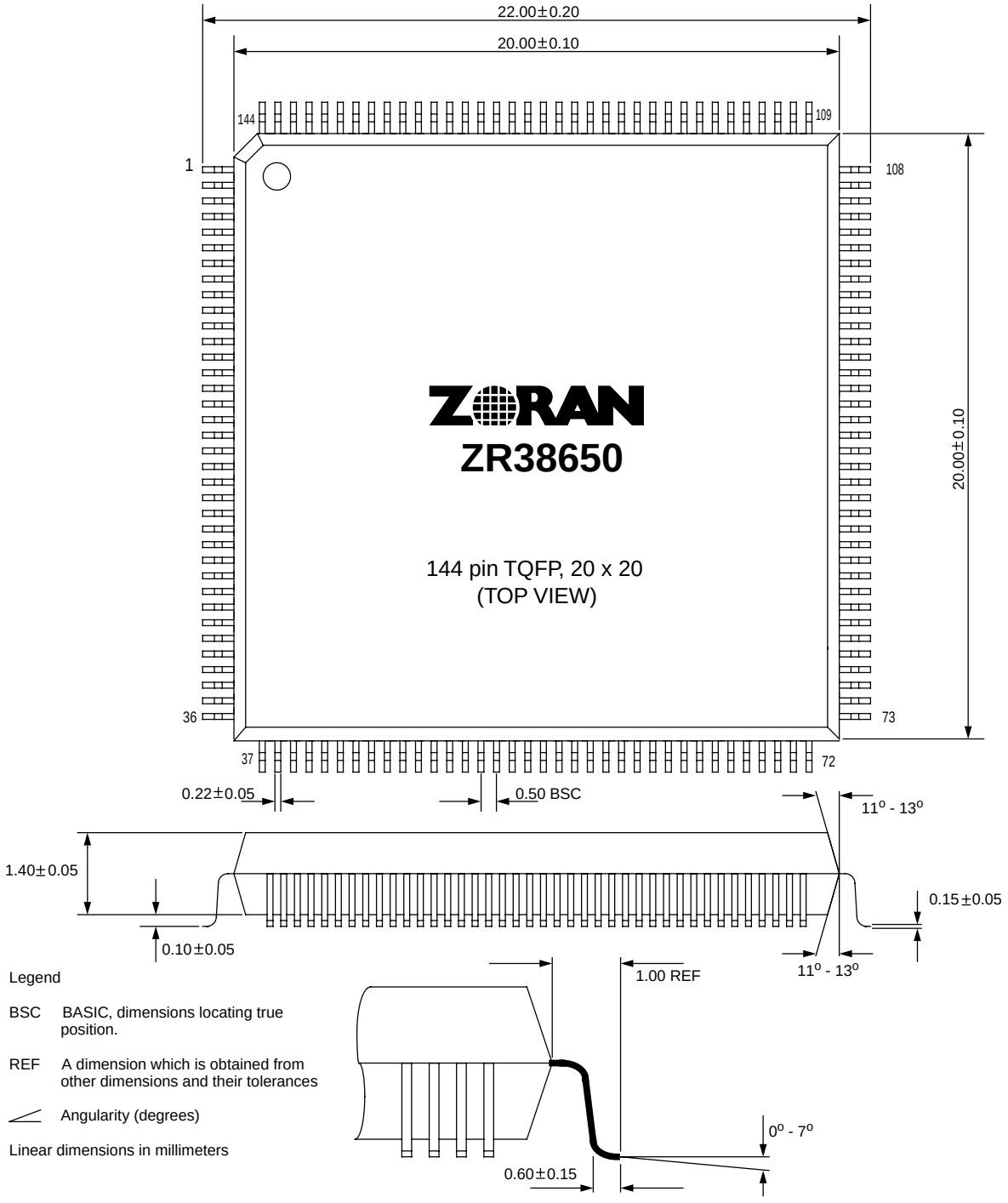
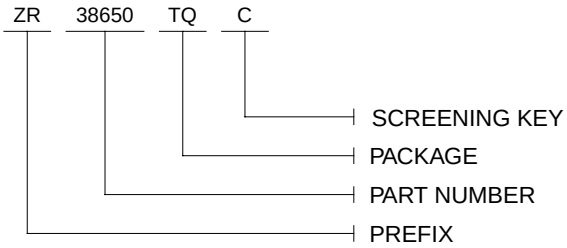


Figure 37. ZR38650 144-Pin TQFP Package Dimensions

ORDERING INFORMATION



PACKAGE

TQ - Plastic Thin Quad Flat Pack (EIAJ)

SCREENING KEY

C - 0°C to +70°C (V_{CC} = 3.15V to 3.45V)

Note: Dolby Licensing:
AC-3 and Pro Logic usage is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA 94111, USA, +1 (415) 558-0200, from whom licensing and application information must be obtained.
Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

SALES OFFICES

■ ***U.S. Headquarters***
Zoran Corporation
3112 Scott Blvd.
Santa Clara, CA 95054 USA
Telephone: +1 (408) 919-4111
FAX: +1 (408) 919-4122

■ ***Israel Operations***
Zoran Microelectronics, Ltd.
Advanced Technology Center
P.O. Box 2495
Haifa, 31024 Israel
Telephone: +972 4 8545-777
FAX: +972 4 8551-550

■ ***Canada***
Zoran Toronto Labs
2157 Queen Street East
Suite 302
Toronto, Ontario, Canada M4E 1ES
Telephone: +1 (416) 690-3356
FAX: +1 (416) 690-3363

■ ***Japan***
Zoran Sales Office
2-26-2 Sasazuka
Shibuya-ku, Tokyo 151
Japan
Telephone: +81 3 5352-0971
FAX: +81 3 5352-0972

■ ***P. R. China***
Zoran China Office (Shenzhen)
Suite 1706, Grand Skylight Hotel
8 Central Shennan Road
Shenzhen, Guangdong 518041
P. R. China
Telephone: +86 755-3363225
Mobile Phone: +86 139-2704950
FAX: +86 755-3363256