ZEN2044F

PROGRAMMABLE UNIVERSAL COUNTER

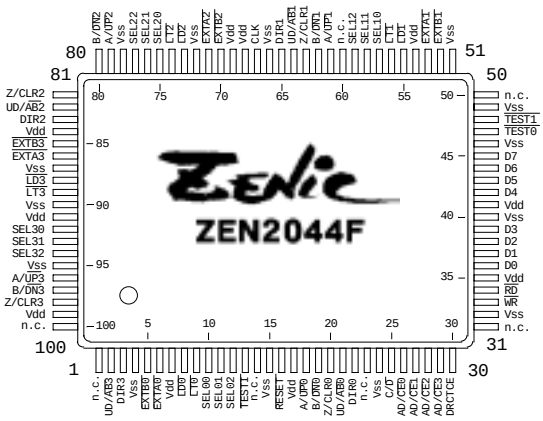
DESCRIPTION

The ZEN2044F is a 24bit x 4ch. programmable universal counter LSI. The ZEN2044F can count phase-shifted pulse signals or up/down pulse signals generated from rotary encoders or linear scales.

Since the counter response speed is as high as 33MHz(MAX), the ZEN2044F can be used in a variety of applications required high speed counting, including digital servo controls and precision measurements. As to command sets, the ZEN2044F has a compatibility with the ZEN2011P.

The ZEN2044F can also monitor input signals and detect any abnormal input accompanied with noise or other disturbances, so that the reliability of counted values are secured.

Pin Configuration(Top View)

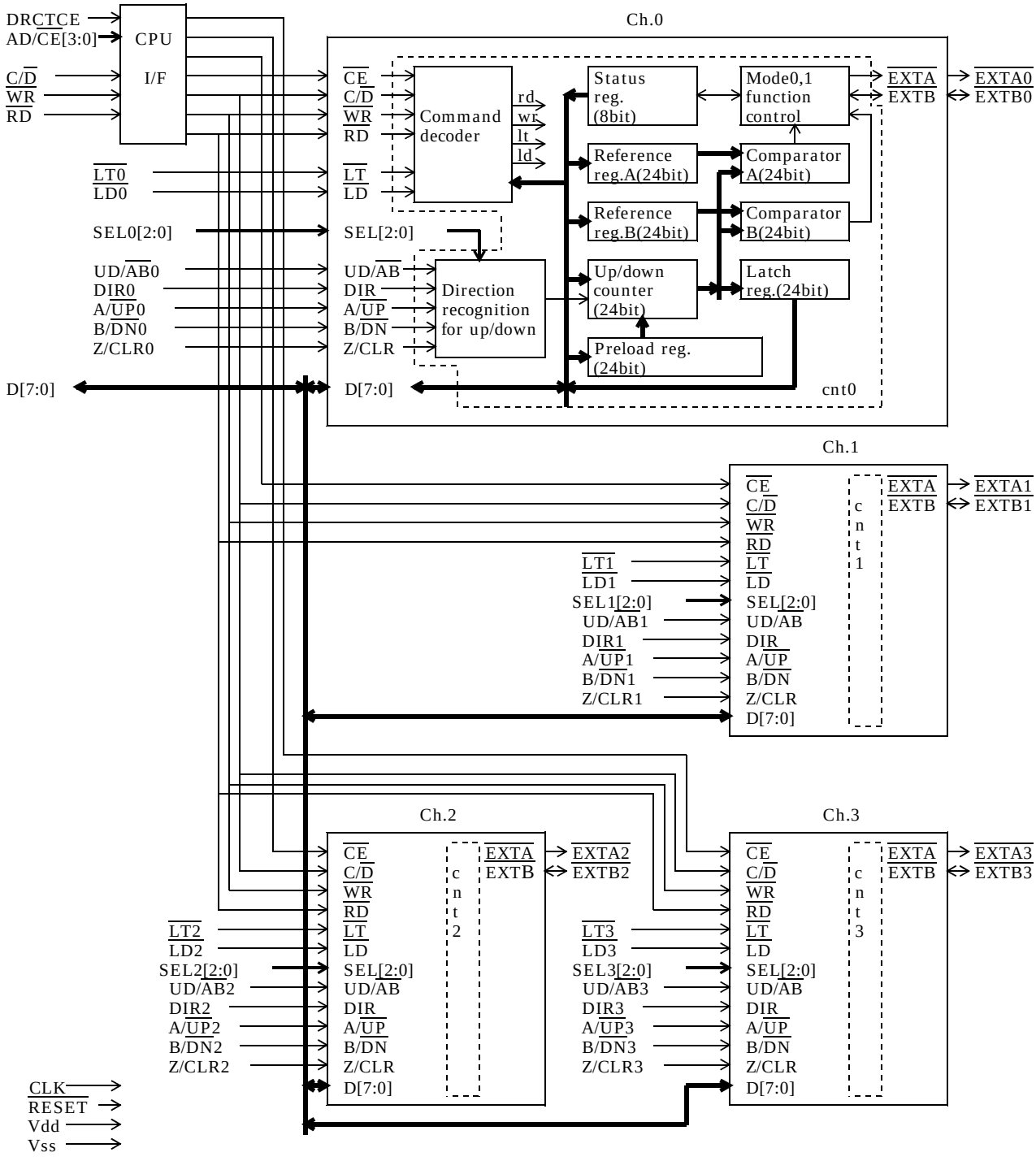


1. Features

24bit binary up/down counter x 4ch.
Counter response speed:
  33MHz(MAX)(CLK fo=33MHz at 50% duty)
Input frequency of count pulse
  Two phase-shifted pulse signal input:
    DC-8.25MHz (less than fo x 1/4)
  Up/down pulse signal input:
    DC-16.5MHz (less than fo x 1/2)
Direction recognition for up/down count
Abnormal input detection circuit
Preload register for the up/down counter
Latch register for the up/down counter
Coincidence detection between reference value and count value
Counter operation mode
  Quad/double/single edge evaluation(for two phase-shifted signal / single pulse signal)
  Counter direction selection
  Count clear control: synchronous/asynchronous
Command mode
  Mode 0:
    Each channel has one comparator for coincidence detection
    Each channel has one port for user input
  Mode 1:
    Each channel has two comparators for coincidence detection
    Each channel has no port for user input
    Logical sum output of coincidence detections available
    Interrupt output under some conditions available
8bit data bus
Low power CMOS technology
TTL level compatible input
Single 5V power supply
100 pin QFP

Note) In following chapters;
"*n*" corresponds to a number of the channel(0-3).
"*" stands for "Don't care".

2. Block diagram



3. Pin description

Table 1

Name	No.	I/O	Function
$\overline{EXTA0}$ $\overline{EXTA1}$ $\overline{EXTA2}$ $\overline{EXTA3}$	6 53 71 86	O	The function of this output depends on the command mode. In Mode 0, $\overline{EXTAn}$ outputs the equal signal A($\overline{EQAn}$). In Mode 1, one of the following three signals can be selected: -The equal signal A($\overline{EQAn}$). -The logical sum($\overline{EQAn}$ +$\overline{EQBn}$) of the equal signal A($\overline{EQAn}$) and the equal signal B($\overline{EQBn}$). -The hold equal signal A($\overline{INTEQAn}$).
CLK	67	I	The CLK synchronizes the internal circuit operation.
$\overline{RESET}$	16	I	The $\overline{RESET}$ initializes the up/down counter, the phase discrimination circuit, the command register and the status register.
AD/$\overline{CE0}$ AD/$\overline{CE1}$ AD/$\overline{CE2}$ AD/$\overline{CE3}$	26 27 28 29	I	The function of these pins depends on the DRCTCE. If DRCTCE="1", they are all treated as signals for enabling the channel directly. If DRCTCE="0",AD/$\overline{CE3}$ and AD/$\overline{CE2}$ are the chip enable pins and AD/$\overline{CE1}$ and AD/$\overline{CE0}$ are used to select the channnel.
DRCTCE	30	I	The DRCTCE specifies the mode of the channel select.
C/$\overline{D}$	25	I	The C/$\overline{D}$ defines the type of the data transfered between the CPU and the ZEN2044F(command or value). This pin is usually connected with LSB of the address lines.
$\overline{RD}$	34	I	The $\overline{RD}$ is the strobe signal of the read operation.
$\overline{WR}$	33	I	The $\overline{WR}$ is the strobe signal of the write operation.
$\overline{LD0}$ $\overline{LD1}$ $\overline{LD2}$ $\overline{LD3}$	8 55 73 88	I	The $\overline{LDn}$ transmits the 32bit data which is stored in the preload register to the up/down counter.
$\overline{LT0}$ $\overline{LT1}$ $\overline{LT2}$ $\overline{LT3}$	9 56 74 89	I	The $\overline{LTn}$ stores the 32bit data of the up/down counter into the latch register.
D0 D1 D2 D3 D4 D5 D6 D7	36 37 38 39 42 43 44 45	I/O	These pins are connected with CPU data bus.
$\overline{EXTB0}$ $\overline{EXTB1}$ $\overline{EXTB2}$ $\overline{EXTB3}$	5 52 70 85	I/O	In Mode 0, $\overline{EXTBn}$ is used as a general purpose input U of which value can be read from the status register. In Mode 1, $\overline{EXTBn}$ is a programable output. One of the following three signals can be selected: -The equal signal B($\overline{EQBn}$) -The signal that indicates detecting an abnormal input($\overline{INTAIn}$) -The hold equal signal B(INTEQB*n*)

Name	No.	I/O	Function
Z/CLR0 Z/CLR1 Z/CLR2 Z/CLR3	20 63 81 98	I	The Z/CLR*n* clears the value of the up/down counter. This pin is usually connected with the index signal of a rotary encoder or a linear scale.
B/$\overline{\text{DN}}$0 B/$\overline{\text{DN}}$1 B/$\overline{\text{DN}}$2 B/$\overline{\text{DN}}$3	19 62 80 97	I	The B/$\overline{\text{DN}}$*n* is the count pulse input B or DN.
A/$\overline{\text{UP}}$0 A/$\overline{\text{UP}}$1 A/$\overline{\text{UP}}$2 A/$\overline{\text{UP}}$3	18 61 79 96	I	The A/$\overline{\text{UP}}$*n* is the count pulse input A or UP.
SEL00 SEL01 SEL02 SEL10 SEL11 SEL12 SEL20 SEL21 SEL22 SEL30 SEL31 SEL32	10 11 12 57 58 59 75 76 77 92 93 94	I	The condition of these three pins(SEL*n*0, SEL*n*1 and SEL*n*2) specifies the counter operation mode. See the Table 4.
DIR0 DIR1 DIR2 DIR3	22 65 83 3	I	The DIR*n* selects the count direction of the up/down counter.
UD/$\overline{\text{AB}}$0 UD/$\overline{\text{AB}}$1 UD/$\overline{\text{AB}}$2 UD/$\overline{\text{AB}}$3	21 64 82 2	I	The UD/$\overline{\text{AB}}$*n* selects the input pulse mode(up/down or not).
Vss	4 15 24 32 40 46 49 51 66 72 78 87 90 95	-	Ground(0V)

Name	No.	I/O	Function
Vdd	7 17 35 41 54 68 69 84 91 99	-	Supply voltage(+5V)
N.C.	1 14 23 31 50 60 100	-	Not connected.
$\overline{\text{TEST0}}$ $\overline{\text{TEST1}}$ $\overline{\text{TESTI}}$	47 48 13	I	These test pins MUST be connected with +5V in nomal operation.

Note) Except N.C., the input pins which are not used MUST be connected with Vdd or Ground.

4. Operation

The opration of the ZEN2044F is controled by the system software. To use this counter, it is necessary to specify "command words","counter reference value(if necessary)" and "preloaded value(if necessary)". Since the entire control circuit woks synchronously, the operations about registers(i.e. data read/write, command write and status read) can be carried out even if the counter is working.

Each channel can be programed separately because the ZEN2044F has four fully independent sets of the counter and the registers.

4-1. CPU Interface

The CPU can access the ZEN2044F with AD/$\overline{CE}$3-0, C/$\overline{D}$, $\overline{RD}$ and $\overline{WR}$. The ZEN2044F has following two modes for selecting the target channel. The mode depends on DRCTCE.

4-1-1. Direct Channel Enable Mode(DRCTCE="1")

In this mode, AD/$\overline{CE}$*n* is used as the channel enable input for channel *n* . So multiple channels can be accessd at a time(write operation only).

Table 2

DRCTCE	AD/$\overline{CE}$3	AD/$\overline{CE}$2	AD/$\overline{CE}$1	AD/$\overline{CE}$0	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Function
1	1	1	1	1	*	*	*	Disable(data bus: High-impedance)
1	1	1	1	0	0	0	1	Read: latch register(ch.0)
1	1	1	0	1	0	0	1	Read: latch register(ch.1)
1	1	0	1	1	0	0	1	Read: latch register(ch.2)
1	0	1	1	1	0	0	1	Read: latch register(ch.3)
1	*	*	*	0	0	1	0	Write: data for registers(ch.0)
1	*	*	0	*	0	1	0	Write: data for registers(ch.1)
1	*	0	*	*	0	1	0	Write: data for registers(ch.2)
1	0	*	*	*	0	1	0	Write: data for registers(ch.3)
1	1	1	1	0	1	0	1	Read: status register(ch.0)
1	1	1	0	1	1	0	1	Read: status register(ch.1)
1	1	0	1	1	1	0	1	Read: status register(ch.2)
1	0	1	1	1	1	0	1	Read: status register(ch.3)
1	*	*	*	0	1	1	0	Write: command(ch.0)
1	*	*	0	*	1	1	0	Write: command(ch.1)
1	*	0	*	*	1	1	0	Write: command(ch.2)
1	0	*	*	*	1	1	0	Write: command(ch.3)

4-1-2. Normal Addressing Mode(DRCTCE="0")

In this mode, A pair of AD/$\overline{CE}$3 and AD/$\overline{CE}$2 is used as the chip enable input for the ZEN2044F and the lower two bits(AD/$\overline{CE}$1 and AD/$\overline{CE}$0) specify the target channel.

Table 3

DRCTCE	AD/$\overline{CE}$3	AD/$\overline{CE}$2	AD/$\overline{CE}$1	AD/$\overline{CE}$0	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Function
0	1	1	*	*	*	*	*	Disable(data bus: High-impedance)
0	0	1	*	*	*	*	*	Disable(data bus: High-impedance)
0	1	0	*	*	*	*	*	Disable(data bus: High-impedance)
0	0	0	0	0	0	0	1	Read: latch register(ch.0)
0	0	0	0	1	0	0	1	Read: latch register(ch.1)
0	0	0	1	0	0	0	1	Read: latch register(ch.2)
0	0	0	1	1	0	0	1	Read: latch register(ch.3)
0	0	0	0	0	0	1	0	Write: data for registers(ch.0)
0	0	0	0	1	0	1	0	Write: data for registers(ch.1)
0	0	0	1	0	0	1	0	Write: data for registers(ch.2)
0	0	0	1	1	0	1	0	Write: data for registers(ch.3)
0	0	0	0	0	1	0	1	Read: status register(ch.0)
0	0	0	0	1	1	0	1	Read: status register(ch.1)
0	0	0	1	0	1	0	1	Read: status register(ch.2)
0	0	0	1	1	1	0	1	Read: status register(ch.3)
0	0	0	0	0	1	1	0	Write: command(ch.0)
0	0	0	0	1	1	1	0	Write: command(ch.1)
0	0	0	1	0	1	1	0	Write: command(ch.2)
0	0	0	1	1	1	1	0	Write: command(ch.3)

4-2. Command mode

The ZEN2044F has the following two system modes. First of all, it is necessary to determine which mode you use(Mode 0 or Mode 1). The system mode is fixed by executing the system mode set command (90H or 91H).

4-2-1. Mode 0 [after executing command(90H) or system reset]

$\overline{\text{EXTB}n}$ is set as a universal input terminal U. One set of the refrence register and the comparator is available.

4-2-2. Mode 1 [after executing command(91H)]

$\overline{\text{EXTB}n}$ is set as an output terminal. Both $\overline{\text{EXTA}n}$ and $\overline{\text{EXTB}n}$ can be controled by the instruction sets of Mode 1. And two sets of the refrence register and the comparator are available.

4-3. Selection of counter operation mode

The type of counter pulse and the mode of clearing counter by Z input depend on the condition of UD/$\overline{\text{AB}}n$, SELn0, SELn1 and SELn2(these signals should be static and not set by the CPU). Refer to Table 4 for detail.

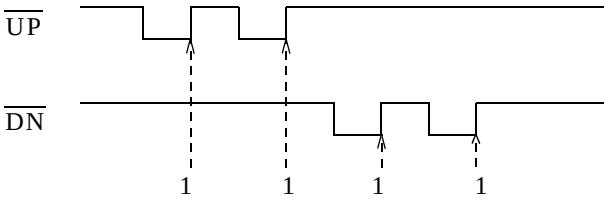
Table 4

UD/$\overline{\text{AB}}n$	SELn2	SELn1	SELn0	Pulse input(Edge eval.)	Clear mode
1	*	*	*	Up/down pulse	Asynchronous clear
0	0	0	0	Phase-shifted(single)	Synchronous clear
	0	0	1	Phase-shifted(double)	
	0	1	0	Phase-shifted(quad)	
	1	0	0	Phase-shifted(single)	Asynchronous clear
	1	0	1	Phase-shifted(double)	
	1	1	0	Phase-shifted(quad)	
	0	1	1	Single pulse(single)	Asynchronous clear
	1	1	1	Single pulse(double)	

4-4. Pulse count timing(Edge evaluation)

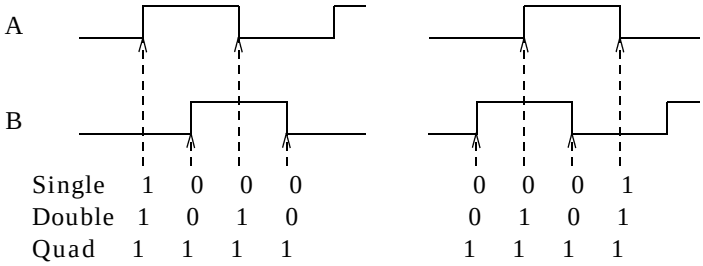
The following diagrams show how an edge of the input pulse is evaluated in each count operation mode. "1" means counting and "0" means no operation.

Up/down pulse input

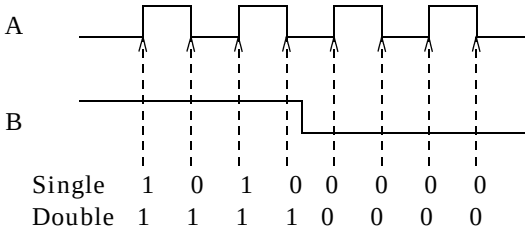


Note) Both $\overline{UP}$ and $\overline{DN}$ should not be "0" at once.

Phase-shifted pulse input



Single pulse input



Note) B is used as the count enable signal.

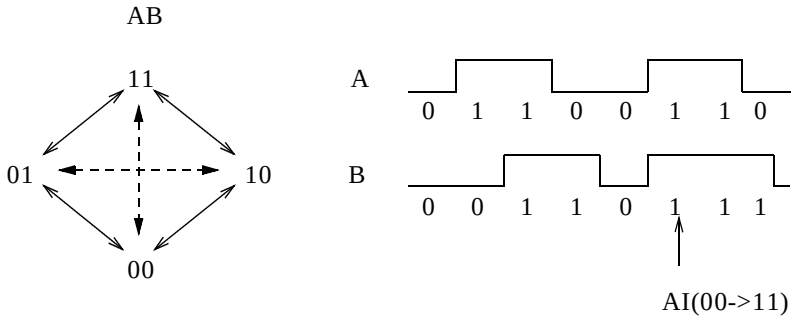
4-5. Detection of abnormal input

The ZEN2044F has the function to check whether the phase-shifted pulse inputs show a correct transition state(shown in Fig.1 with ⟷ mark) or not.

When an abnormal transition state(shown in Fig.1 with ◄- - ► mark) occurs, the Abnormal Input flag(D7 bit of the status register) is set. Some causes of the abnormal transition state are as follows:

(1) The frequencies of phase shifted pulse inputs exceed the one fourth of the system clock frequency. In this case, the transition state cannot be sampled correctly.
(2) When the line-noises are sampled, the ZEN2044F detects the abnormal transition.

Fig.1 State transitions and an example of detecting the abnormal input



4-6. Default values of internal registers after reset

After RESET is asserted, the values of the internal registers and the system mode are set according to Table 6.

Table 6

Regsiter/Mode	The reset value	Regsiter/Mode	The reset value
Counter	000000H	System mode	Mode 0
Preload reg.	keeping the value before reset	Reference reg. A	keeping the value before reset
Latch reg.	keeping the value before reset	Reference reg. B	keeping the value before reset
Command reg. D7(LD) D6(ZE1) D5(ZE0) D4(LT) D3(RS1) D2(RS0) D1(BS1) D0(BS0)	 0 (NOP) 1 ZNE 0 0 (NOP) 0 Up/down counter 0 0 Low byte 0		
Status reg. D7(AI) D6(Z) D5(A) D4(B) D3(DTR) D2(U/D) D1(EQA) D0(U)	 0 Depending on input Z/CLR Depending on input A/UP Depending on input B/DN 0 0 1 Depending on input U		

5. Registers

The ZEN2044F has the following registers at each cannel.

A command register for controling the action of the counter.[write only]
A status register for indicating the internal state.[read only]
A preload register for storing the counter value to be loaded.[write only]
A reference register for storing the value to be compared with the counter.[write only]
A latch register for storing the counter value to be read by the CPU.[read only]

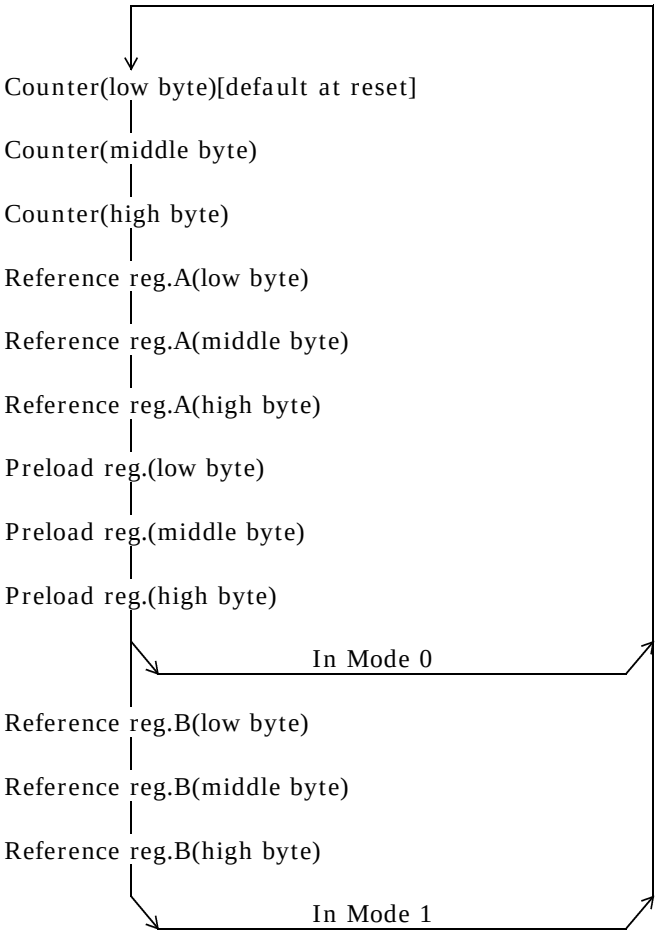
Note) The counter value can be directly wrote without storing it in the preload register but we don't recommend it.

5-1. Access pointer

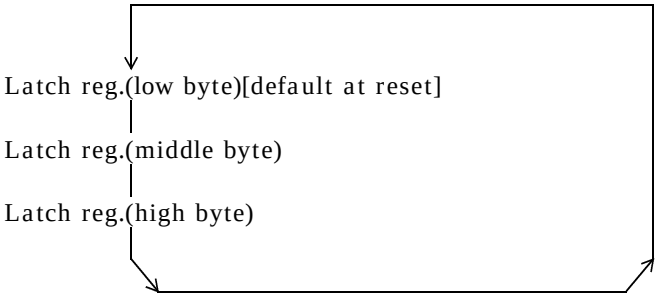
Before you write a data to a certain register, you should set an access pointer properly. But the ZEN2044F has an auto-incremental function of the access pointer. So when you write data in the following sequence, what you have to set is only a starting point. Also when reading the latch register, the target byte(low, middle or high) is changed automatically.

Fig.2

For writes



For reads



5-2. System mode set command

This is the command word to select system mode. If you use the conter in Mode 1, you need to write the Mode 1 select command at first because the Mode 0 is the default setting at reset.

Table 6 Format of system mode set command

D7	D6	D5	D4	D3	D2	D1	D0	HeX	Operation
1	0	0	1	0	0	0	0	90	Mode 0 select[default]
1	0	0	1	0	0	0	1	91	Mode 1 select

(1) Mode 0[default]

$\overline{EXTA}n$ is set as a comparator output ($\overline{EQA}n$) and $\overline{EXTB}n$ is set as a universal input U.

(2) Mode 1

$\overline{EXTB}n$ is set as an output. Both $\overline{EXTA}n$ and $\overline{EXTB}n$ can be programed. Please refer to Mode1 register format in detail.

5-3. Command register format(common to Mode 0 and Mode 1)

This is the command word for selecting register, selecting byte, latching counter, loading preloaded value and controling action of Z phase input.

Table 7 Field format of command register(common to Mode 0 and Mode 1)

D7	D6	D5	D4	D3	D2	D1	D0
LD	ZE1	ZE0	LT	RS1	RS0	BS1	BS0

BS1,BS0(Byte Select)

The registers(preload, reference and latch) and the up/down counter have 24 bit length but the CPU bus is 8 bit in the ZEN2044F. The BS1 and BS0 determine the target byte(high byte, middle byte or low byte) when the CPU accesses ZEN2044F.

RS1,RS0(Register Select)

RS1 and RS0 specify the register to be accessed from among the three registers(preload, reference and latch) and the up/down counter.

LT(Latch)

This bit is used to store the value of the up/down counter into the latch register.

ZE1, ZE0(Z phase input control)

ZE1 and ZE0 control the way of clearing the counter by Z phase input. One of "ignoring", "once" or "every time" can be selected.

LD(Load)

This bit is used to transmit the data which is stored in the preload register to the up/down counter.

Note 1)

Do not execute Load and Latch operations at once.

Note 2)

When Load or Latch command is executed, the external pins, $\overline{LT}$ and $\overline{LD}$, must be fixed at "1" .

Table 8 Format of command register

D7	D6	D5	D4	D3	D2	D1	D0	Operation
*	*	*	*	0	0	*	*	Selecting up/down counter[default]
*	*	*	*	0	1	*	*	Selecting reference reg. A
*	*	*	*	1	*	*	*	Selecting preload reg.(in Mode 0)
*	*	*	*	1	0	*	*	Selecting preload reg.(in Mode 1)
*	*	*	*	1	1	*	*	Selecting reference reg. B(in Mode 1)
*	*	*	*	*	*	0	0	Selecting low byte[default]
*	*	*	*	*	*	0	1	Selecting middle byte
*	*	*	*	*	*	1	*	Selecting high byte
*	0	0	*	*	*	*	*	Keeping current setting as to Z phase input
*	0	1	*	*	*	*	*	Setting Z phase pulse ineffective
*	1	0	*	*	*	*	*	Setting only next Z phase pulse effective
*	1	1	*	*	*	*	*	Setting every Z phase pulse effective
0	*	*	0	*	*	*	*	No operation as to Load/Latch
0	*	*	1	*	*	*	*	Latching the count value
1	*	*	0	*	*	*	*	Loading the preload value
1	0	0	1	*	*	*	*	Command ID
1	*	*	1	*	*	*	*	Inhibit(except Command ID)

Note 1)
"*" stands for "don't care".
Note 2)
Command ID indicates system mode select or Mode 1 command.

5-4. Command register format(Mode 1)

Only when the system mode is Mode 1, the command group of Mode 1 becomes effective. The reference register B can be accessed in Mode 1 only and the D0 of the status register shows the result of the comparator B. $\overline{EXTA}n$ can be programmed to output one of three signals($\overline{EQA}n$,$\overline{EQA}n$ + $\overline{EQB}n$ or $\overline{INTEQA}n$). $\overline{EXTB}n$ can be programmed to output one of three signals($\overline{EQB}n$,$\overline{INTEQB}n$ or $\overline{INTAI}n$).

$\overline{EQA}n$ is the result of comparing the reference register A to the up/down counter.
$\overline{EQB}n$ is the result of comparing the reference register B to the up/down counter.
$\overline{EQA}n$+$\overline{EQB}n$ is the logical sum(OR) of $\overline{EQA}n$ and $\overline{EQB}n$.
$\overline{INTEQA}n$ is the hold output of $\overline{EQA}n$.
$\overline{INTEQB}n$ is the hold output of $\overline{EQB}n$.
$\overline{INTAI}n$ is holding low once an abnormal transition state is detected.

Above three hold outputs can be used for an interrupt request. And they have three functions, enabling, disabling and reset. AI reset command resets $\overline{EXTB}n$ output and initializes the phase discrimination circuit.

Table 9 Format of command register(mode1)

D7	D6	D5	D4	D3	D2	D1	D0	HEX	Operation
1	0	0	1	0	0	1	0	92	Inhibit
1	0	0	1	0	0	1	1	93	Inhibit
1	0	0	1	0	1	0	0	94	$\overline{EQAn}$ + $\overline{EQBn}$ -> $\overline{EXTAn}$
1	0	0	1	0	1	0	1	95	$\overline{EQAn}$ -> $\overline{EXTAn}$ [default]
1	0	0	1	0	1	1	0	96	Inhibit
1	0	0	1	0	1	1	1	97	$\overline{EQBn}$ -> $\overline{EXTBn}$ [default]
1	0	0	1	1	0	0	0	98	$\overline{INTEQAn}$ command reset
1	0	0	1	1	0	0	1	99	$\overline{INTEQBn}$, $\overline{INTAIn}$ command reset
1	0	0	1	1	0	1	0	9A	$\overline{INTAIn}$ -> $\overline{EXTBn}$ disabling
1	0	0	1	1	0	1	1	9B	$\overline{INTAIn}$ -> $\overline{EXTBn}$ enabling
1	0	0	1	1	1	0	0	9C	$\overline{INTEQAn}$ -> $\overline{EXTAn}$ disabling
1	0	0	1	1	1	0	1	9D	$\overline{INTEQAn}$ -> $\overline{EXTAn}$ enabling
1	0	0	1	1	1	1	0	9E	$\overline{INTEQBn}$ -> $\overline{EXTBn}$ disabling
1	0	0	1	1	1	1	1	9F	$\overline{INTEQBn}$ -> $\overline{EXTBn}$ enabling

Note) $\overline{EXTAn}$ and $\overline{EXTBn}$ cannot share an interrupt line with outputs of other IC because they don't have 3st output.

5-5. Status register

The status register is used to monitor internal conditions. Please refer to "4-1. CPU Interface" for the method of reading out this register.

Table 10 Format of status register

Bit	Symbol	Active	Description
D7	AI	High	Abnormal input detection flag(only phase-shifted pulse input) A value of "1" indicates that the abnormal transition state of phase shifted inputs is detected.
D6	Z	None	Z/CLR*n* input monitor This bit indicates the value of Z/CLR*n* input that is sampled at the rising edge of CLK.
D5	A	None	A/$\overline{\text{UP}n}$ input monitor This bit indicates the value of A/$\overline{\text{UP}n}$ input that is sampled at the rising edge of CLK.
D4	B	None	B/$\overline{\text{DN}n}$ input monitor This bit indicates the value of B/$\overline{\text{DN}n}$ input that is sampled at the rising edge of CLK.
D3	DTR	High	Data ready flag of the latch register A value of "1" indicates the counter data has been transfered to the latch register. This flag is cleared by reading the data of the latch register.
D2	U/$\overline{\text{D}}$	None	Direction of counting The current counting direction is indicated. "1" means up count and "0" means down count.
D1	$\overline{\text{EQA}}$	Low	Coincident flag of comparator A A value of "0" indicates the data of counter and comparator A is coincident.
D0	U [Mode 0]	None	Universal input U($\overline{\text{EXTB}n}$) input monitor This bit indicates the value of $\overline{\text{EXTB}n}$ input. This signal is not sampled but directly monitored.
	$\overline{\text{EQB}}$ [Mode 1]	Low	Coincident flag of comparator B A value of "0" indicates the data of counter and comparator B is coincident.

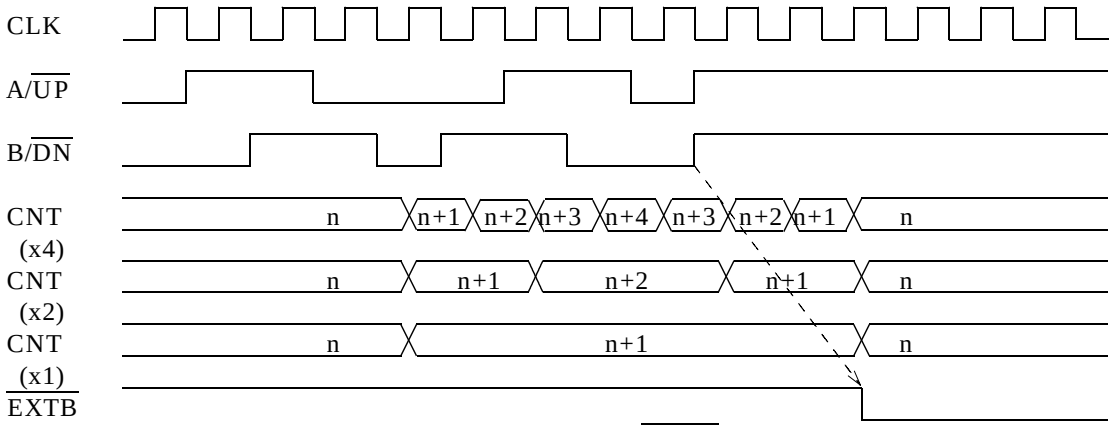
6. Internal timing(for reference only)

The internal timings of the ZEN2044F are as follows.

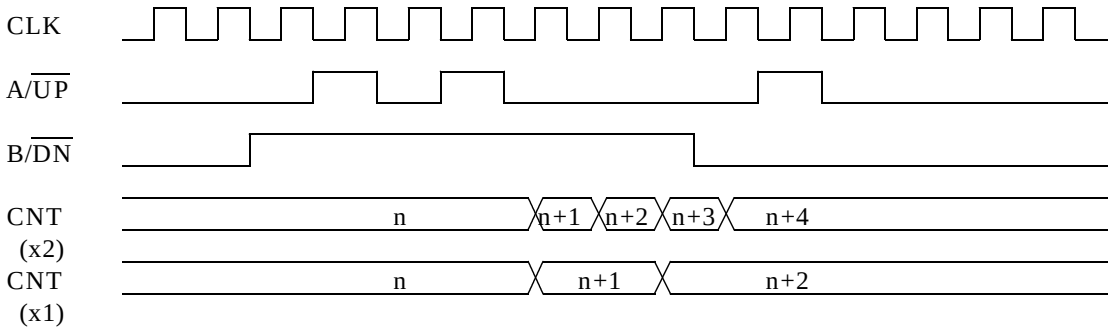
Note)
CNT stands for the value of the internal counter.
LDR stands for the value of the preload register.
LTR stands for the value of the latch register.
CMPRA stands for the value of the reference register A.

6-1. Counting up/down

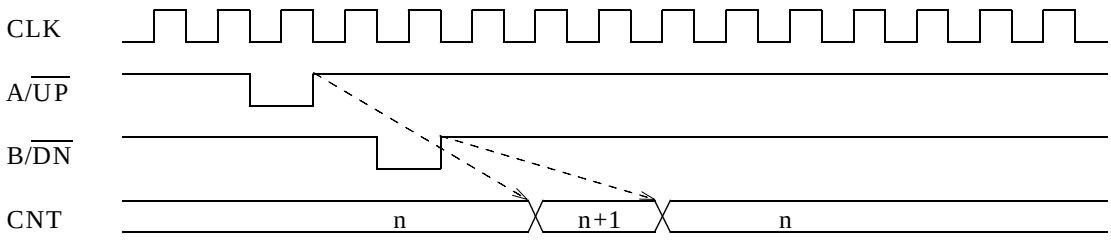
6-1-1. Two phase-shifted pulse mode(DIR="1")



6-1-2. Single pulse mode(DIR="1")

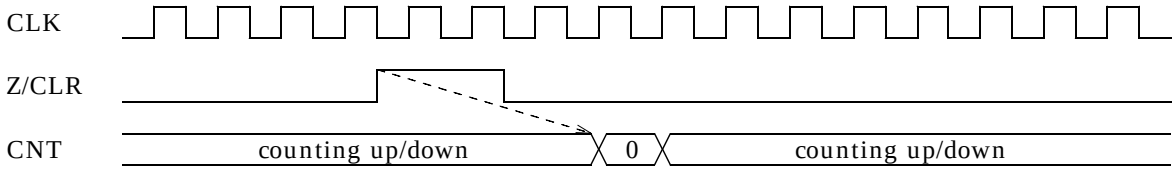


6-1-3. Up/down pulse mode(DIR="1")

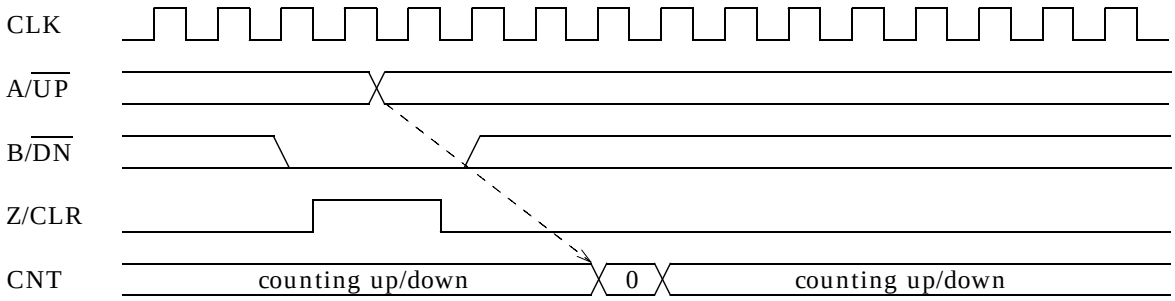


6-2. Clearing counter

6-2-1. Asynchronous mode(Detecting the rising edge of Z/CLR)

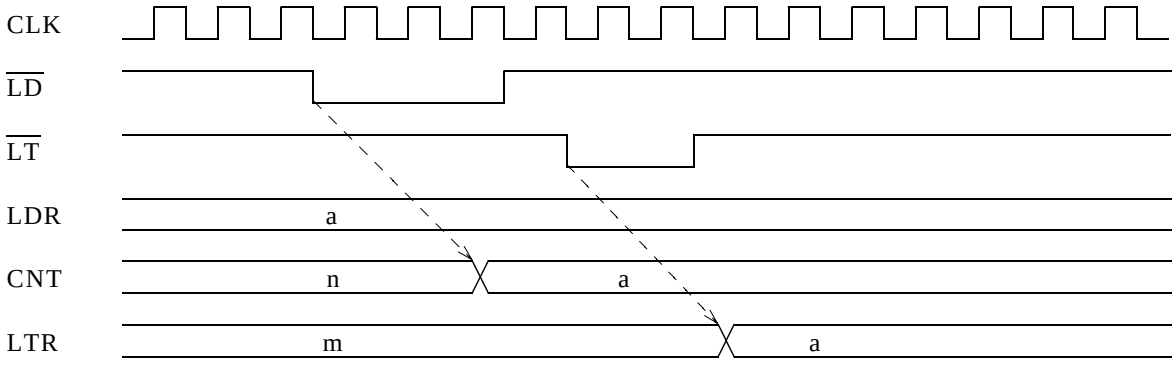


6-2-2. Synchronous mode(Detecting the rising or falling edge of A/$\overline{UP}$ when Z/CLR is "1" and B/$\overline{DN}$ is "0")



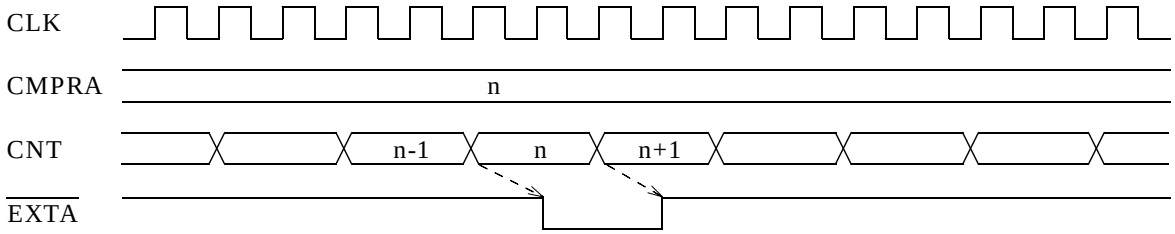
6-3. Loading or latching counter value

6-3-1. External loading or latching

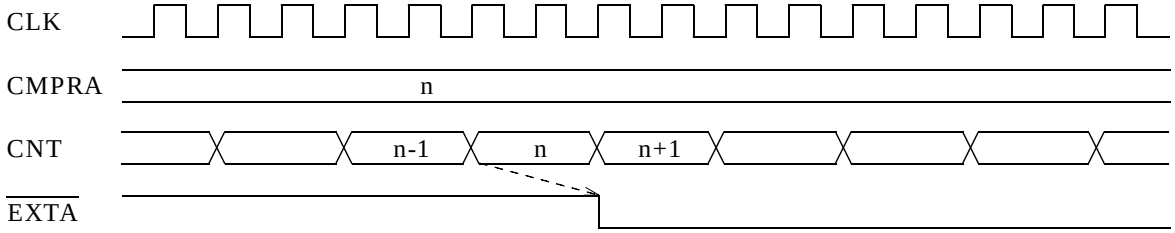


6-4. Detecting coincidence

6-4-1. Momentary coincident output



6-4-2. Hold coincident output



Note)
$\overline{\text{EXTB}}$ has the same timing as $\overline{\text{EXTA}}$ in Mode 1.

7. Electrical specifications

7-1. Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	Vdd	-0.3 to +7.0	V
Input voltage	Vin	-0.3 to VDD+0.3	V
Output voltage	Vout	-0.3 to VDD+0.3	V
Input current	Iin	-10 to +10	mA
Storage temperature	Tstg	-40 to +125	°C

7-2. Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	Vdd	4.75	5.00	5.25	V
Operation temperature	Topr	0	-	+70	°C

7-3. DC chracteristics(at the recomended operating conditions)

Parameter	Symbol	Conditions	Min	Max	Unit
Input "High" voltage	Vih		2.2		V
Input "Low" voltage	Vil			0.8	V
Input "High" current	Iih	Vin=Vdd	-10	10	uA
Input "Low" current	Iil	Vin=Vss	-10	10	uA
Output "High" voltage	Voh	Ioh=-4mA	2.4		V
Output "Low" voltage	Vol	Iol=4mA		0.4	V
Standby current	Idds	Vin=Vdd or Vss		17	uA
Operation current	Iddo			60	mA

Note)
Ioh is Output "High" current and Iol is Output "Low" current.

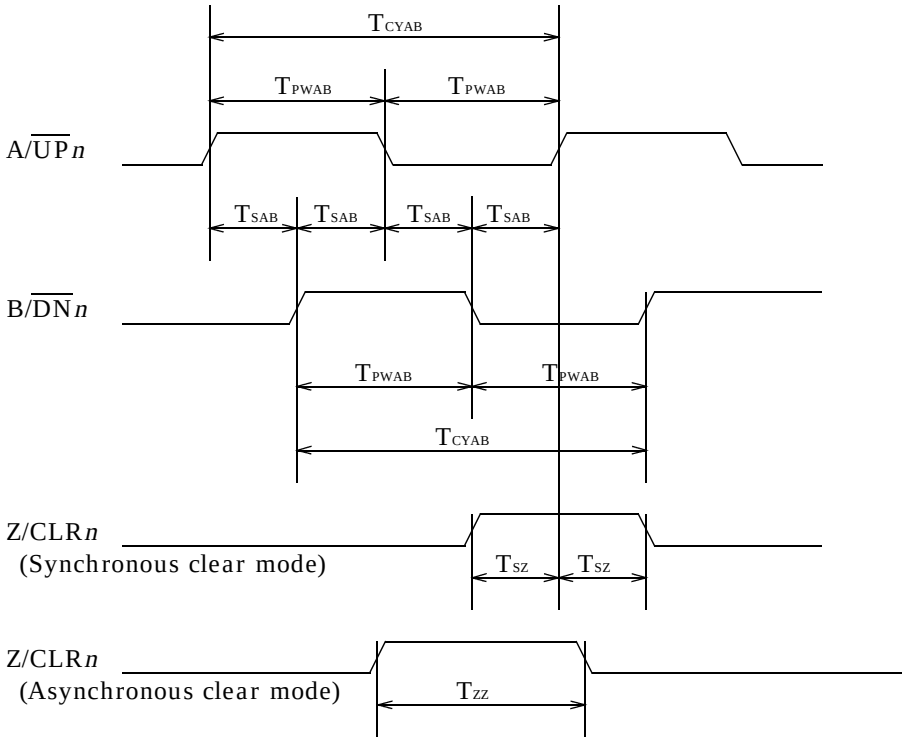
7-4. AC chracteristics

Parameter	Symbol	Min	Max	Unit
C/$\overline{D}$,AD/$\overline{CE}n$ setup time(to D7-D0)	T_{AW}	0		nS
C/$\overline{D}$,AD/$\overline{CE}n$ hold time(to D7-D0)	T_{WA}	0		nS
Data setup time(to WR)	T_{DW}	30		nS
Data hold time(to WR)	T_{WD}	3		nS
$\overline{WR}$ pulse width	T_{WW}	25		nS
$\overline{WR}$ recovery time[1]	T_{WRC}	T_{CY}*5		nS
C/$\overline{D}$,AD/$\overline{CE}n$ setup time(to RD)	T_{AR}	0		nS
C/$\overline{D}$,AD/$\overline{CE}n$ hold time(to RD)	T_{RA}	5		nS
$\overline{RD}$ pulse width	T_{RR}	25		nS
Data access time(from RD)	T_{RD}		20	nS
Data float time(from RD)	T_{DF}	4		nS
$\overline{RD}$ recovery time[1]	T_{RRC}	T_{CY}*5		nS
Clock high/low pulse width	T_{CP}	15		nS
Clock cycle time	T_{CY}	30		nS
Reset pulse width	T_{RST}	T_{CY}*2		nS
Reset recovery time	T_{RSRC}	T_{CY}*5		nS
$\overline{LDn}$ pulse width	T_{LDW}	25		nS
$\overline{LTn}$ pulse width	T_{LTW}	25		nS
$\overline{EXTBn}$ set time(from CLK)[2]	T_{SEB}		15	nS
$\overline{EXTBn}$ float time(from CLK)[3]	T_{FEB}		15	nS
$\overline{EXTAn}$, $\overline{EXTBn}$ fix time(from CLK)	T_{EXF}		15	nS
A/$\overline{UP}n$, B/$\overline{DN}n$ cycle time[4]	T_{CYAB}	T_{CY}*4+32		nS
A/$\overline{UP}n$, B/$\overline{DN}n$ high/low level time[4]	T_{PWAB}	T_{CY}*2+16		nS
A/$\overline{UP}n$, B/$\overline{DN}n$ phase difference time[4]	T_{SAB}	T_{CY}+8		nS
Z/CLRn high level width[5]	T_{SZ}	T_{CY}+8		nS
Z/CLRn pulse width[6]	T_{ZZ}	T_{CY}+8		nS
A/$\overline{UP}n$ setup time(to B/$\overline{DN}n$)[7]	T_{SS}	T_{CY}+8		nS
A/$\overline{UP}n$ high/low level time[7]	T_{AHL}	T_{CY}+8		nS
A/$\overline{UP}n$ cycle time[7]	T_{ACY}	T_{CY}*2+16		nS
A/$\overline{UP}n$, B/$\overline{DN}n$ cycle time[8]	T_{UDCY}	T_{CY}*2+16		nS
A/$\overline{UP}n$, B/$\overline{DN}n$ high/low level time[8]	T_{U}	T_{CY}+8		nS

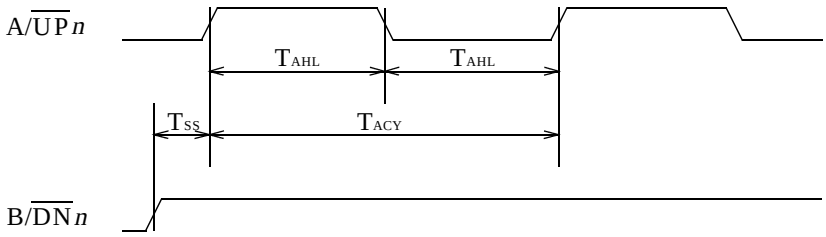
Note)
[1] Required interval clock cycles to access the ZEN2044F
[2] At executing Mode 1 select command
[3] At executing Mode 0 select command
[4] Two phase-shfted pulse mode
[5] Synchronous clear mode
[6] Asynchronous clear mode
[7] Single pulse mode
[8] Up/down pulse mode

7-5. Timing diagrams

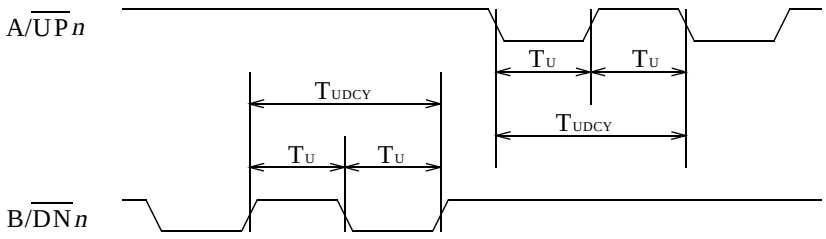
7-5-1. Two phase-shifted pulse input timing



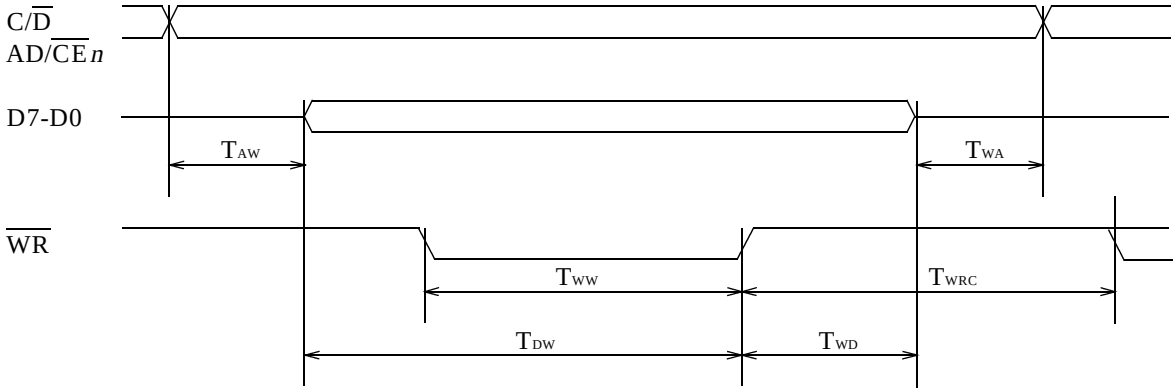
7-5-2. Single pulse input timing



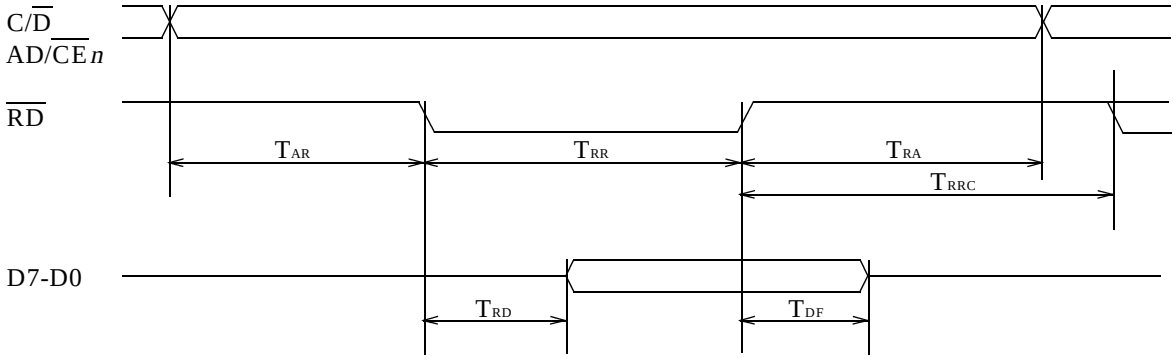
7-5-3. Up/down pulse input timing



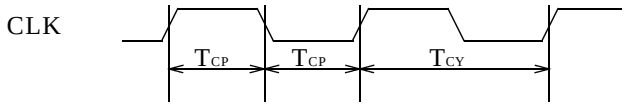
7-5-4. Write cycle timing



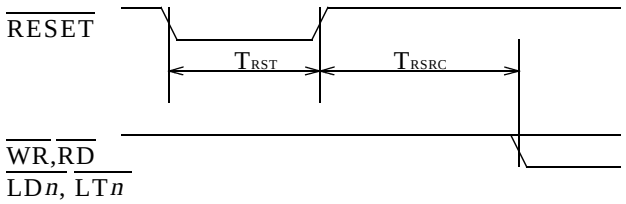
7-5-5. Read cycle timing



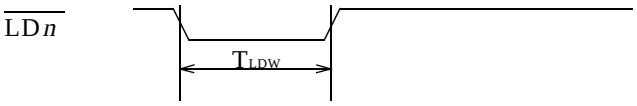
7-5-6. System clock timing



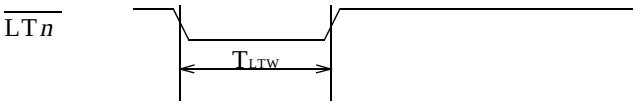
7-5-7. System reset timing



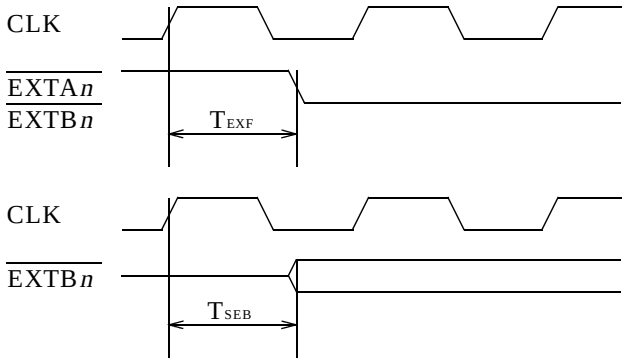
7-5-8. Load pulse input timing



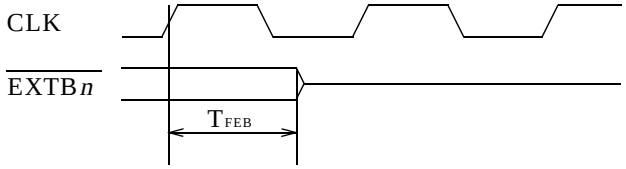
7-5-9. Latch pulse input timing



7-5-10. $\overline{\text{EXTA}n}$, $\overline{\text{EXTB}n}$ output timing

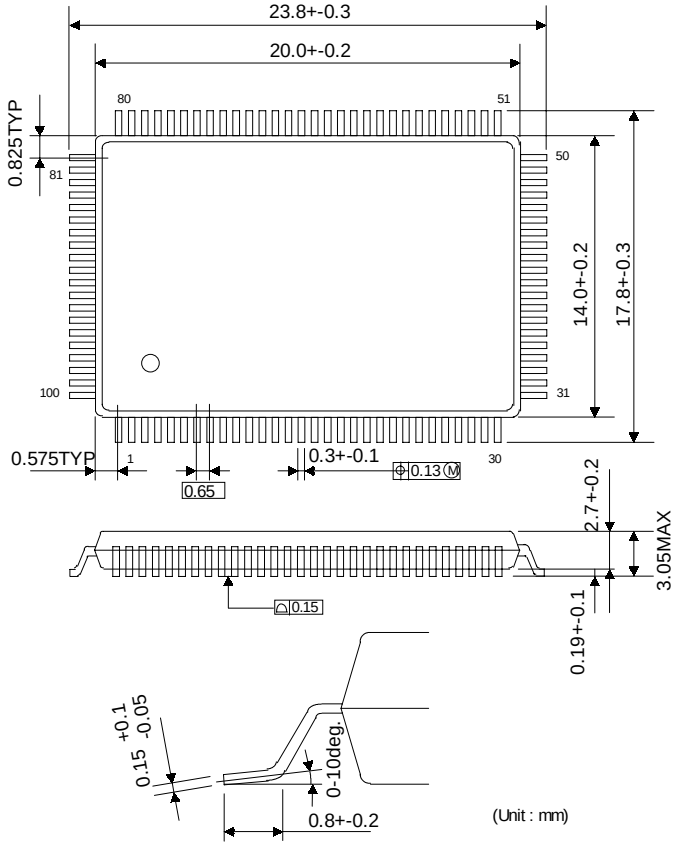


Note)
At executing Mode 1 select command($\overline{\text{EXTB}n}$ is changed from input into output)



Note)
At executing Mode 0 select command($\overline{\text{EXTB}n}$ is changed from output into input)

8. Package Outlines



Note

This document is the user manual for the ZEN2044F and all information is applicable for reference only. Copying the whole contents or any part of this document is strictly prohibited.

ZENIC reserves the right to change or alter this information or prices of specfied products at any time without any notice. ZENIC advises its customers to obtain the latest version of device specifications.

ZENIC does not assume any liability arising out of the application or use of any product or circuit described herein; nor does it convey any license under its patent right or the rights of others.

ZENIC products are not designed, intended, or authrized for use as componets in systems intended for surgical implant into the body, or other applications inteded to support or sustain life, or for any other application in which the failure of the ZENIC products could create a situation where personal injury or death may occur.

ZENIC Inc. URL http://www.zenic.co.jp/
1-17-14, Ogaya Otsu Shiga 520-2144, JAPAN
Fax. +81-77-543-9431 Phone. +81-77-543-2101 E-mail support@zenic.co.jp