WM2130

10-bit 30MSPS Analogue-To-Digital Converter

Production Data, April 2001, Rev 1.2

DESCRIPTION

The WM2130 is a high speed 10-bit analogue-to-digital converter and operates with independent analogue and digital supplies of 3V to 5.5V. This device includes a high bandwidth sample and hold and internal voltage references. Conversion is controlled by a single clock input.

The differential-input sample and hold input gives excellent common-mode noise immunity and low distortion. The device can also be driven in a single ended fashion.

The device provides internal reference voltages for setting the ADC full-scale range without the requirement for external circuitry. The WM2130 can also accept external reference levels for applications where higher precision references are required.

The WM2130 has also been designed to offer a speed upgrade to users of the AD876 and a replacement for the AD9200 and AD9202 devices. The WM2130 operates as an AD876 in those design slots but at speeds of up to 50% faster.

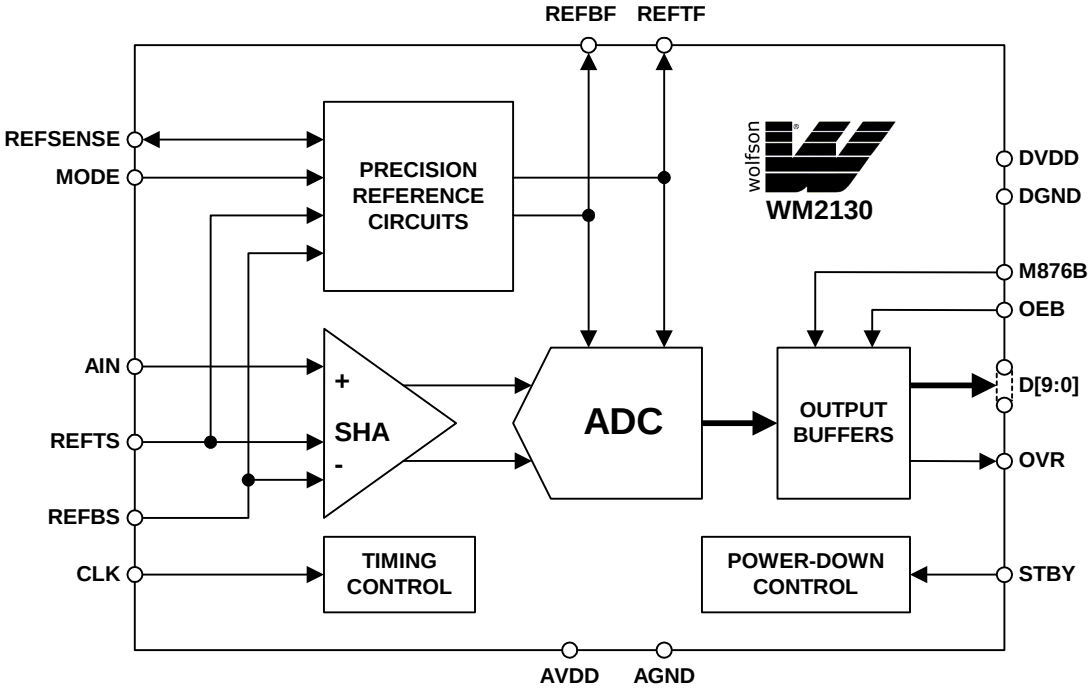
FEATURES

- 10-bit resolution ADC
- 30MSPS conversion rate
- Wide input bandwidth (150 MHz full-power bandwidth) sample and hold input amplifier
- Independent analogue and digital supplies
- Adjustable internal voltage references
- Out of range indicator
- Low power: 87mW typical at 3V supplies
- Powerdown mode to 3mW typical
- 28-pin TSSOP package

APPLICATIONS

- Set Top Box (STB)
- IF and Baseband Digitisation
- Medical Imaging
- High speed data acquisition

BLOCK DIAGRAM



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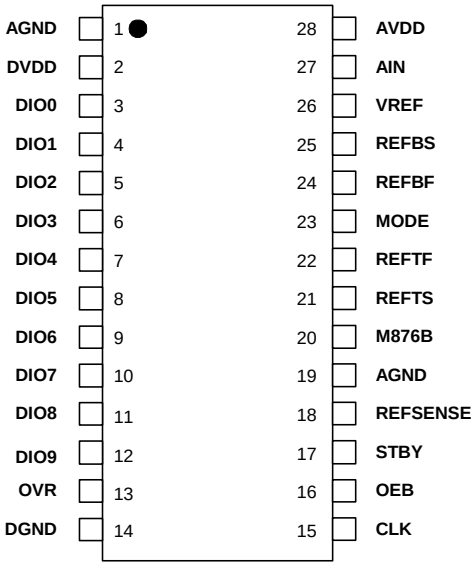
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2130CDT/V	0 to +70°C	28-pin TSSOP
WM2130IDT/V	-40 to +85°C	28-pin TSSOP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AGND	Ground	Analogue Ground
2	DVDD	Supply	Positive Digital Supply
3	DO0	Digital Output	Digital output bit 0 (lsb)
4	DO1	Digital Output	Digital output bit 1
5	DO2	Digital Output	Digital output bit 2
6	DO3	Digital Output	Digital output bit 3
7	DO4	Digital Output	Digital output bit 4
8	DO5	Digital Output	Digital output bit 5
9	DO6	Digital Output	Digital output bit 6
10	DO7	Digital Output	Digital output bit 7
11	DO8	Digital Output	Digital output bit 8
12	DO9	Digital Output	Digital output bit 9 (msb)
13	OVR	Digital Output	Over-range output (tri-statable)
14	DGND	Ground	Digital Ground
15	CLK	Digital Input	Clock input
16	STBY	Digital Input	Powerdown control
17	OEB	Digital Input	Output enable bar – low to enable DO[9:0] and OVR
18	REFSENSE	Analogue Input/Output	VREF mode control
19	AGND	Ground	Negative Analogue Supply
20	M876B	Digital Input	AD876 mode select
21	REFTS	Analogue Input	Top reference sense
22	REFTF	Analogue Input/Output	Top reference force
23	MODE	Digital Input	Input mode select
24	REFBF	Analogue Input/Output	Bottom reference force
25	REFBS	Analogue Input	Bottom reference sense
26	VREF	Analogue Input/Output	Internal reference output
27	AIN	Analogue Input	Analog Input
28	AVDD	Supply	Positive Analogue Supply

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per specifications IPC/JEDEC J-STD-020A and JEDEC A113-B, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION	MIN	MAX
Digital supply voltage, DVDD to DGND	-0.3V	+6.5V
Analogue supply voltage, AVDD to AGND	-0.3V	+6.5V
Supply voltage difference, AVDD to DVDD	-6.5V	+6.5V
Ground difference, AGND to DGND	-0.3V	+0.3V
Digital inputs voltage range (DO[9:0], STBY, OEB, M876B)	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs (REFTS, REFBS, REFTF, REFBF, AIN, VREF, REFSENSE, CLK, MODE)	AGND - 0.3V	AVDD + 0.3V
Storage temperature	-65°C	+150°C
Soldering lead temperature, 1.6mm (1/16 inch) from package body for 10 seconds		+300°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Digital supply range	DVDD		3.0	3.3	5.5	V
Analogue supply range	AVDD		3.0	3.3	5.5	V
Clock frequency	f_{CLK}		5		30	MHz
Clock duty cycle			45	50	55	%
Operating Free Air Minimum Temperature	T_{MIN}	WM2130C	0			°C
		WM2130I	-40			°C
Operating Free Air Maximum Temperature	T_{MAX}	WM2130C			70	°C
		WM2130I			85	°C

ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% Duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy						
Integral nonlinearity	INL			±1.0	±2.0	LSB
Differential nonlinearity	DNL			±0.3	±1.0	LSB
Offset error				0.4	2.0	% of FS
Gain error				1.4	3.5	% of FS
Missing codes			No missing codes guaranteed			
Analogue Input Signal to AIN pin						
Input signal range		MODE = AGND	REFBS		REFTS	V
		MODE = AVDD / 2, V_{CMCS} fixed	V_{CMCS} – VREF/2		V_{CMCS} + VREF/2	V
		MODE = AVDD	REFBS		REFTS	V
AIN voltage limits			AGND		AVDD	V
Switched input capacitance				1.2		pF
Analogue input bandwidth				150		MHz
DC leakage current		± Full-scale input		±60		µA
Aperture delay	t_A			4		ns
Aperture jitter				2		ps rms
Conversion Characteristics						
Conversion frequency	f_{CLK}		5		30	MHz
Pipeline delay				3		CLK cycles
Aperture delay	t_A			4		ns
Aperture jitter				2		ps rms
Dynamic Performance						
Effective number of bits	ENOB	f_{IN} = 3.5MHz	8.4	9		dB
		f_{IN}=3.5MHz, AVDD 5V		9		
		f_{IN} = 15MHz		7.8		
		f_{IN}=15MHz, AVDD 5V		7.7		
Spurious free dynamic range	SFDR	f_{IN} = 3.5MHz	56	60.6		dB
		f_{IN}=3.5MHz, AVDD 5V		64.6		
		f_{IN} = 15MHz		48.5		
		f_{IN}=15MHz, AVDD 5V		53		
Total Harmonic Distortion	THD	f_{IN} = 3.5MHz		-60	-56	dB
		f_{IN}=3.5MHz, AVDD 5V		-66.9		
		f_{IN} = 15MHz		-47.5		
		f_{IN}=15MHz, AVDD 5V		-53.1		
Signal to noise ratio	SNR	f_{IN} = 3.5MHz	53	57		dB
		f_{IN}=3.5MHz, AVDD 5V		56		
		f_{IN} = 15MHz		53.1		
		f_{IN}=15MHz, AVDD 5V		49.4		
Signal to noise and distortion ratio	SINAD	f_{IN} = 3.5MHz	52.5	56		dB
		f_{IN}=3.5MHz, AVDD 5V		56		
		f_{IN} = 15MHz		48.6		
		f_{IN}=15MHz, AVDD 5V		48.1		

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% Duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Inputs / Outputs in Top/Bottom Mode (MODE=AVDD)						
Bottom reference voltage applied to REFBS			0		AVDD – 1	V
Top reference voltage applied to REFTS			1		AVDD	V
Differential reference input (REFTS – REFBS)	V_{TB}		1		2	V
Switched input capacitance on REFBS				0.6		pF
Switched input capacitance on REFTS				0.6		pF
REFBF output voltage				(AVDD - V_{TB})/2		V
REFTF output voltage				(AVDD + V_{TB})/2		V
Analogue Reference Inputs / Outputs in Centre-Span Mode (MODE=AVDD/2)						
Reference voltage derived or applied to VREF			1		2	V
REFBF output voltage				(AVDD - VREF)/2		V
REFTF output voltage				(AVDD + VREF)/2		V
Analogue Reference Inputs / Outputs in Full External Reference Mode (MODE=AGND) (Note 1)						
Differential reference voltage applied (REFTF – REFBF)			1		2	V
Reference input common mode		AVDD = 3.0V	1.3	1.5	1.7	V
(REFTF + REFBF) / 2		AVDD = 5.0V	2.0	2.5	3.0	V
Reference input resistance				680		Ω
VREF Input / Output specifications						
Internal 1V reference to VREF		REFSENSE = VREF	0.95	1.0	1.05	V
Internal 2V reference to VREF		REFSENSE = AGND	1.9	2.0	2.1	V
External reference applied to VREF pin in centre-span mode		REFSENSE = AVDD, MODE = AVDD / 2	1		2	V
Input impedance in centre-span mode		REFSENSE = AVDD, MODE = AVDD / 2		18		kΩ
Power Supplies						
Operating supply current	$I_{AVDD} + I_{DVDD}$	AVDD = DVDD = 3V, MODE = AGND		29	40	mA
		AVDD = DVDD = 5V		50		
Standby Power	P_{STBY}	AVDD = DVDD = 3V, MODE = AGND		3	5	mW
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}	(Note 2)			0.2 x VDD	V
Input HIGH level	V_{IH}	(Note 2)	0.8 x VDD			V

Notes

1. In full external reference mode the REFTF and REFTS pins should be shorted together, and the REFBF and REFBS pins should be shorted together. Please refer to device operation examples in the device description section of the datasheet.
2. Digital input and output levels refer to the supply used for the input/output buffer on the relevant pin. MODE refers to the AVDD supply, all other digital input/output refers to the DVDD supply.

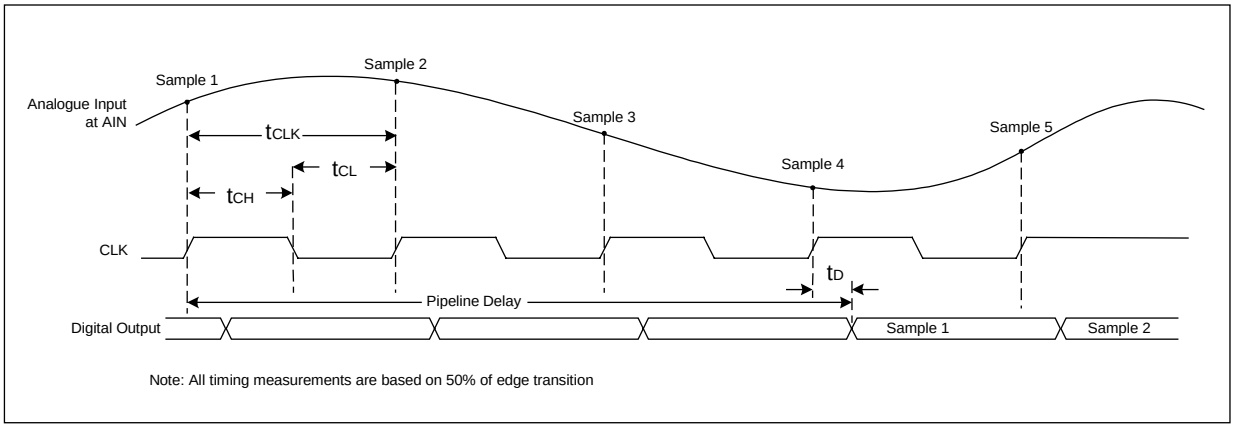


Figure 1 Output Timing

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock						
Clock period	t_{CLK}		33			ns
Clock high time	t_{CH}		15	16.5		ns
Clock low time	t_{CL}		15	16.5		ns
Timing						
Pipeline delay				3		CLK cycles
Clock to data valid	t_D				25	ns
Output disable to hi-Z output	t_{DZ}		0		20	ns
Output enable to data valid	t_{DEN}		0		20	ns

TYPICAL SYSTEM PERFORMANCE

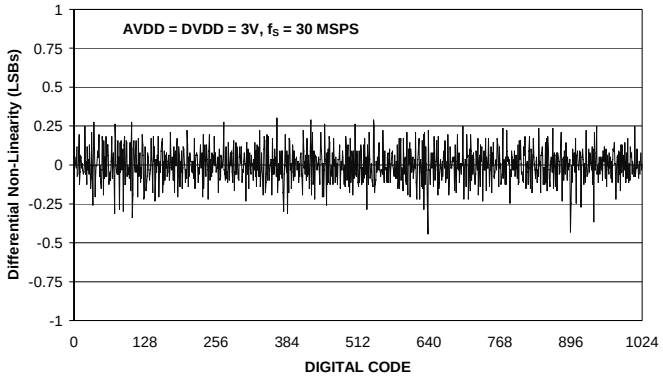


Figure 2 Differential Non-Linearity

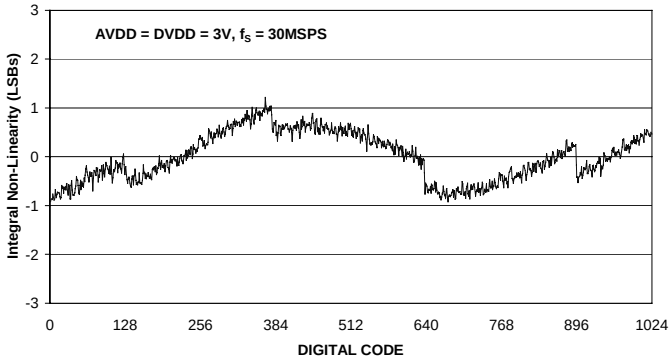


Figure 3 Integral Non-Linearity

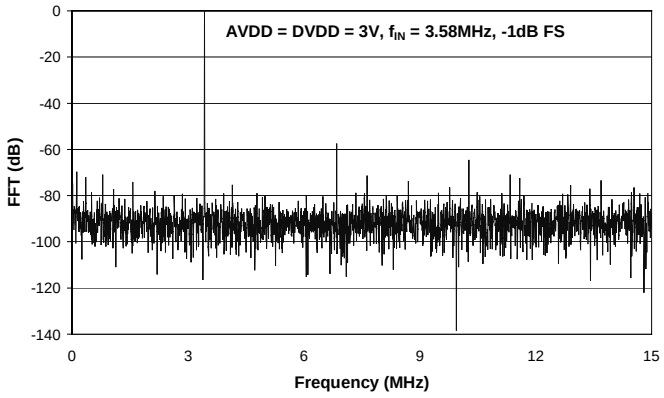


Figure 4 Fast Fourier Transform (FFT)

DEVICE DESCRIPTION

INTRODUCTION

The WM2130 is a high speed analogue-to-digital converter (ADC) with on-chip sample and hold and reference generation, designed for applications such as composite video digitisation, digital copiers and and high speed data acquisition. The chip architecture consists of:

- High bandwidth sample and hold input, which can operate in differential or single-ended mode
- 10-bit, 30MSPS pipeline analogue-to-digital converter (ADC) core
- On-chip reference generator and reference buffer (external references can also be used for applications where common or high precision references are required)
- 10-bit parallel interface to read ADC conversion data. An out-of-range output pin indicates when the input signal is outside the converter's range (this is disabled in AD876 compatible mode).

ANALOGUE SIGNAL PATH

The WM2130 analogue signal path consists of a DC clamp with a 10-bit clamp level DAC (discussed under 'DC Clamp', below), a high-bandwidth sample and hold unit and a fast 10-bit pipelined analogue to digital converter (ADC core).

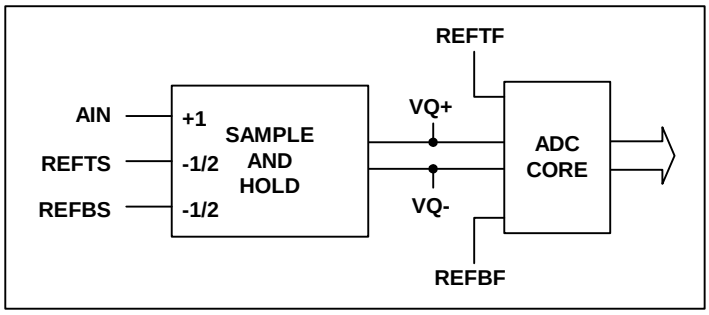


Figure 5 Analogue Input Signal Flow

Figure 5 shows the signal flow through the sample and hold unit to the ADC core, where the process of analogue to digital conversion is performed against the ADC reference voltages, REFTF and REFBF (their generation from internal or external reference sources is described later).

SAMPLE AND HOLD

The analogue input voltage V_{IN} is applied to the AIN pin, either DC coupled or AC coupled. The differential sample and hold processes V_{IN} with respect to the voltages applied to the REFTS and REFBS pins, and produces a differential output $V_Q = V_{Q+} - V_{Q-}$ given by:

$$V_Q = V_{IN} - V_M \qquad \text{where} \qquad V_M = \frac{REFTS + REFBS}{2}$$

For single-ended input signals, V_M is a constant voltage; usually the AIN mid-scale input voltage. However, in differential mode (see 'ADC Reference Modes', below), REFTS and REFBS can be connected together to operate with AIN as a complementary pair of differential inputs.

ANALOGUE-TO-DIGITAL CONVERTER

Regardless of the reference configuration, V_Q is digitised against ADC Reference Voltages REFTF and REFBF, full scale values of V_Q being given by:

$$V_{QFS+} = \frac{REFTF - REFBF}{2} \quad \text{and} \quad V_{QFS-} = -\left(\frac{REFTF - REFBF}{2}\right)$$

Attempts to convert V_Q voltages outside the range of V_{QFS-} to V_{QFS+} are signalled to the application by driving the OVR output pin high. If V_Q is less than V_{QFS-}, the ADC output code is 0. If V_Q is greater than V_{QFS+}, the output code is 1023.

SIGNAL CHAIN SUMMARY

Combining the above equations and referring back to the input, the positive and negative full-scale voltages at the AIN pin are:

$$V_{INFS+} = V_M + \frac{REFTF - REFBF}{2} \quad \text{and} \quad V_{INFS-} = V_M - \frac{REFTF - REFBF}{2}$$

Therefore the input signal span is given by:

$$V_{INFS+} - V_{INFS-} = REFTF - REFBF$$

In order to match the ADC input range to the input signal amplitude, REFTF and REFBF should be set such that:

$$REFTF - REFBF = (V_{INFS+} - V_{INFS-})$$

ADC REFERENCE MODES

The WM2130 supports three basic modes of reference generation, selected by the voltage applied to the MODE pin. These are summarised and explained in Table 1.

In differential, Centre Span and Top/Bottom modes, the internally generated ADC references are intened solely for WM2130 internal use and REFTF and REFBF must not be used as voltage references for any other device in the application.

MODE PIN	MODE	FUNCTION	COMMENTS
AGND	Full external	$REFTF = REFTS$ $REFBF = REFBS$	On-chip reference generator and reference buffer are not used.
AVDD/2	Differential	$REFTF = \frac{AVDD + V_{REF}}{2}$ $REFTF = \frac{AVDD - V_{REF}}{2}$	V_{REF} can be internally or externally generated. REFTS and REFBS are joined together and connected either to the negative end of the input signal (true differential mode) or to the AIN mid-scale voltage (centre-span mode).
AVDD	Top/Bottom	$REFTF = \frac{AVDD + (REFTS - REFBS)}{2}$ $REFBF = \frac{AVDD - (REFTS - REFBS)}{2}$	On-chip reference generator is not used. Reference buffer centers external reference voltages around AVDD/2.

Table 1 WM2130 Reference Generation Modes

FULL EXTERNAL REFERENCE MODE (MODE = AGND)

When MODE is connected to AGND, the WM2130 operates in full external reference mode. The internal reference buffer is powered down and bypassed, so that the ADC core takes the user-supplied reference voltages at pins REFTS and REFBS (REFTS and REFBS are internally connected to REFTF and REFBF). The mean of REFTF and REFBF must be equal to AVDD/2. Only single-ended input is possible in this mode.

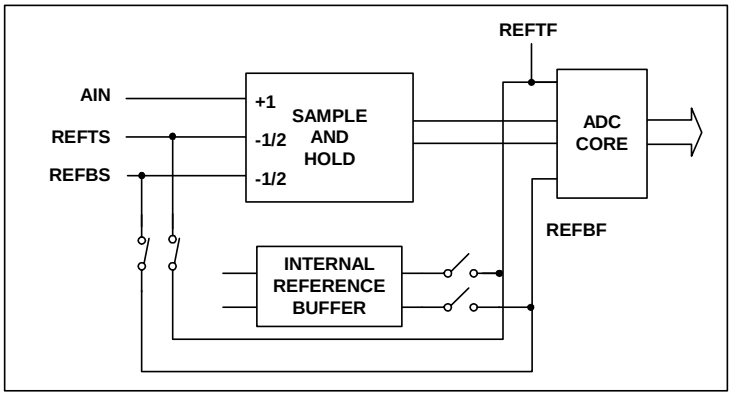


Figure 6 ADC Reference Generation in Full External Mode

The full external mode of operation is useful when the application requires more accurate or lower drift reference voltages than the WM2130 can provide, or when devices need to share common reference voltages for best ADC matching. It also offers the possibility of using REFTS and REFBS as sense lines to drive the REFTF and REFBF lines (**Kelvin mode**) to eliminate any voltage drops from remote references within the system (see Figure 7). In Kelvin configurations, take care when choosing the external op-amps to ensure that they can drive large capacitive loads without oscillating.

Although the on-chip reference generator is not used by the WM2130 in full external mode, its output is available on the VREF pin and can be used by other parts of the system. Note that in addition to the internal connections from REFTS to REFTF and REFBS to REFBF, external wire connections must also be made as shown in Figure 8 to minimise resistance (except in Kelvin mode).

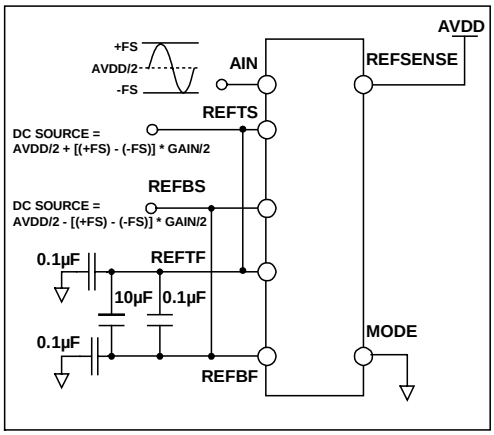


Figure 7 Full External Reference Mode (Reference Generator Disabled)

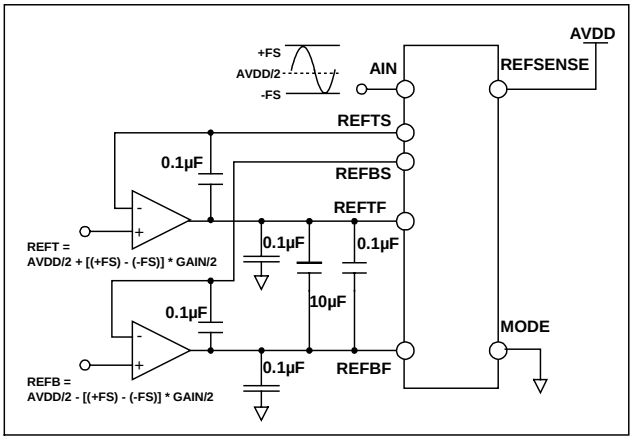


Figure 8 Full External Mode with Kelvin connections (Reference Generator Disabled)

DIFFERENTIAL MODE (MODE = AVDD/2)

The WM2130 operates in differential mode when the voltage at the MODE pin is AVDD/2 (mid-supply). The ADC reference voltages REFTF and REFBF are generated by the internal reference buffer from V_{REF}. Depending on the connection of the REFSENSE pin, V_{REF} may be supplied by the on-chip reference generator or driven by an external source, as discussed under 'On-chip Reference Voltage Generation', below. REFTF and REFBF are centred around AVDD/2 by the internal reference buffer and the voltage difference between them equals V_{REF}.

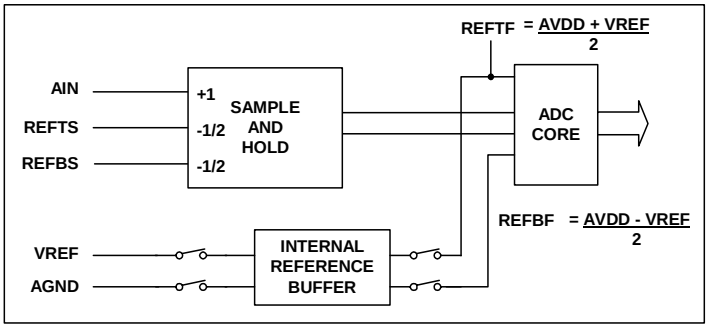


Figure 9 ADC Reference Generation in Differential Mode

This mode is suitable for handling differentially presented inputs, which are applied to the AIN and REFTS/REFBS pins. A special case of differential mode is **centre span mode**, in which the user applies a single-ended signal to AIN and applies the mid-scale input voltage (V_M) to the REFTS and REFBS pins.

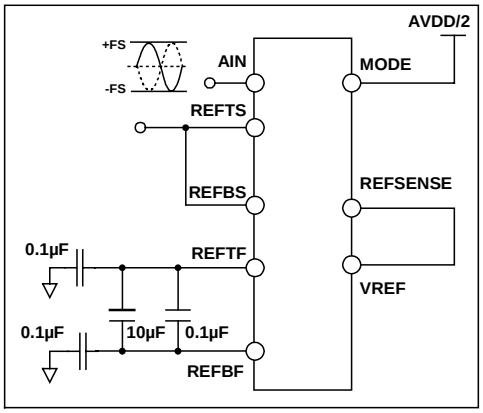


Figure 10 Differential Mode, 1V Reference Span

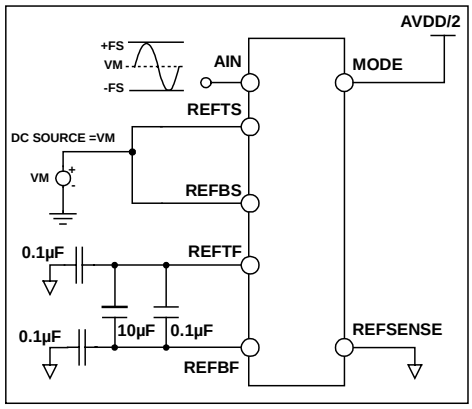


Figure 11 Centre Span Mode, 2V Reference Span

TOP/BOTTOM MODE (MODE = AVDD)

Top/Bottom mode is enabled by connecting the MODE pin to AVDD. In this mode, the ADC Reference voltages REFTF and REFBF are generated by the internal reference buffer from the externally supplied voltages REFTS and REFBS. Only single-ended input is possible in TOP/BOTTOM Mode.

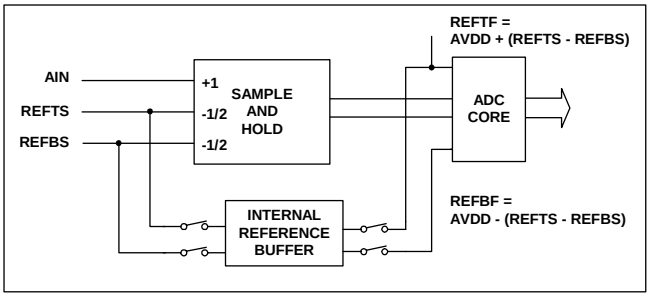


Figure 12 ADC Reference Generation in Top/Bottom Mode

The voltage difference between REFTS and REFBS should equal the peak-to-peak input signal amplitude. A smaller voltage difference would give rise to out-of-range conditions, whereas a larger one would not fully utilise the ADC resolution. The average of REFTS and REFBS must be the AIN mid-scale voltage, V_M.

Typically, REFSENSE is tied to AVDD to disable the on-chip reference generator, but the user can also choose to use its output to drive either REFTS or REFBS.

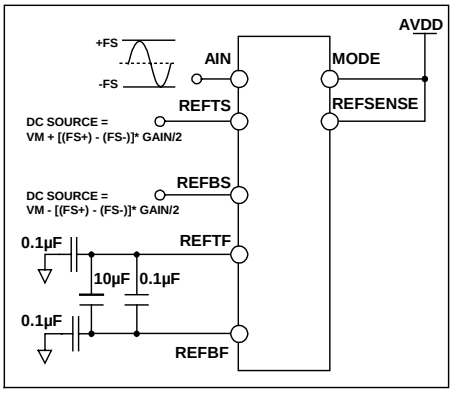


Figure 13 Top/Bottom Mode (Reference Generator Disabled)

ON-CHIP REFERENCE VOLTAGE GENERATOR

The On-chip Reference Generator (ORG) can provide a reference voltage on the VREF pin that is independent of temperature and supply voltage. External connections to the REFSENSE pin control the ORG's output to VREF, as shown in Figure 14.

REFSENSE CONNECTION	ORG OUTPUT TO VREF
VREF pin	1 Volt
AGND	2 Volts
External divider junction	(1 + R_A/R_B) Volts – see Figure 14
AVDD	None (VREF becomes input pin)

Table 2 Controlling the On-chip Reference Generator

Connecting REFSENSE to AVDD powers the ORG down, saving power when the ORG function is not required.

In differential mode (MODE = AVDD/2), the voltage on VREF determines the ADC reference voltages as follows:

$$REFTF = \frac{AVDD + V_{REF}}{2}$$

$$REFBF = \frac{AVDD - V_{REF}}{2}$$

$$REFTF - REFBF = V_{REF}$$

When the ORG is enabled, the VREF pin should be decoupled to the circuit board's analogue ground plane close to the WM2130 AGND pin via a 1µF tantalum capacitor and a 0.1µF ceramic capacitor. The ORG can source currents up to 1mA into external grounded loads when it is not used by the WM2130. Typical buffer load regulation is about 0.5Ω.

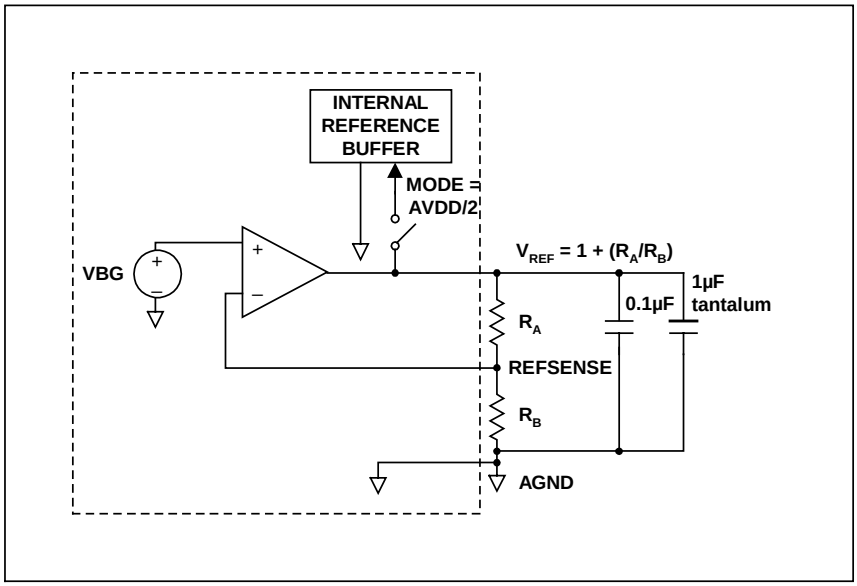


Figure 14 ORG Operating with External Divider (for Intermediate Reference Voltages)

POWER MANAGEMENT

In power-sensitive applications (such as battery-powered systems) where the WM2130 ADC is not required to convert continuously, power can be saved between conversion intervals by placing the WM2130 into Power Down mode. This is achieved by pulling the Standby Mode Pin (STBY, pin 16) HIGH. In Power Down mode, the device typically consumes less than 3mW of power. Power down mode is exited by resetting control register bit 3 to 0. On power up from long periods of power down, the WM2130 typically requires 5ms of wake up time before valid conversion results are available.

When REFSENSE is tied to AVDD, the reference generator is disabled and supply current reduced by approximately 1.2mA.

DIGITAL OUTPUT FORMAT

While the OEB pin is held low, ADC conversion results are output at the data output pins DO0 (LSB) to DO9 (MSB). The output data format is unsigned binary (output codes 0 to 1023).

AD876 COMPATIBILITY MODE

Pulling M876B (pin 20) low puts the WM2130 into AD876 compatibility mode. In this mode the device latency increases to 3.5 clock cycles and the OVR pin is tri-stated to avoid conflict with the DRGND connection present at pin 13 in AD876 slots.

For best dynamic performance, use a 3 cycle latency operating mode if possible.

APPLICATIONS INFORMATION

DRIVING THE CLOCK INPUT

Obtaining good performance from the WM2130 requires care when driving the clock input.

Different sections of the Sample-and-Hold and ADC operate while the clock is low or high. The user should ensure that the clock duty cycle remains near 50% to ensure that all internal circuits have as much time as possible in which to operate.

The CLK pin should also be driven from a low jitter source for best dynamic performance. To maintain low jitter at the CLK input, any clock buffers external to the WM2130 should have fast rising edges. Use a fast logic family such as AC or ACT to drive the CLK pin, and consider powering any clock buffers separately from any other logic on the PCB to prevent digital supply noise appearing on the buffered clock edges as jitter.

As the CLK input threshold is nominally around AVDD/2, any clock buffers need to have an appropriate supply voltage to drive above and below this level.

DRIVING THE SAMPLE AND HOLD INPUTS

DRIVING THE AIN PIN

Figure 15 shows an equivalent circuit for the WM2130 AIN pin. The load presented to the system at the AIN pin comprises the switched input sampling capacitor, C_{Sample}, and various stray capacitances, C_{P1} and C_{P2}.

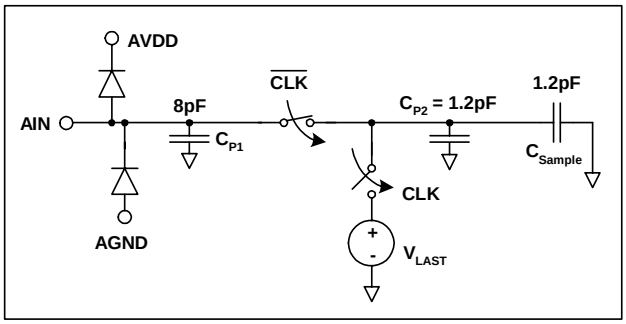


Figure 15 Equivalent Circuit for Analogue Input Pin AIN

The input current pulses required to charge C_{Sample} can be time averaged and the switched capacitor circuit modelled as an equivalent resistor

$$R_{IN2} = \frac{1}{C_S \times f_{CLK}}$$

where C_S is the sum of C_{Sample} and C_{P2} (see Figure 16). This model can be used to estimate the input loading versus source resistance for high impedance sources.

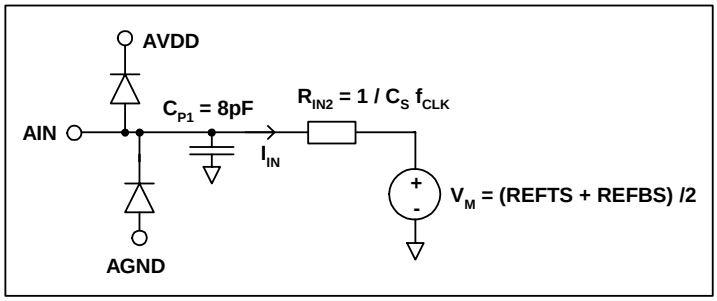


Figure 16 Equivalent Circuit for the AIN Switched Capacitor Input

AIN INPUT DAMPING

The charging current pulses into AIN can make the signal source jump or ring, especially if the source is slightly inductive at high frequencies. Inserting a small series resistor of 20Ω or less in the input path can damp source ringing (see Figure 17). The resistor can be made larger than 20Ω if reduced input bandwidth or distortion performance is acceptable.

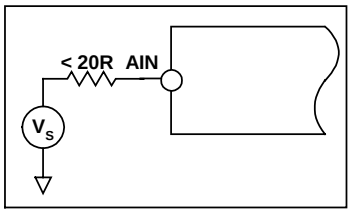


Figure 17 Damping Source Ringing Using a Small Resistor

DRIVING THE SAMPLE & HOLD REFERENCE INPUTS

The sample and hold reference inputs (connected to pins REFTS and REFBS) present switched-capacitor loads similar to the AIN pin, but with smaller capacitors (see Figure 18 below). Note that in Top/Bottom mode, the internal reference buffer is also driven from REFTS and REFBS and the total load on these pins is therefore the parallel combination of the sample and hold circuit and the reference buffer.

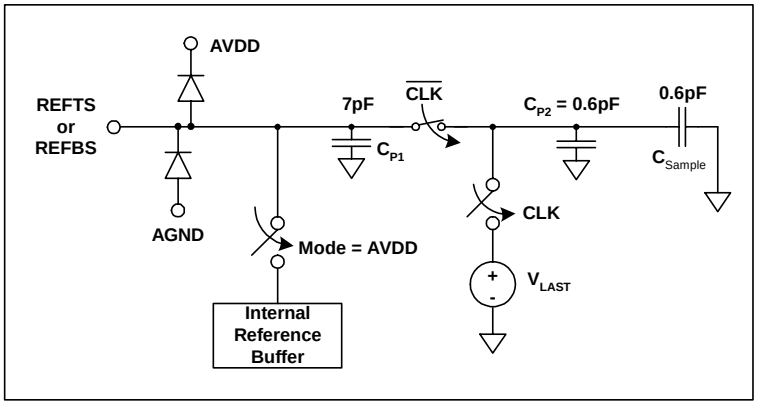


Figure 18 Equivalent Circuit of REFTS and REFBS Sample & Hold Inputs

DRIVING THE INTERNAL REFERENCE BUFFER

DRIVING THE VREF PIN (DIFFERENTIAL MODE)

Figure 19 shows the equivalent load on the VREF pin when driving the internal reference buffer via this pin (MODE = AVDD/2 and REFSENSE = AVDD).

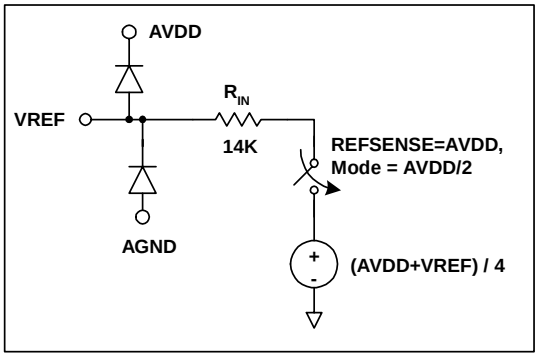


Figure 19 Equivalent Circuit of VREF

The input current I_{REF} is given by

$$I_{REF} = \frac{3V_{REF} - AVDD}{4 \times R_{IN}}$$

Tolerance on this current is $\pm$ 30 % or greater. The user should ensure that VREF is driven from a low noise, low drift source, well-decoupled to analogue ground and capable of driving I_{REF}.

DRIVING THE INTERNAL REFERENCE BUFFER (TOP/BOTTOM MODE)

Figure 20 shows the loading on the REFTS and REFBS pins in Top/Bottom mode due to the internal reference buffer. Note that the sample and hold circuit must also be driven via these pins, which adds additional load (see Driving the Sample & Hold Reference Inputs, above).

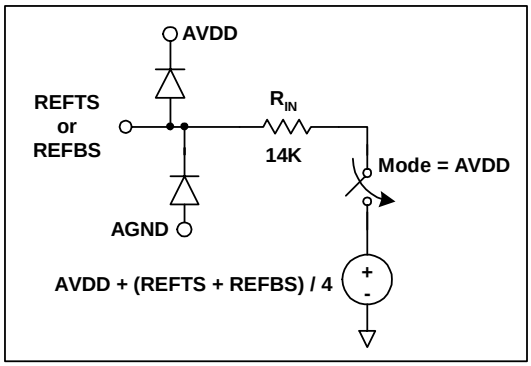


Figure 20 Equivalent Circuit of Inputs to Internal Reference Buffer

The input currents are given by:

$$I_{INTS} = \frac{3REFTS - AVDD - REFBS}{4 \times R_{IN}}$$

and $$I_{INBS} = \frac{3REFBS - AVDD - REFTS}{4 \times R_{IN}}$$

These currents must be provided by the sources on REFTS and REFBS in addition to the requirements of driving the sample and hold.

DRIVING REFTF AND REFBF (FULL EXTERNAL REFERENCE MODE)

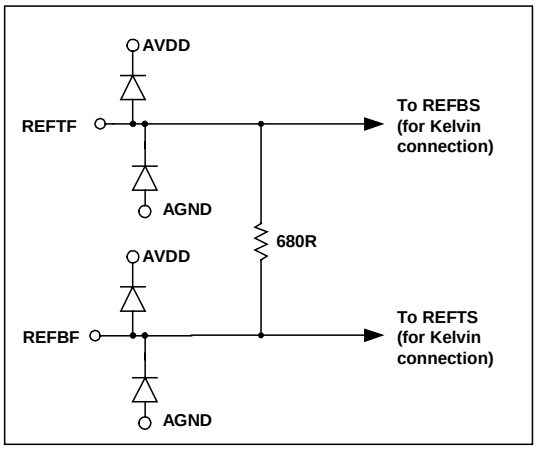


Figure 21 Equivalent Circuit of REFTF and REFBF Inputs

REFERENCE DECOUPLING

VREF PIN

When the on-chip reference generator is enabled, the VREF pin should be decoupled to the circuit board's analogue ground plane close to the WM2130 AGND pin via a 1µF tantalum capacitor and a 0.1µF ceramic capacitor.

REFTF AND REFBF PINS

In any mode of operation, the REFTF and REFBF pins should be decoupled as shown in Figure 22 below. Use short board traces between the WM2130 and the capacitors to minimise parasitic inductance.

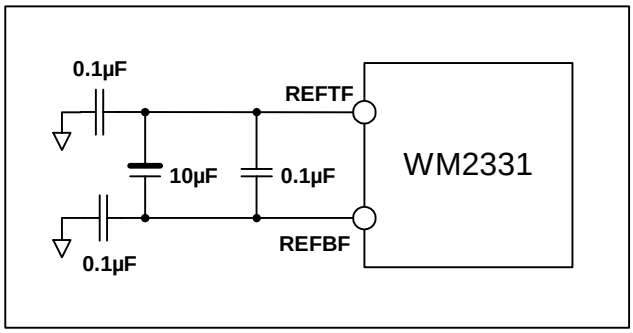


Figure 22 Recommended Decoupling for the ADC Reference Pins REFTF and REFBF

SUPPLY DECOUPLING

The analogue (AVDD, AGND) and digital (DVDD, DGND) power supplies to the WM2130 should be separately decoupled for best performance. Each supply needs at least a 10µF electrolytic or tantalum capacitor (as a charge reservoir) and a 100nF ceramic type capacitor placed as close as possible to the respective pins (to suppress spikes and supply noise).

DIGITAL OUTPUT LOADING AND CIRCUIT BOARD LAYOUT

The WM2130 outputs are capable of driving rail-to-rail with up to 20pF of load per pin at 30MHz clock and 3V digital supply. Minimising the load on the outputs will improve WM2130 signal-to-noise performance by reducing the switching noise coupling from the WM2130 output buffers to the internal analogue circuits. The output load capacitance can be minimised by buffering the WM2130 digital outputs with a low input capacitance buffer placed as close to the output pins as physically possible, and by using the shortest possible tracks between the WM2130 and this buffer.

Noise levels at the output buffers, which may affect the analogue circuits within WM2130, increase with the digital supply voltage. Where possible, consider using the lowest DVDD that the application can tolerate.

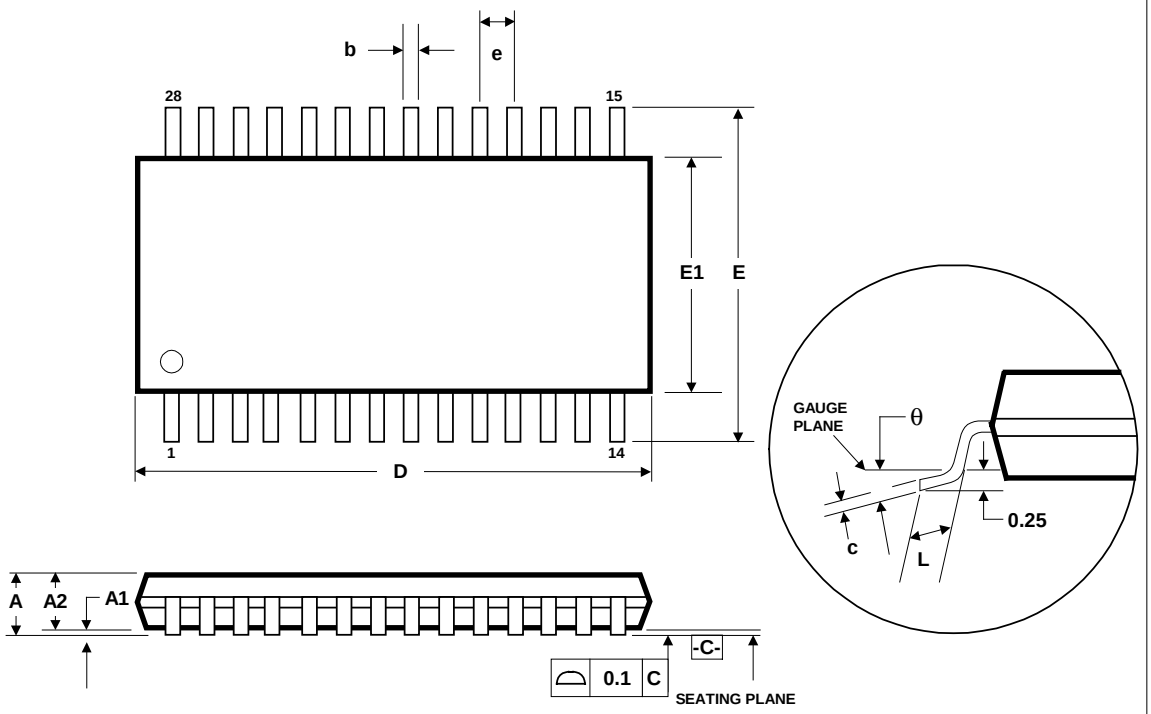
Use good layout practices when designing the application PCB to ensure that any off-chip return currents from the WM2130 digital outputs (and any other digital circuits on the PCB) do not return via the supplies to any sensitive analogue circuits. The WM2130 should be soldered directly to the PCB for best performance. Socketing the device will degrade performance by adding parasitic socket inductance and capacitance to all pins.

USER TIPS FOR OBTAINING BEST PERFORMANCE FROM THE WM2130

- Choose differential input mode for best distortion performance.
- Choose a 2V ADC input span for best noise performance.
- Choose a 1V ADC input span for best distortion performance.
- Drive the clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.

PACKAGE DIMENSIONS

DT: 28 PIN TSSOP (9.7 x 4.4 x 1.0 mm) **DM022.A**



Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	9.60	9.70	9.80
e		0.65 BSC	
E		6.4 BSC	
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.