W81282F

USB Keyboard Controller with 4 Ports Hub

W81282F Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.	08/27/99	0.50	n.a.	First published.
2					
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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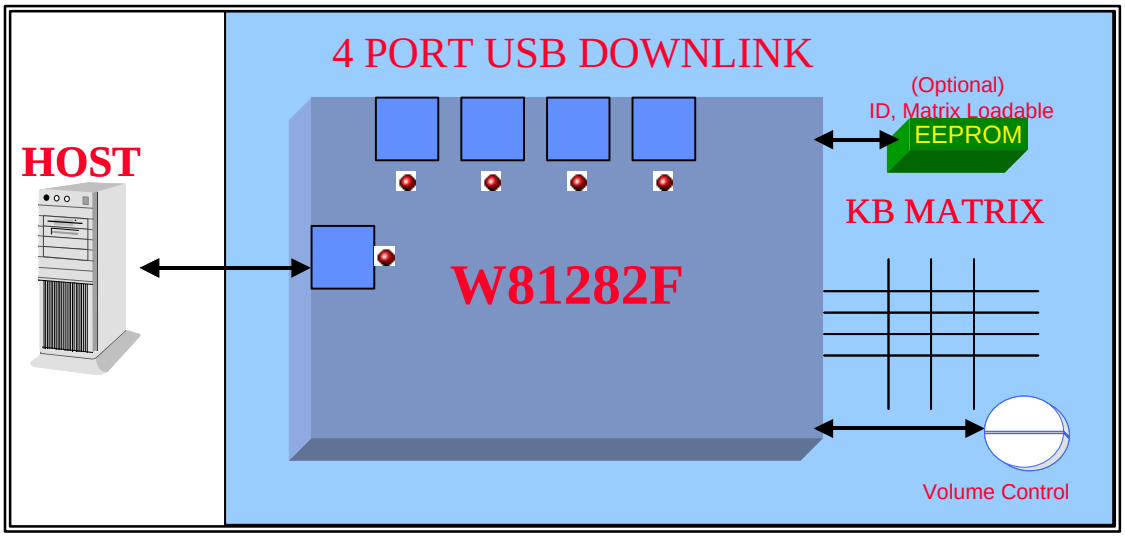
Winbond Electronics Corp.

USB HUB CONTROLLER

1. GENERAL DESCRIPTION

The W81282F is a highly integrated USB keyboard with 4 port hub controller chip. The W81282F has a built-in 21X8 default keyboard matrix, so that it can be directly connected to keyboard with multi-media function matrix. The keyboard matrix, vendor ID, and device ID can be easily customized from an optional EEPROM or modify firmware to meet any customers' requirement. The 4 USB down-stream port can be used to connect various USB peripheral devices, such as printer, modem, speaker, camera, mice, and joystick, to system without any external glue logics. The W81282F use 12MHz clock input with internal PLL to eliminate EMI effect. The W81282F also built-in ESD/EFT protection circuit so it can pass ESD/EFT test without any external glue logics.

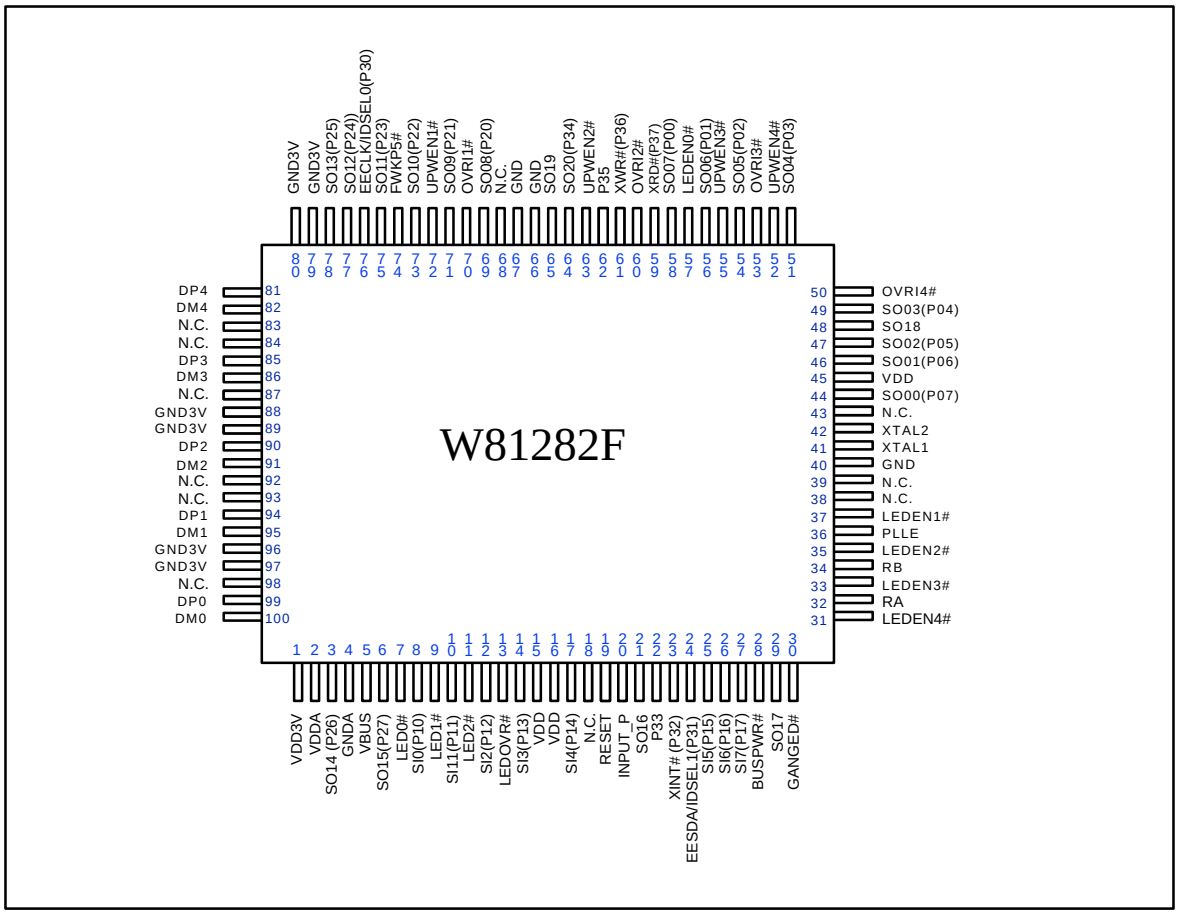
2. APPLICATION BLOCK DIAGRAM



3. FEATURES

- Full compliance with USB spec Rev 1.1 and HID Class Definition Rev 1.0
- Embedded microprocessor--8052 (6K ROM + 256 Byte RAM)
- Support auto-detected two power source mode between bus power mode and self power mode.
- 12-Mhz crystal/oscillator input to lower EMI
- Support Suspend and Resume operation
- Support ACPI features
- Four downstream ports with per port over-current protection
- Single 5V supplied with embedded 5V-3.3V regulator
- Provides the external pull-up resistor control for the up-stream connection.
- Per-port/Global power control optional
- Built-in ESD/EFT protection circuit
- Support 21 X 8 keyboard matrix
- Support consumer control function for multi-media
- Support optional EEPROM for vendor ID, device ID, and KB matrix down load
- Support encoder input for audio volume control
- Provide the external pull-up resistor control for the up-stream connect
- 100-pin PQFP
- 5V CMOS device

4. PIN CONFIGURATION



5. PIN DESCRIPTION

Pin Number	Pin Name	I/O Type	Pin Function	Pull Up/ Down
1	**VDD3V**	Power1	3.3V Regulator Output. Supplying voltage for all transceivers	-
2	**VDDA**	Power1	Analog power.	-
3	**SO14 (P26)**	IOUD2	Port 2.6 and function of Scan Out line 14.	U
4	**GNDA**	Power0	Analog ground.	-
5	**VBUS**	IUD2T	Input of upstream power status. On self-power mode, connection should be controlled by VBUS status.	-
6	**SO15 (P27)**	IOUD2	Port 2.7 and function of Scan Out line 15.	U
7	**LED0#**	IOU2P	Keyboard NumLock LED driver. To drive LED directly.	O
8	**SI0 (P10)**	IOUD2	Port 1.0 and function of Scan In line 0.	U
9	**LED1#**	IOU2P	Keyboard CapLock LED driver. To drive LED directly.	O
10	**SI1 (P11)**	IOUD2	Port 1.1 and function of Scan In line 1.	U
11	**LED2#**	IOU2P	Keboard ScrolLock LED driver. To drive LED directly	O
12	**SI2 (P12)**	IOUD2	Port 1.2 and function of Scan In line 2.	U
13	**LEDOVR#**	IOU2P	Flag of any downstream port1 over-current. To drive LED directly	O
14	**SI3 (P13)**	IOUD2	Port 1.3 and function of Scan In line 3.	U
15,16	**VDD**	Power1	Digital supply voltage.	-
17	**SI4 (P14)**	IOUD2	Port 1.4 and function of Scan In line 4.	U
18	**N.C.**	IOUD2	No connection. This pin should be floated.	U
19	**RESET**	IUD2T	Master reset input. Active high.	-
20	**INPUT_P**	IOUD2	A programmable port and reverse for input application.	U
21	**SO16**	O2	This pin is function of Scan Out line 16.	-
22	**P33**	IOUD2	Port 3.3 and reverse for input or output application.	U
23	**XINT# (P32)**	IOUD2	Port 3.2. This pin is dedicated for internal use.	U
24	**EESDA/IDSEL1 (P31)**	IOUD2	Port 3.1 and function of serial data line interfacing with external EEPROM. If no serial EEPROM present, this pin is used to scan ID selection and named IDSEL1	U
25	**SI5 (P15)**	IOUD2	Port 1.5 and function of Scan In line 5.	U
26	**SI6 (P16)**	IOUD2	Port 1.6 and function of Scan In line 6.	U
27	**SI7 (P17)**	IOUD2	Port 1.7 and function of Scan In line 7.	U

28	**BUSPWR#**	IUD2	Buspower/Selfpower control setting. This pin should be floated or tied to VDD.	D
29	**SO17**	IOU2P	This pin is function of Scan Out line 17.	O
30	**GANGED#**	IUD2	Ganged/Individual downstream power switch control setting. Default is Individual mode.	U
31	**LEDEN4#**	IOU2P	Downstream port4 LED. Active low when port4 enable.	O
32	**RA**	IUD2	**This pin is a Rotation A input for consumer HID application.**	U
33	**LEDEN3#**	IOU2P	Downstream port3 LED. Active low when port3 enable.	O
34	**RB**	IUD2	**This pin is a Rotation B input for consumer HID application.**	U
35	**LEDEN2#**	IOU2P	Downstream port2 LED. Active low when port2 enable.	O
36	**PLLE**	IUD2	PLL clock generator enable/disable control. It should be tied to VDD. (PLLE=1, clock=12MHz ; PLLE=0,clock=48MHz)	U
37	**LEDEN1#**	IOU2P	Downstream port1 LED. Active low when port1 enable.	O
38	**N.C.**	IUD2	No connection. This pin should be floated.	U
39	**N.C.**	IUD2	No connection. This pin should be floated.	U
40	**GND**	Power0	Digital ground	-
41	**XTAL1**	OSCM	Clock In. (12MHz when PLLE=1, 48MHz when PLLE=0)	-
42	**XTAL2**	OSCM	Clock Out.	-
43	**N.C.**	IUD2	No connection. This pin should be floated.	D
44	**SO00 (P07)**	IOUD2	Port 0.7 and function of Scan Out line 0.	U
45	**VDD**	Power1	Digital supply voltage.	-
46	**SO01 (P06)**	IOUD2	Port 0.6 and function of Scan Out line 1.	U
47	**SO02 (P05)**	IOUD2	Port 0.5 and function of Scan Out line 2.	U
48	**SO18**	O2	This pin is function of Scan Out line 18.	-
49	**SO03 (P04)**	IOUD2	Port 0.4 and function of Scan Out line 3.	U
50	**OVRI4#**	IUD2T	Downstream port4 over-current status input. Active low.	-
51	**SO04 (P03)**	IOUD2	Port 0.3 and function of Scan Out line 4.	U
52	**UPWEN4#**	O2	Downstream port4 power control. Active low.	-
53	**OVRI3#**	IUD2T	Downstream port3 over-current status input. Active low.	-
54	**SO05 (P02)**	IOUD2	Port 0.2 and function of Scan Out line 5.	U
55	**UPWEN3#**	O2	Downstream port3 power control. Active low.	-
56	**SO06 (P01)**	IOUD2	Port 0.1 and function of Scan Out line 6.	U
57	**LEDEN0#**	IOU2P	Up_stream port LED. Active low when up_stream port enable.	O
58	**SO07 (P00)**	IOUD2	Port 0.0 and function of Scan Out line 7.	U

59	**XRD# (P37)**	IOUD2	Port 3.7.This pin is dedicated for internal use.	U
60	**OVRI2#**	IUD2T	Downstream port2 over-current status input. Active low.	-
61	**XWR# (P36)**	IOUD2	Port 3.6.This pin is dedicated for internal use.	U
62	**P35**	IOUD2	Port 3.5 and reverse for input or output application.	U
63	**UPWEN2#**	O2	Downstream port2 power control. Active low.	-
64	**SO20 (P34)**	IOUD2	Port 3.4 and function of Scan Out line 20.	U
65	**SO19**	O2	This pin is function of Scan Out line 19.	-
66,67	**GND**	Power0	Digital ground.	-
68	**N.C.**	IOUD2	No connection. This pin should be floated.	U
69	**SO08 (P20)**	IOUD2	Port 2.0 and function of Scan Out line 8.	U
70	**OVRI1#**	IUD2T	Downstream port1 over-current status input. Active low.	-
71	**SO09 (P21)**	IOUD2	Port 2.1 and function of Scan Out line 9.	U
72	**UPWEN1#**	O2	Downstream port1 power control. Active low.	-
73	**SO10 (P22)**	IOUD2	Port 2.2 and function of Scan Out line 10.	U
74	**FWKP5#**	IUD2	Embedded function wake-up input. Can be used for Wake-up hot key.	D
75	**SO11 (P23)**	IOUD2	Port 2.3 and function of Scan Out line 11.	U
76	**EECLK/IDSEL0 (P30)**	IOUD2	**This pin is Port 3.0 and function of serial clock line interfacing with external EEPROM. If no serial EEPROM present, this pin is used to scan ID selection and named IDSEL0.**	U
77	**SO12 (P24)**	IOUD2	Port 2.4 and function of Scan Out line 12.	U
78	**SO13 (P25)**	IOUD2	Port 2.5 and function of Scan Out line 13.	U
79,80	**GND3V**	Power0	Ground of port3 and port4 transceivers.	-
81	**DP4**	AIO	USB D+ for downstream port4.	-
82	**DM4**	AIO	USB D- for downstream port4.	-
83,84	**N.C.**	-	No connection.	
85	**DP3**	AIO	USB D+ for downstream port3.	-
86	**DM3**	AIO	USB D- for downstream port3.	-
87	**N.C.**	-	No connection.	
88,89	**GND3V**	Power0	Ground of port1 and port2 transceivers.	-
90	**DP2**	AIO	USB D+ for downstream port2.	-
91	**DM2**	AIO	USB D- for downstream port2.	-

92,93	**N.C.**	-	No connection.	
94	**DP1**	AIO	USB D+ for downstream port1.	-
95	**DM1**	AIO	USB D- for downstream port1.	-
96,97	**GND3V**	Power0	Ground of port0 transceivers.	-
98	**N.C.**	-	No connection.	
99	**DP0**	AIO	USB D+ for upstream port0.	-
100	**DM0**	AIO	USB D- for upstream port0.	-

6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMIT
Supply Voltage (Vcc to Vss)	5.5V
Analog Input Voltage	Vss-0.5V to Vcc+0.5V
Digital Input Voltage	Vss-0.5V to Vcc+0.5V
Power Dissipation	TBD
Ambient Operating Temperature	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	250°C

7. ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 5V +/-5%, Ta=0° to 70°C

PARAMETER	Symbol	Conditions	Min	Max	Unit
VCC Supply Current	Icc			TBD	mA
Logic Output High	VOH	Io≥24ma	2.5	VCC	V
Logic Output Low	VOL	Io≥6ma		0.4	V
Logic Input Leakage Current		Ta=70°C		10	uA
USB CHARACTERISTICS		Note 8			
Leakage Current:					
Hi-Z State Output Leakage	ILO	V< V IN <3.3 V	-10	+10	uA
Input Levels:					
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2		V
Single Ended Signal “0”	VSE0		0.8	2.0	V
Differential Common Mode Range	V_{CM}	Includes VDI range	0.8	2.5	
Output Levels:					
Driver Output Low	VOLU	RL of 1.5 kΩ to 3.6 V		0.3	V
Driver Output High	VOHU	RL of 15 kΩ to GND	2.8	3.6	V
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Full Speed Timings:					
Output Rise/Fall Times	t R /t F	Note 1, 4 (C_L= 50 pF)	4	20	ns
Source Differential Driver Jitter to Next Transition / to Paired Transition	t DJ1 /tDJ2	Note 2, 3	-3.5 /-4	3.5 /4	ns ns
Differential to EOP transition Skew	t_{DEOP}	Note 3	-2	5	ns
Hub Differential Data Delay(without cable)	t HDD2	Note 2,3,5		44	ns
Hub Differential Driver Jitter to Next Transition / to Paired Transition (including cable)	t HDJ1 / t HDJ2	Note 2,3,5	-3 / -1	3 /1	ns
Data bit width distortion after SOP	t SOP	Note 3,5	-5	5	ns
Hub SE0 Delay Relative to t_{HDD}	t EOPD	Note 3,5	0	15	ns
Hub EOP Output Width Skew	t HESK	Note 3,5	-15	15	ns
Low Speed Timings:					
Output Rise/Fall Times	t R /t F	Note 1, 4 (C_L= 50 pF)	75	300	ns

7. ELECTRICAL CHARACTERISTICS, continued

PARAMETER	Symbol	Conditions	Min	Max	Unit
Source Differential Driver Jitter to Next Transition / to Paired Transition	t DJ1 /tDJ2	Note 2, 3	-25 /-14	25 /14	ns ns
Differential to EOP transition Skew	t_{DEOP}	Note 3	-40	100	ns
Hub Differential Data Delay(without cable)	t HDD2	Note 2,3,5		300	ns
Hub Differential Driver Jitter to Next Transition / to Paired Transition (including cable)	t HDJ1 / t HDJ2	Note 2,3,5	-45 / -45	45 /-45	ns
Data bit width distortion after SOP	t SOP	Note 3,5	-60	60	ns
Hub SE0 Delay Relative to t_{HDD}	t EOPD	Note 3,5	0	200	ns
Hub EOP Output Width Skew	t HESK	Note 3,5	-300	300	ns

Note 1: Measured from 10% to 90% of the data signal.

Note 2: Timing difference between the differential signals.

Note 3: Measured at crossover point of differential data signals.

Note 4: The rising and falling edges should be smoothly transiting(monotonic)

Note 5: Full Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D+ (DP) data line.

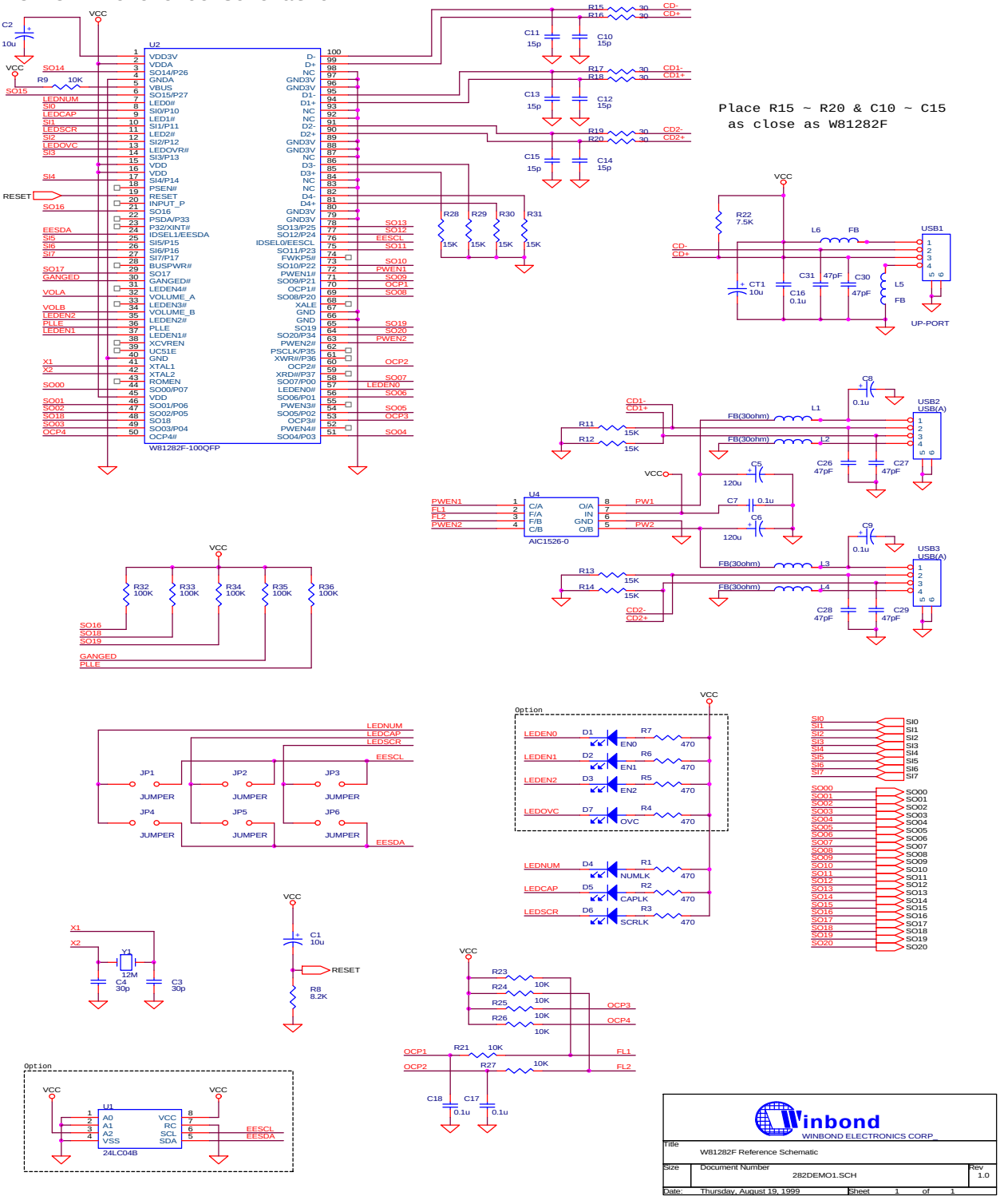
Note 6: Low Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D- (DM) data line.

Note 7: The maximum load specification is the maximum effective capacitive load allowed that meets the target hub VBUS droop of 330 mV.

Note 8: All other USB Electrical Characteristics refer to USB spec Rev 1.1 7.3.2 and 7.3.3.

8. TYPICAL APPLICATION

W81282F Reference Schematic



9. HOW TO READ THE TOP MARKING

Example: The top marking of W81282F-05

1st line: Winbond logo

2nd line: the type number: W81282F-05

3rd line: the tracking code: 732 A C 2 7242968

732: packages made in '97, week 19

A: assembly house ID; A means ASE, S means SPIL ... etc

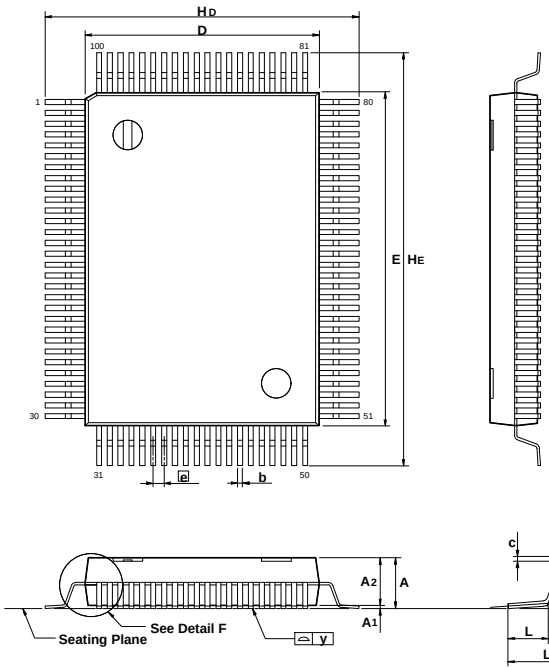
C: IC revision; B means version B, C means version C

2: wafers manufactured in Winbond FAB 2

7242968: wafer production series lot number

10. PACKAGE DIMENSIONS

(100-pin QFP)



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.010	0.012	0.016	0.25	0.30	0.40
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.50	0.65	0.80
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
q	0°	—	12°	0°	—	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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