Winbond Electronics Corp.

64K ´ 16 CMOS 3.3V FLASH MEMORY

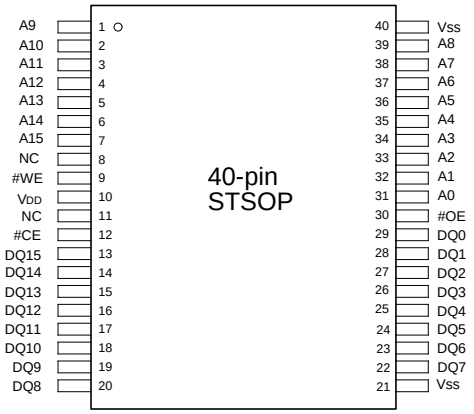
GENERAL DESCRIPTION

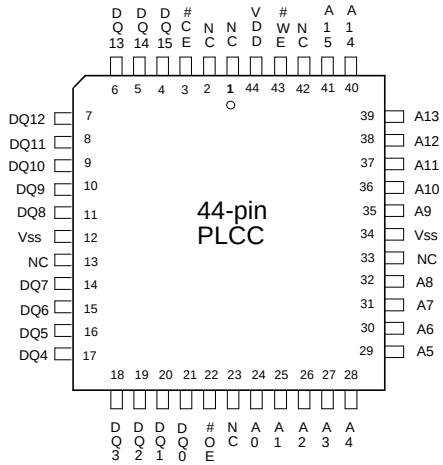
The W49L102 is a 1-megabit, 3.3-volt only CMOS flash memory organized as 64K × 16 bits. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is not required. The unique cell architecture of the W49L102 results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

FEATURES

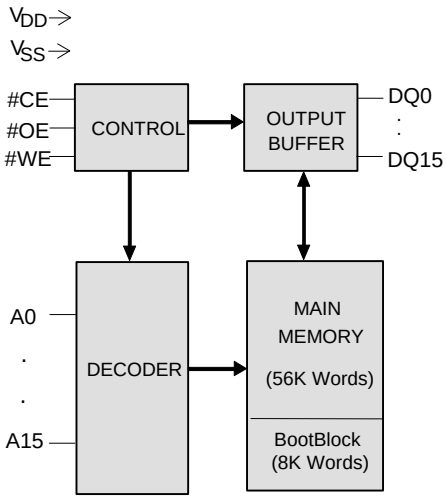
- Single 3.3-volt Operations:
  - 3.3-volt Read
  - 3.3-volt Erase
  - 3.3-volt Program
- Fast Program Operation:
  - Word-by-Word Programming: 60 µS (max.)
- Fast Erase Operation: 100 mS (typ.)
- Fast Read Access Time: 70/90/120 nS
- Endurance: 10K cycles (typ.)
- Twenty-year Data Retention
- Hardware Data Protection
- 8K word Boot Block with Lockout Protection
- Low Power Consumption
  - Active Current: 15 mA (typ.)
  - Standby Current: 10 µA (typ.)
- Automatic Program and Erase Timing with Internal VPP Generation
- End of Program or Erase Detection
  - Toggle Bit
  - Data Polling
- Latched Address and Data
- TTL Compatible I/O
- JEDEC Standard Word-wide Pinouts
- Available Packages: 40-pin STSOP (10 x 14 mm) and 44-pin PLCC

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0 – A15	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
VSS	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49L102 is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words of the memory with the address range from 0000 hex to 1FFF hex.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block can not be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function will only affect the main memory.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data is "FF hex," the boot block programming lockout feature is activated; if the output data is "FE hex," the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Input Levels

While operating with a 3.0V – 3.6V power supply, the address inputs and control inputs (#OE, #CE and #WE) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6V.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the main memory will be erased to FF(hex), and the data in the boot block will not be erased (remains same as before the chip erase operation). The entire memory array (main memory and boot block) will be erased to FF hex. by the chip erase operation if the boot block programming lockout feature is not activated. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Main Memory Erase Operation

The main memory erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal main-memory erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Program Operation

The W49L102 is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0" The erase operation (changed entire data in main memory and/or boot block from "0" to "1" is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will internally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (60 μS max. - T_{BP}) once completed and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49L102 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming and read operation are inhibited when V_{DD} is less than 1.8V typical.

(3) Write Inhibit Mode: Forcing #OE low, #CE high, or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 10 mS before any write (erase/program) operation.

Data Polling (DQ_7 & DQ_{15})- Write Status Detection

The W49L102 includes a data polling feature to indicate the end of a program or erase cycle. When the W49L102 is in the internal program or erase cycle, any attempt to read DQ_7 or DQ_{15} of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 or DQ_{15} will show the true data. Note that DQ_7 or DQ_{15} will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has completed.

Toggle Bit (DQ_6 & DQ_{14})- Write Status Detection

In addition to data polling, the W49L102 provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ_6 or DQ_{14} will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (00DAh). A read from address 0001H outputs the device code (002Fh). The product ID operation can be terminated by a three-word command sequence or an alternate one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing #CE and #OE low, #WE high, and raising A9 to 12 volts.

Note: The hardware SID read function is not included in all parts; please refer to Ordering Information for details.

TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V ±0.5V)

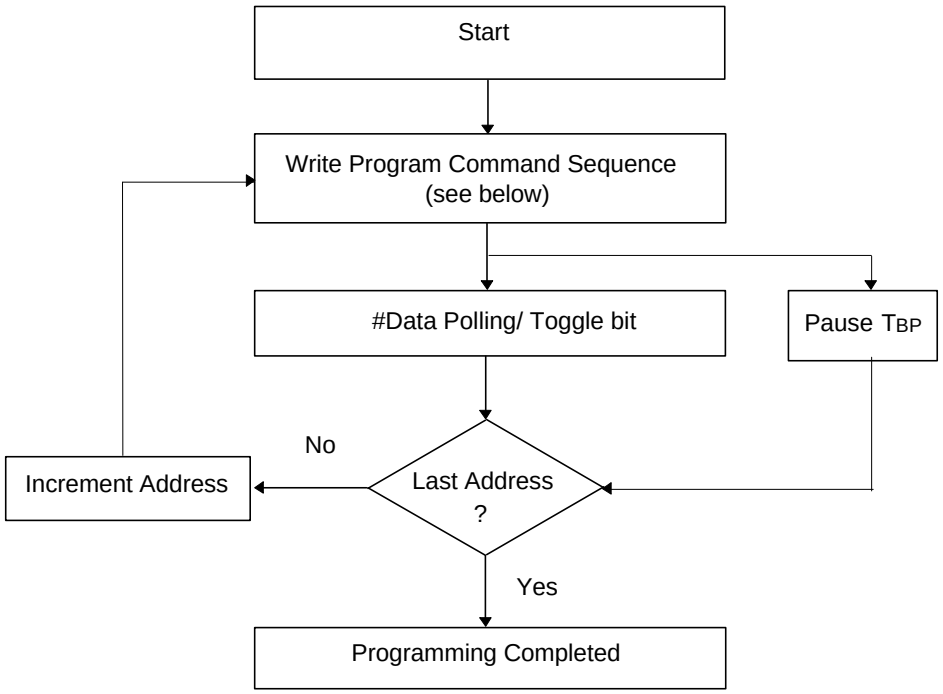
MODE	PINS				
	#CE	#OE	#WE	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1 – A15 = V_{IL}; A9 = V_{HH}	Manufacturer Code 00DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}; A1 – A15 = V_{IL}; A9 = V_{HH}	Device Code 002F (Hex)

TABLE OF COMMAND DEFINITION

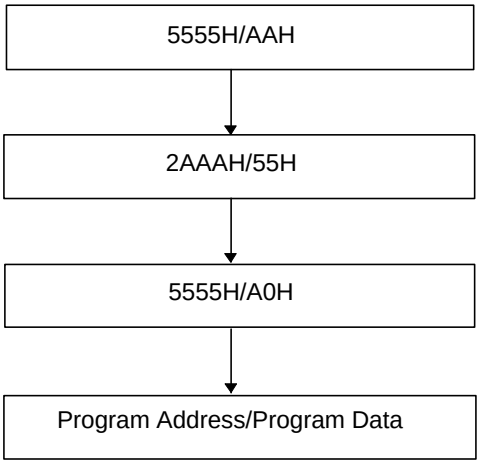
COMMAND DESCRIPTION	No. of Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read	1	A_{IN}	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Main Memory Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	30
Word Program	4	5555	AA	2AAA	55	5555	A0	A_{IN}	D_{IN}				
Boot Block Lockout	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit [1]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit [1]	1	XXXX	F0										

Note: Address Format: A14 – A0 (Hex); Data Format: DQ15 – DQ8 (Don't Care); DQ7 – DQ0 (Hex)
Either one of the two Product ID Exit commands can be used.

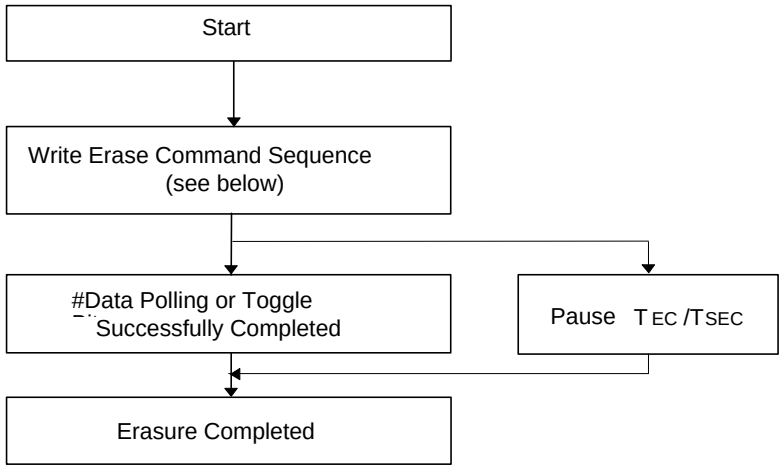
Embedded Programming Algorithm



Program Command Sequence (Address/Command):

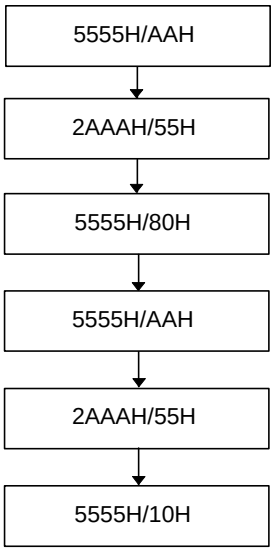


Embedded Erase Algorithm



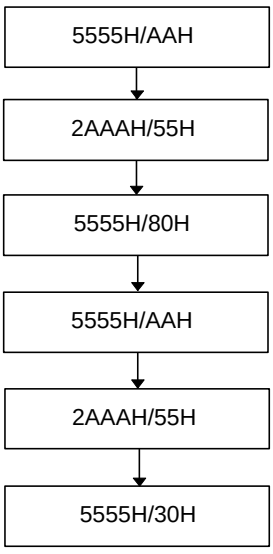
Chip Erase Command Sequence

(Address/Command):

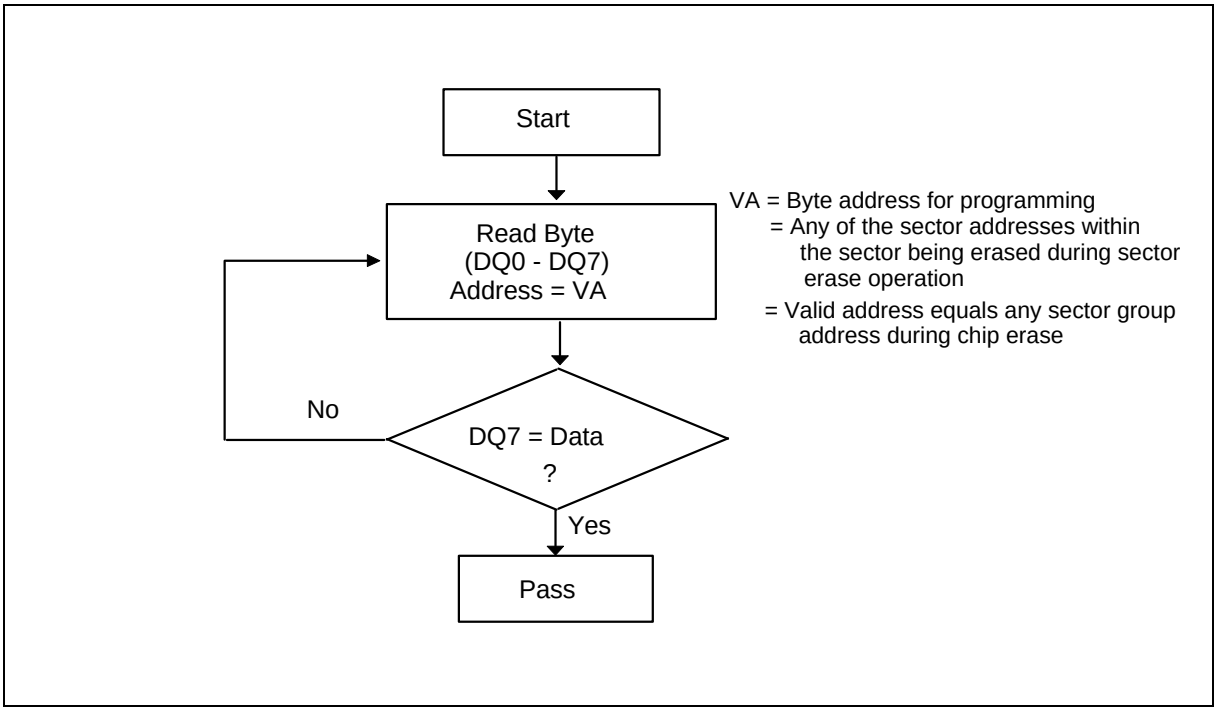


Main Memory Erase Command Sequence

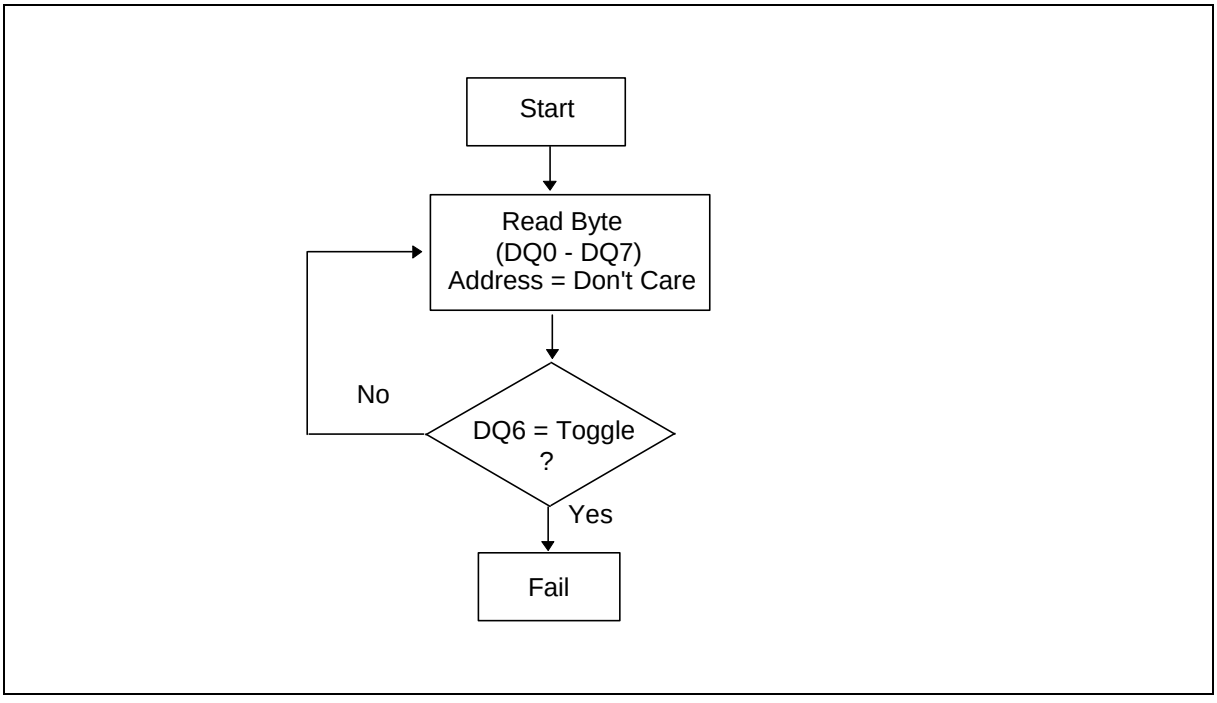
(Address/Command):



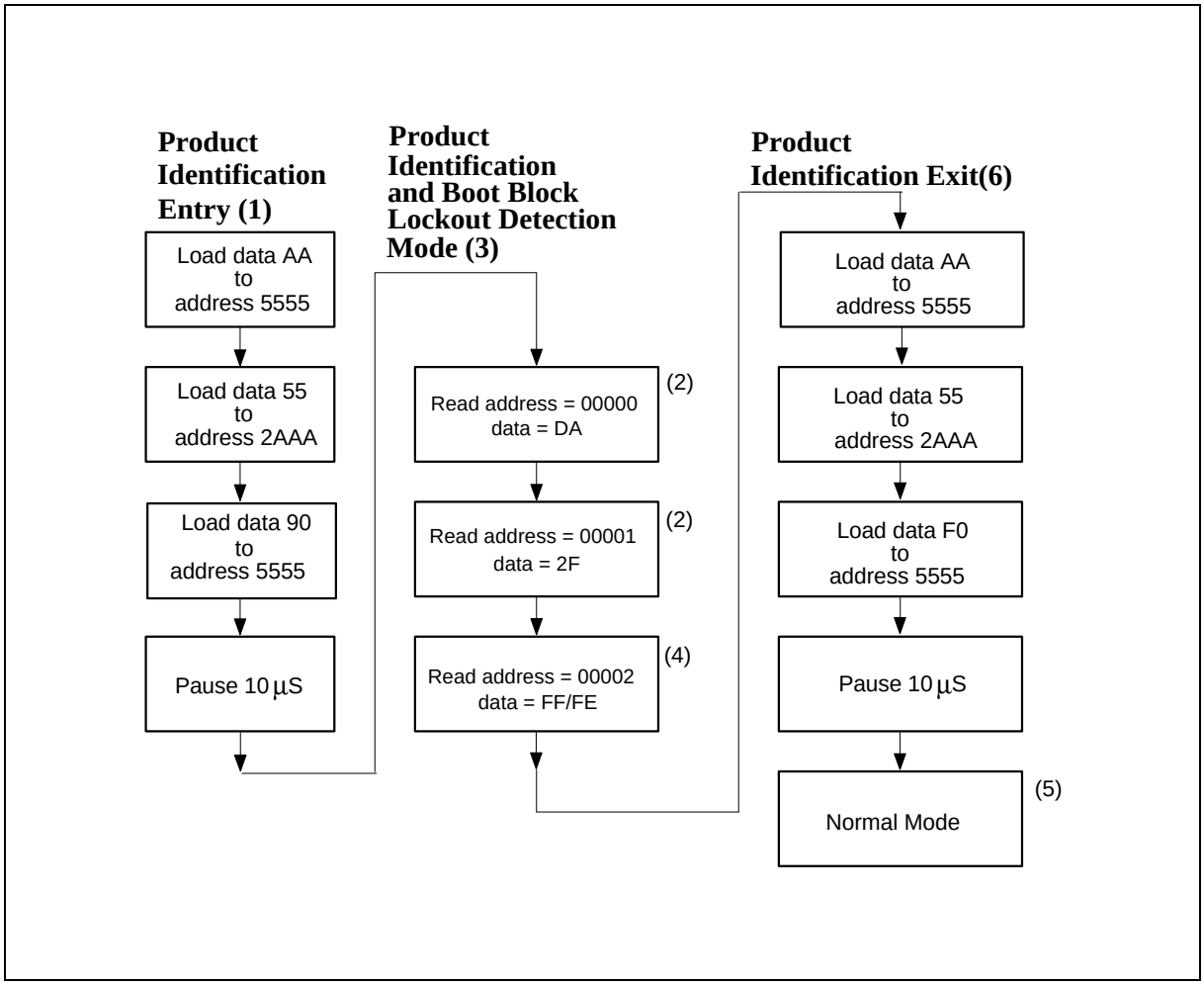
Embedded #Data Polling Algorithm



Embedded Toggle Bit Algorithm



Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ15 – DQ8 (Don't Care), DQ7 – DQ0 (Hex); Address Format: A14 – A0 (Hex)

(2) A1 – A15 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

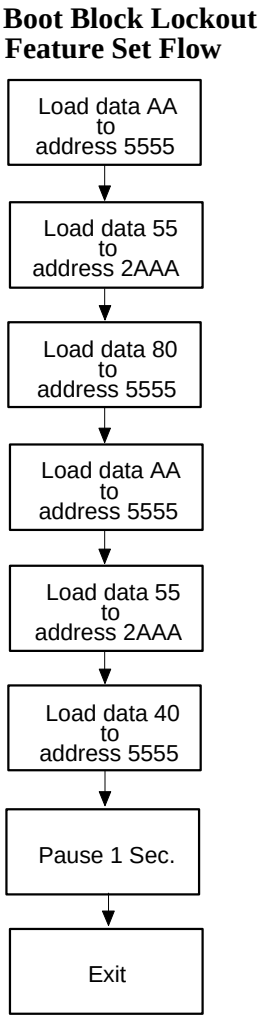
(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the output data is "FF Hex," the boot block programming lockout feature is activated; if the output data "FE Hex," the lockout feature is inactivated and the block can be programmed.

(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Boot Block Lockout Enable Acquisition Flow



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except A9	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{DD}	#CE = #OE = V_{IL}, #WE = V_{IH}, all I/Os open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	15	25	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	#CE = V_{IH}, all I/Os open Other inputs = V_{IL}/V_{IH}	-	-	1	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	#CE = V_{DD} -0.3V, all I/Os open Other inputs = V_{DD} -0.3V/ V_{SS}	-	10	50	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.6	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.1 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	200	µS
Power-up to Write Operation	$T_{PU. WRITE}$	10	mS

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

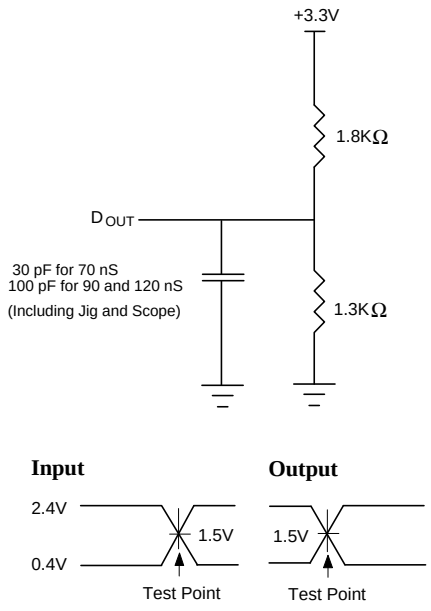
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.4V/2.4V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF for 70 nS C_L = 100 pF for 90 and 120 nS

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49L102-70B		W49L102-90B		W49L102-12B		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	120	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	-	120	nS
Address Access Time	T_{AA}	-	70	-	90	-	120	nS
Output Enable Access Time	T_{OE}	-	35	-	40	-	50	nS
#CE Low to Active Output	T_{CLZ}	0	-	0	-	0	-	nS
#OE Low to Active Output	T_{OLZ}	0	-	0	-	0	-	nS
#CE High to High-Z Output	T_{CHZ}	-	30	-	30	-	30	nS
#OE High to High-Z Output	T_{OHZ}	-	30	-	30	-	30	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	0	-	nS

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	10	-	-	nS
Address Hold Time	T_{AH}	100	-	-	nS
#WE and #CE Setup Time	T_{CS}	0	-	-	nS
#WE and #CE Hold Time	T_{CH}	0	-	-	nS
#OE High Setup Time	T_{OES}	0	-	-	nS
#OE High Hold Time	T_{OEH}	0	-	-	nS
#CE Pulse Width	T_{CP}	200	-	-	nS
#WE Pulse Width	T_{WP}	200	-	-	nS
#WE High Width	T_{WPH}	200	-	-	nS
Data Setup Time	T_{DS}	100	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Word Programming Time	T_{BP}	-	50	60	µS
Erase Cycle Time	T_{EC}	-	0.1	1	Sec.

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

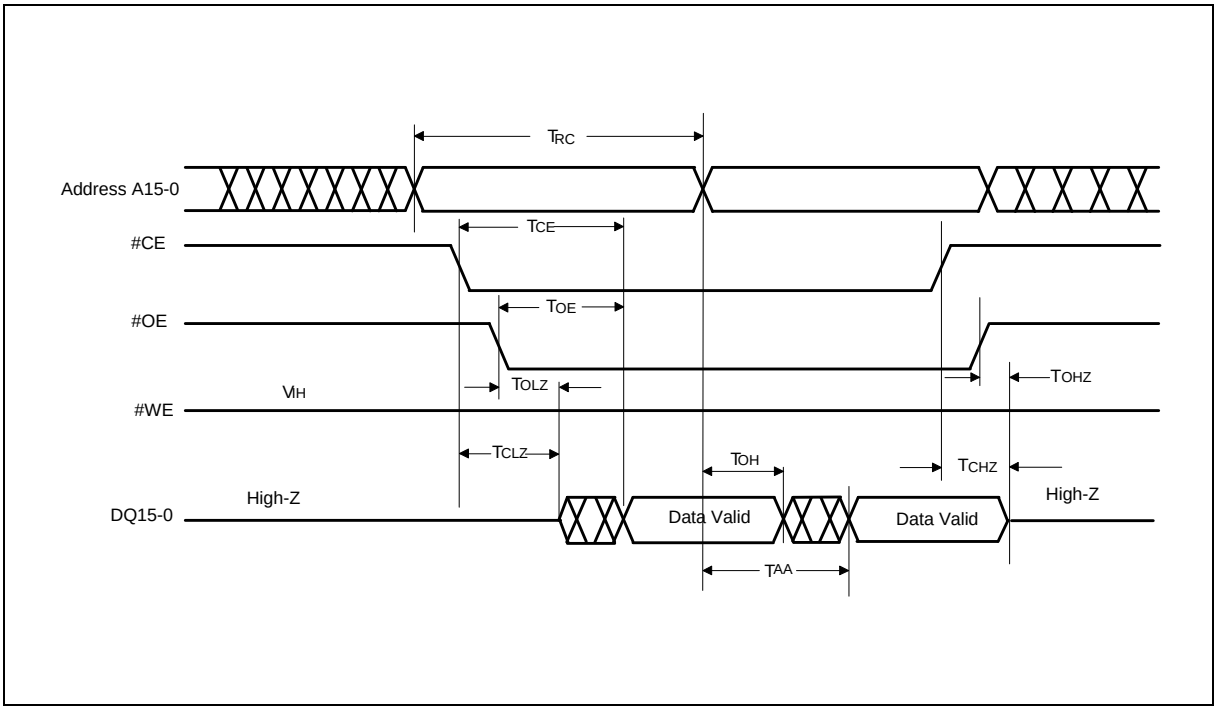
AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W49L102-70B		W49L102-90B		W49L102-12B		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
#OE to Data Polling Output Delay	T_{OEP}	-	35	-	40	-	50	nS
#CE to Data Polling Output Delay	T_{CEP}	-	70	-	90	-	120	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	35	-	40	-	50	nS
#CE to Toggle Bit Output Delay	T_{CET}	-	70	-	90	-	120	nS

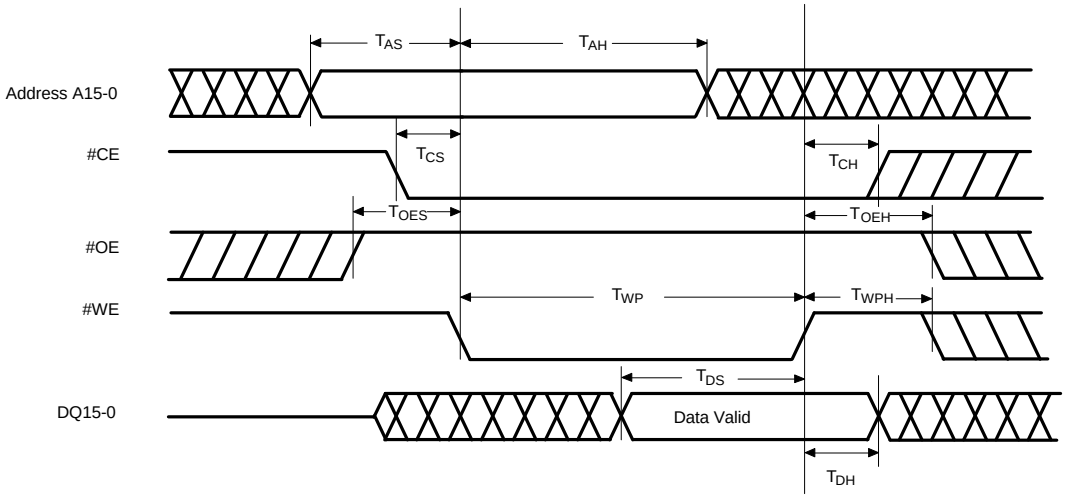
TIMING WAVEFORMS

Read Cycle Timing Diagram

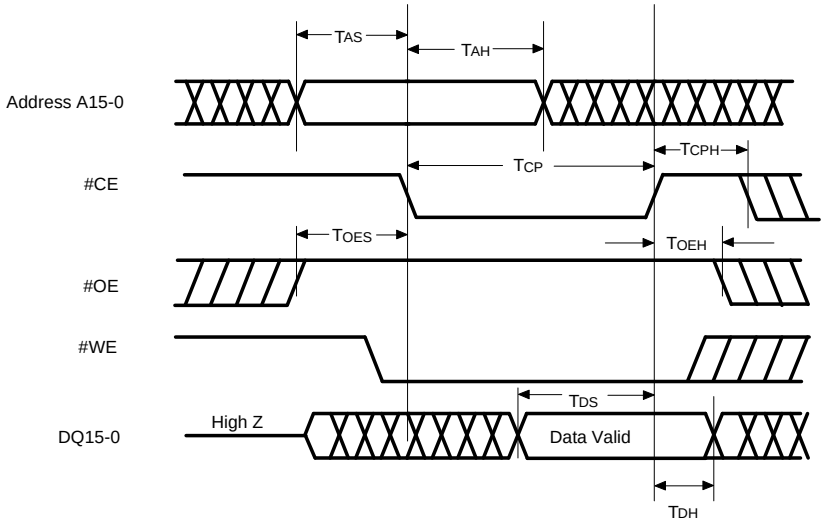


Timing Waveforms, continued

#WE Controlled Command Write Cycle Timing Diagram

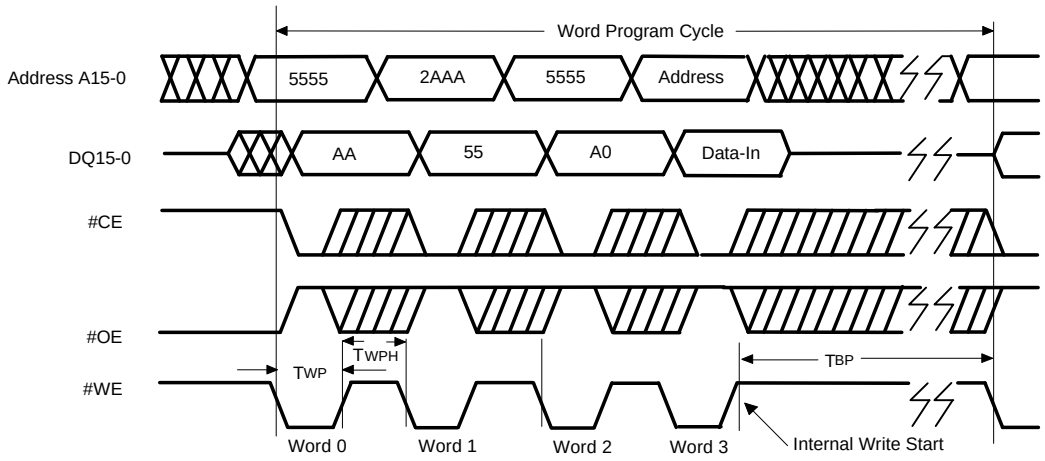


#CE Controlled Command Write Cycle Timing Diagram

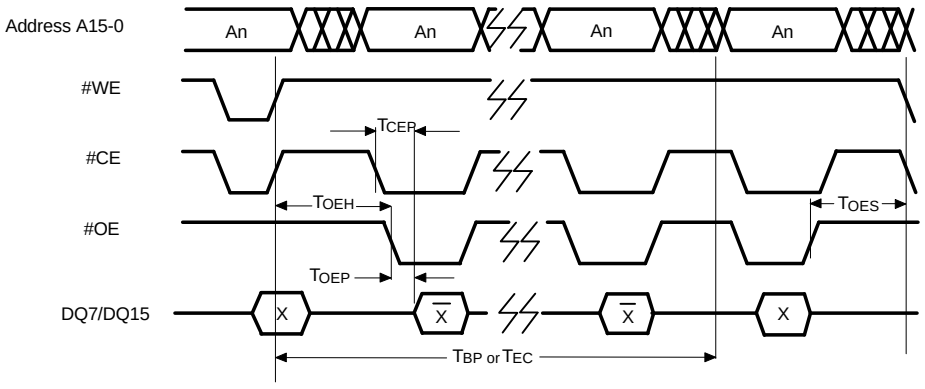


Timing Waveforms, continued

Program Cycle Timing Diagram

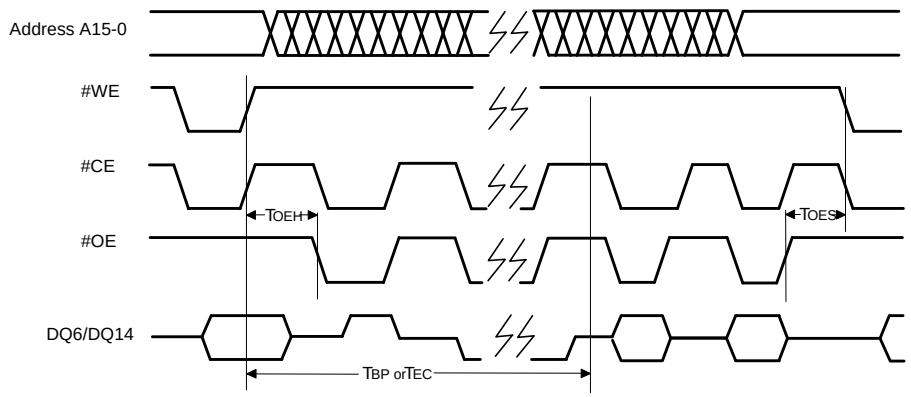


#DATA Polling Timing Diagram

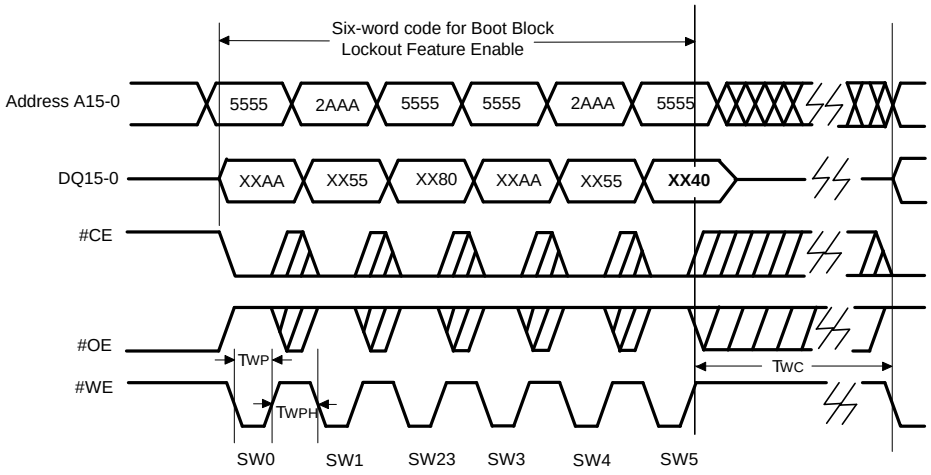


Timing Waveforms, continued

Toggle Bit Timing Diagram

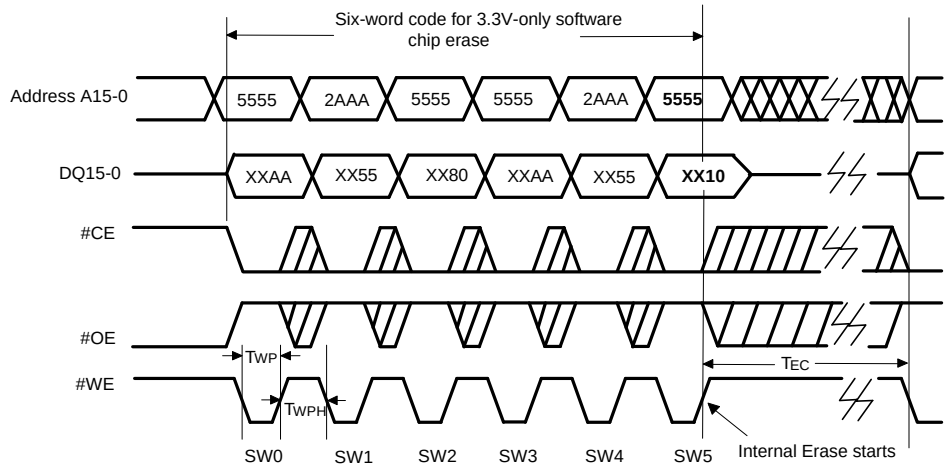


Boot Block Lockout Enable Timing Diagram

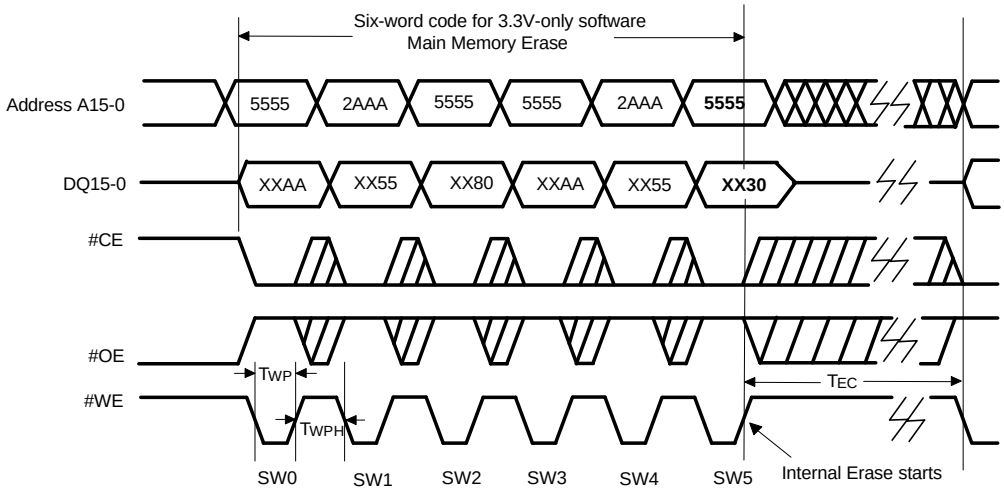


Timing Waveforms, continued

Chip Erase Timing Diagram



Main Memory Erase Timing Diagram



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (μA)	PACKAGE	CYCLE	HARDWARE SID READ FUNCTION
W49L102Q-70	70	25	50 (CMOS)	40-pin STSOP (10 mm × 14 mm)	10K	Y
W49L102Q-90	90	25	50 (CMOS)	40-pin STSOP (10 mm × 14 mm)	10K	Y
W49L102Q-12	120	25	50 (CMOS)	40-pin STSOP (10 mm × 14 mm)	10K	Y
W49L102P-70	70	25	50 (CMOS)	44-pin PLCC	10K	Y
W49L102P-90	90	25	50 (CMOS)	44-pin PLCC	10K	Y
W49L102P-12	120	25	50 (CMOS)	44-pin PLCC	10K	Y

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. In Hardware SID Read column: Y = with SID read function; N = without SID read function.

HOW TO READ THE TOP MARKING

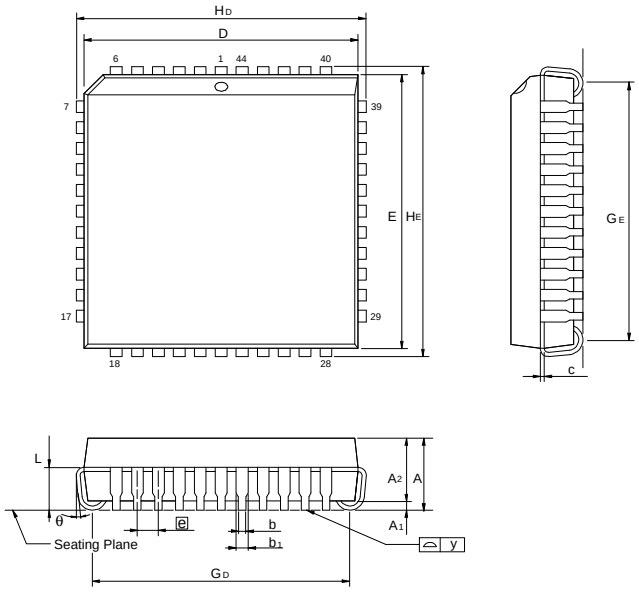
Example: The top marking of 44-pin PLCC W49L102

1st line: winbond logo
2nd line: the part number: W49L102
3rd line: the lot number
4th line: the tracking code: 149 O B SA

149: Packages made in 01, week 49
O: Assembly house ID: A means ASE, O means OSE, ...etc.
B: IC revision; A means version A, H means version H, … etc.
SA: Process code

PACKAGE DIMENSIONS

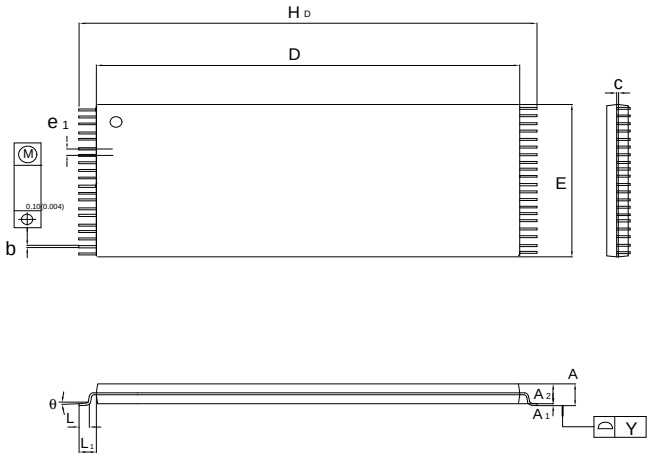
44-pin PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

40-pin STSOP (10 mm ´ 14 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.484	0.488	0.492	12.30	12.40	12.50
E	0.390	0.394	0.398	9.90	10	10.10
H_D	0.543	0.551	0.559	13.80	14.00	14.20
e	—	0.020	—	—	0.50	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1	—	0.031	—	—	0.8	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 1999	-	Renamed from W29N102C
A2	Jan. 2001	4, 5, 9	Change Device Code from BF to 2F
		1, 12, 13, 14, 19	Delete 55 nS
		1, 19	Endurance: 10K cycles
		13	Change Word Programming Time (T_{BP}) as 50 μS (typ.) and 60 μS (max.)
		1, 12, 13, 14, 19	Add in 120 nS
A3	Feb. 2001	4, 19	Add in Hardware SID Read function note
		19	Correct Part No. in Ordering Information
A4	Feb. 19, 2002	1, 2, 19, 21	Rename TSOP (10 x 14 mm) as STSOP (10 x 14 mm)
		4	Modify V_{DD} Power Up/Down Detection In Hardware Data Protection
		6, 7, 8	Delete old flow chart and add embedded algorithm
		19	Add HOW TO READ THE TOP MARKING
		19	Remove Part. No of W49L102Q-70N & W49L102P-70N for ordering information

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu Chiu, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064