Description

The 256Mb DDR SDRAM is a high-speed COMS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM. The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 256Mb DDR SDRAM operates from a differential clock (CLK and CLK#; the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is latched by both edges of DQS with DQS aligned to center of data packet, and output data is latched by both edges of DQS with DQS aligned to edge of data packet.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The 256Mb DDR SDRAM is designed to operate in either low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation. This is the only normal operating mode for these DDR devices.

Operating Frequencies

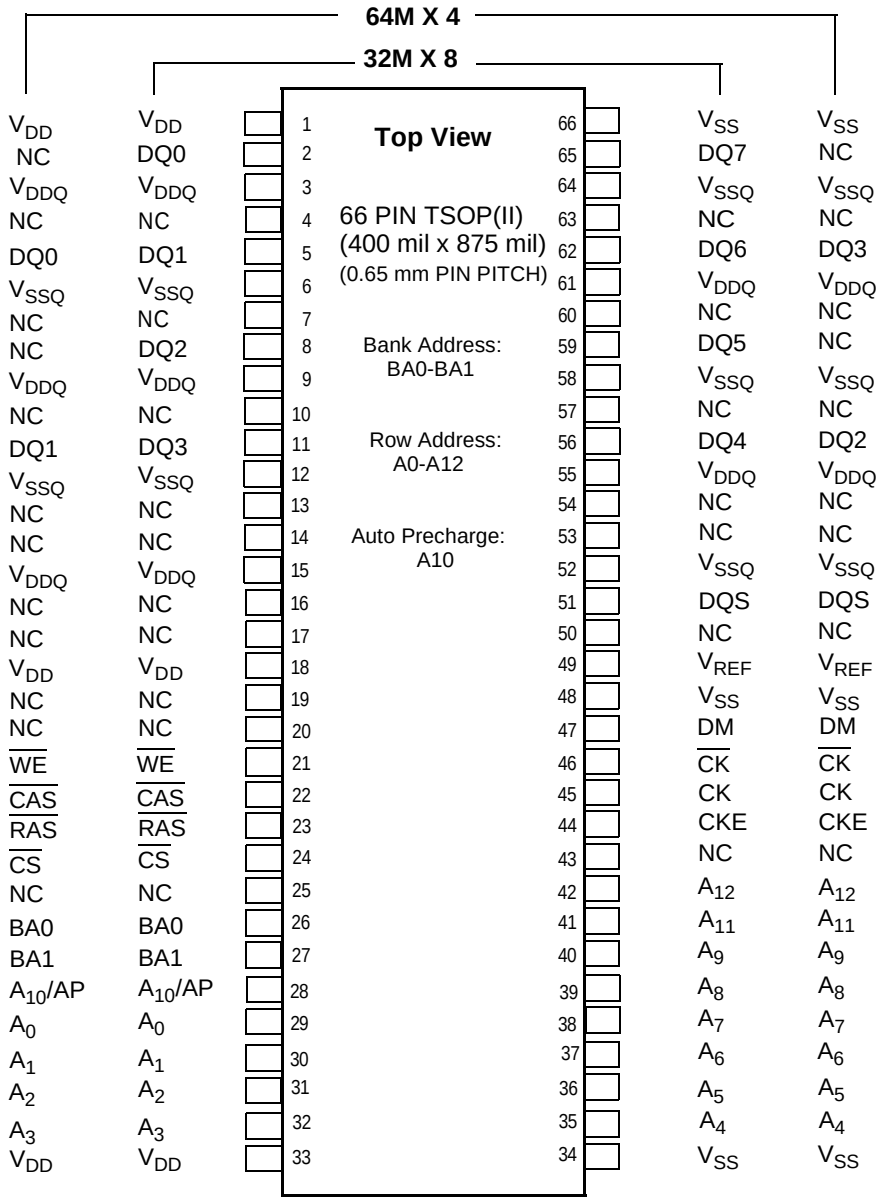
Part Number	Cycle time	Standard
VG3725640(80)2AT-66	6.6 ns (150MHz CL=2.5) 7.5 ns (133MHz CL=2)	DDR300
VG3725640(80)2AT-7L	7.5 ns (133MHz CL=2) 7.5 ns (133MHz CL=2.5)	DDR266A
VG3725640(80)2AT-75	7.5 ns (133MHz CL=2.5) 10 ns (100MHz CL=2)	DDR266B
VG3725640(80)2AT-8	8 ns (125MHz CL=2.5) 10 ns (100MHz CL=2)	DDR200

Features

- JEDEC standard
- Double-data-rate architecture: two data transfers per clock cycle
- Bidirectional, intermittent data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs, and center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL aligns DQ and DQS transitions with CLK transitions
- Commands entered on each positive CLK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8 (programmable)
- CAS Latency: 2, 2.5 (programmable)
- Burst type: sequential / interleave (programmable)
- AUTO PRECHARGE / All bank precharge controlled by A10
- Auto Refresh and Self Refresh Modes
- 8192 refresh cycles / 64ms (4 banks concurrent refresh)
- 2.5V (SSTL_2 compatible) I/O
- 400-mil, 66-pin TSOP II

Pin Configuration

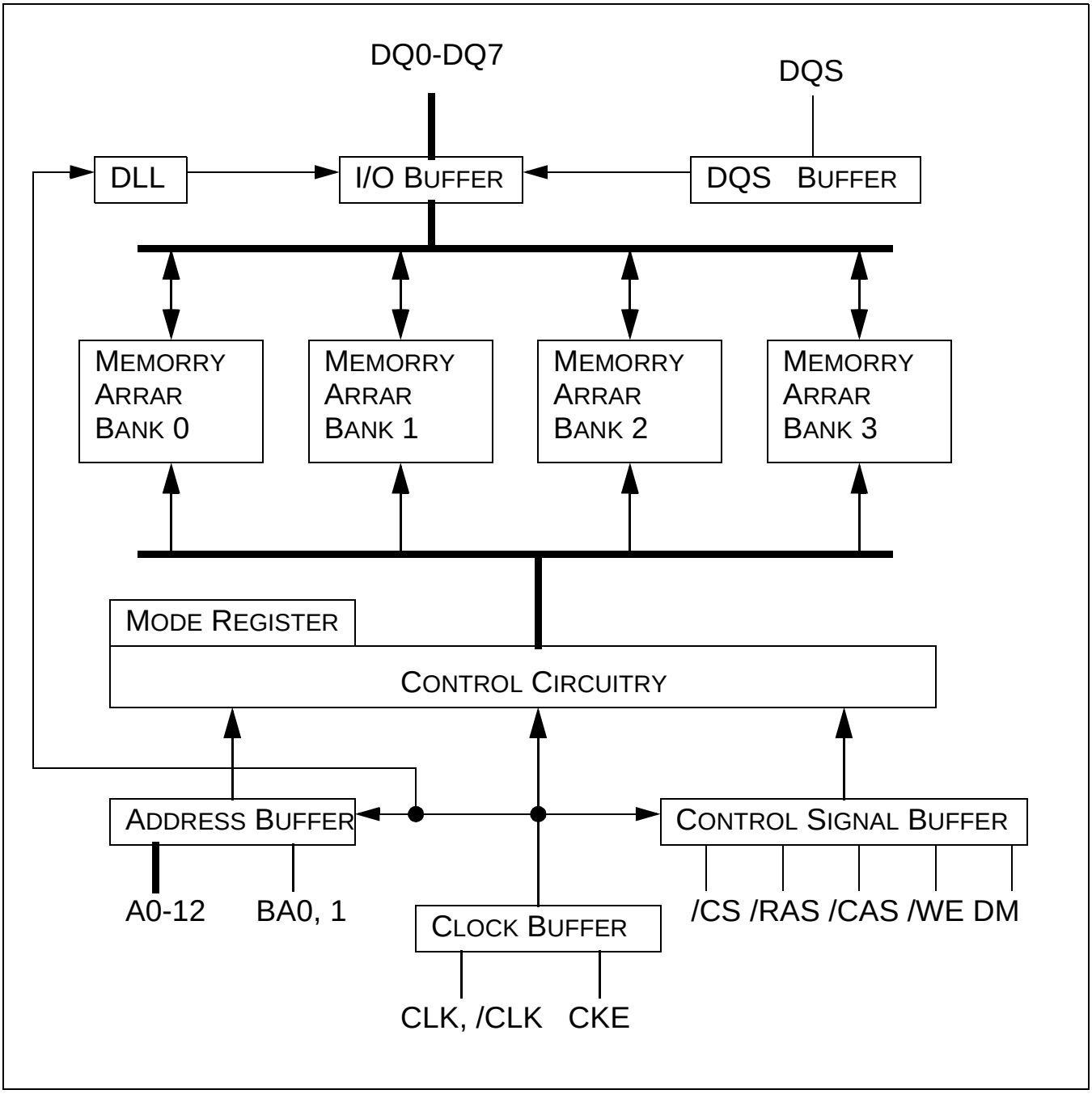
256M DDR SDRAM (x4/x8) Pin-out



Column Address Table

Organization	Column Address
32Mx8	A0-A9
64Mx4	A0-A9, A11

FUNCTIONAL BLOCK DIAGRAM



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not necessarily represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

PIN DESCRIPTIONS

Symbol	Type	Description
CLK,CLK#	Input	Clock: CLK and CLK# are differential clock inputs. All address and control input signals are sampled on the positive edge of CLK (negative edge of CLK#). Output (read) data is referenced to both edges of CLK. Internal clock signals are derived from CLK/ CLK#.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CLK, CLK# and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
RAS#,CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to match the DQ and DQS loading.
BA0,BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0-A12	Input	Address Inputs: Provide the row address for ACTIVE commands and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0,BA1. The address inputs also provide the op-code during a MODE REGISTER SET command.
DQ	I/O	Data Input/Output: Data bus
DQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
NC	-	No Connect: these pins should be left unconnected.
V_{DDQ}	Supply	DQ Power Supply:+2.5V ±0.2V .
V_{SSQ}	Supply	DQ Ground.
V_{DD}	Supply	Power Supply: +2.5V ±0.2V .
V_{SS}	Supply	Ground.
V_{REF}	Input	SSTL_2 reference voltage.

Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. No power sequencing is specified during power up or power down given the following criteria:

- VDD and VDDQ are driven from a single power converter output, and
- VTT is limited to 1.44V (reflection VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation),and
- VREF tracks VDDQ/2,and
- A minimum resistance of 42 ohms(22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.

If the above Criteria cannot be met by the system design, then the following table must be adhered to during power up:

Voltage Description	Sequencing	Voltage Relationship to avoid latch-up
$V_{DD}Q$	After or with V_{DD}	< V_{DD} + 0.3V
V_{TT}	After or with $V_{DD}Q$	< $V_{DD}Q$ + 0.3V
V_{REF}	After or with $V_{DD}Q$	< $V_{DD}Q$ + 0.3V

Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up will put the DQ and DQS outputs in the High-Z stage, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200μs delay prior to applying an executable a command.

Once the 200μs delay has been satisfied, a DSEL or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Registerand to reset DLL. Then two or more AUTO REFRESH cycles must be performed. 200 clock cycles are required before any read command after the AUTO REFRESH cycles. After these sequences, the SDRAM is in idle state and ready for normal operation.

Register Definition

Mode Register

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 1. The mode register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is programmed again or the device loses power.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A11 specify the operating mode.

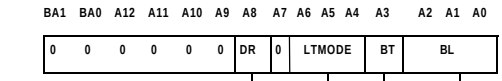
The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. the burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.



* BA1 and BA0 must be 0, 0 to select the mode register (vs. the extended mode register).

DLL Reset	0	No
	1	Yes

A2 A1 A0	Burst Length	
	A3=0	A3=1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

A3	Burst Type
0	Sequential
1	Interleaved

A6 A5 A4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

A 11	A 10	A 9	A 8	A 7	A6-A0	Operating Mode
0	0	0	0	0	Valid	Normal Operation
0	0	0	1	0	Valid	Reset DLL
0	0	0	0	1	VS*	Test Mode
-	-	-	-	-	-	All other states reserved

*:VS = Vendor Specific

Figure 1

MODE REGISTER DEFINITION

Table 1

BURST DEFINITION

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1-A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data-element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2, or 2.5 clocks.

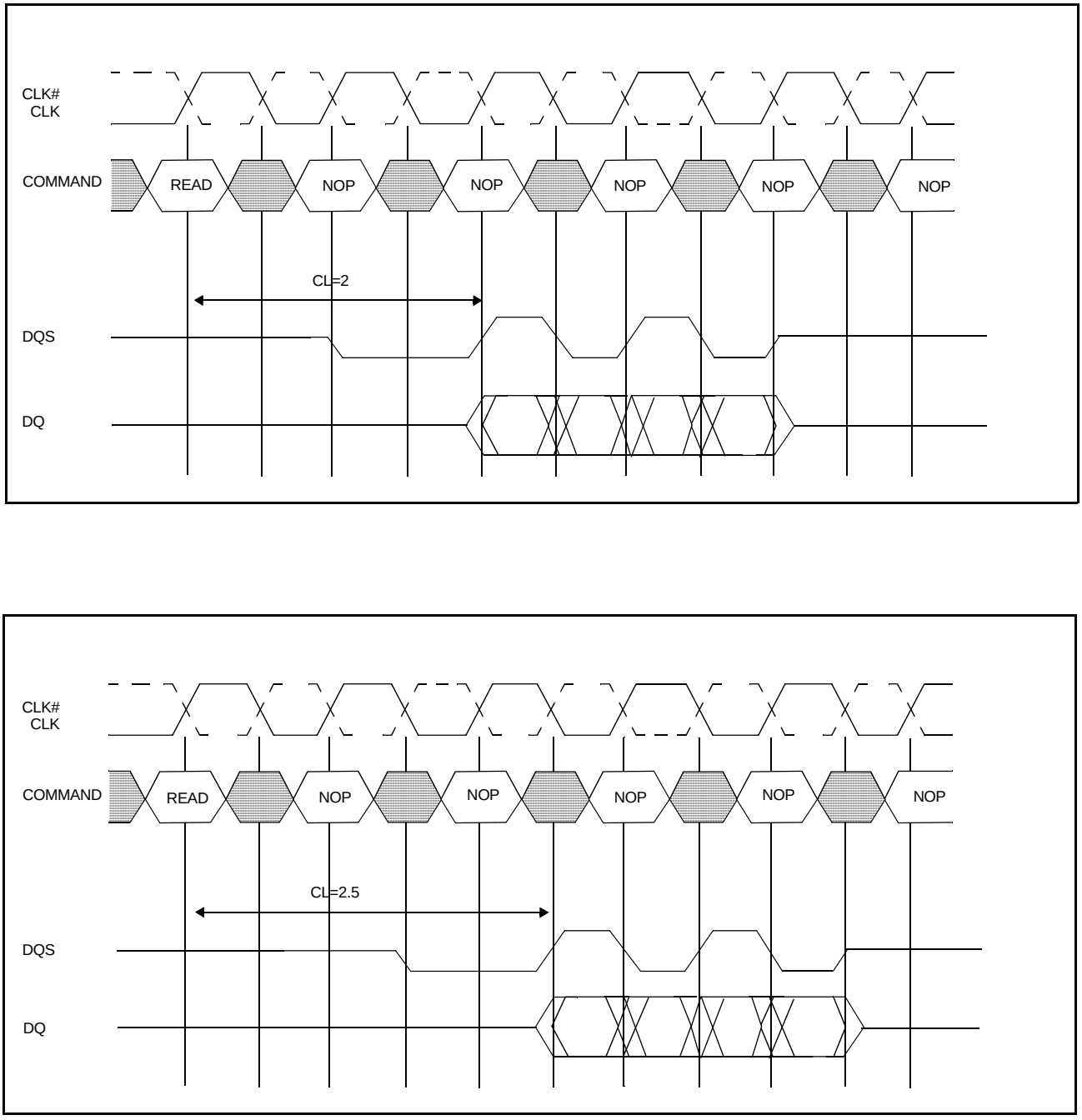
If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m shown in Fig. 2.

Reserved stated should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting A7-A12 to zero; to reset the DLL and select normal operation, program A7, A9-A12 to 0 and A8 to 1. All other combinations of values for A7-A12 are reserved for future use and/ or test modes.

Test Modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.



Burst Length=4 in the cases shown

Figure 2
CAS LATENCIES = 2 or 2.5

EXTENDED MODE REGISTER

The Extended Mode Resister is used to enable/disable the DLL of the DDR SDRAM, and select the drive strength as shown in Figure 3. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=0 and BA0=1) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle, and the controller must wait tMRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

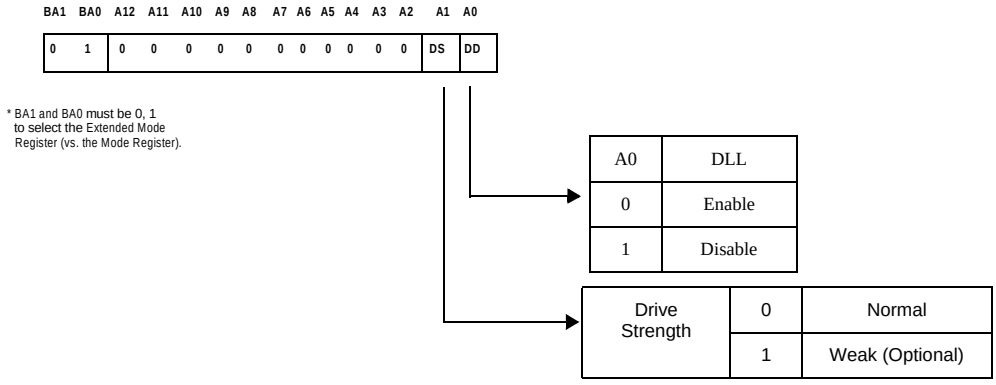


Figure 3 EXTENDED MODE REGISTER

COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1-Commands and DM Operation
(Notes:1)

Burst Length	CS#	RAS#	CAS#	WE#	DM	ADDR	DQs	NOTES
DSEL	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	X	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	X	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	9
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6,7
MODE REGISTER SET	L	L	L	L	X	Op-Code	X	2
Write Enable	-	-	-	-	L	-	Active	8
Write Inhibit	-	-	-	-	H	-	High-Z	8

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.

2. BA0-BA1 select either the Mode Register or the Extended Mode Register (BA0=0, BA=1 selects Mode Register; BA0=1, BA1=0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A11 provide the op-code to be written to the selected mode Register).
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0-BA1 provide bank address; A0-Ai provide column address (where i=9 for x8 and 11 for x4 except A10); A10 HIGH enables the auto precharge feature (non-persistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0-BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Used to mask write data; provided coincident with the corresponding data.
9. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts

DSEL

The DSEL function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an DDR SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0-A11 See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai (where i=9 for x8 or for x 4, including A11) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai (where i=9 for x8 or for x 4, including A11) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is non-persistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS# BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are “Don’t Care” during SELF REFRESH.

Once self refresh mode is engaged, the DDR SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The DDR SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for ^{t}XNR or ^{t}XRD because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command). a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

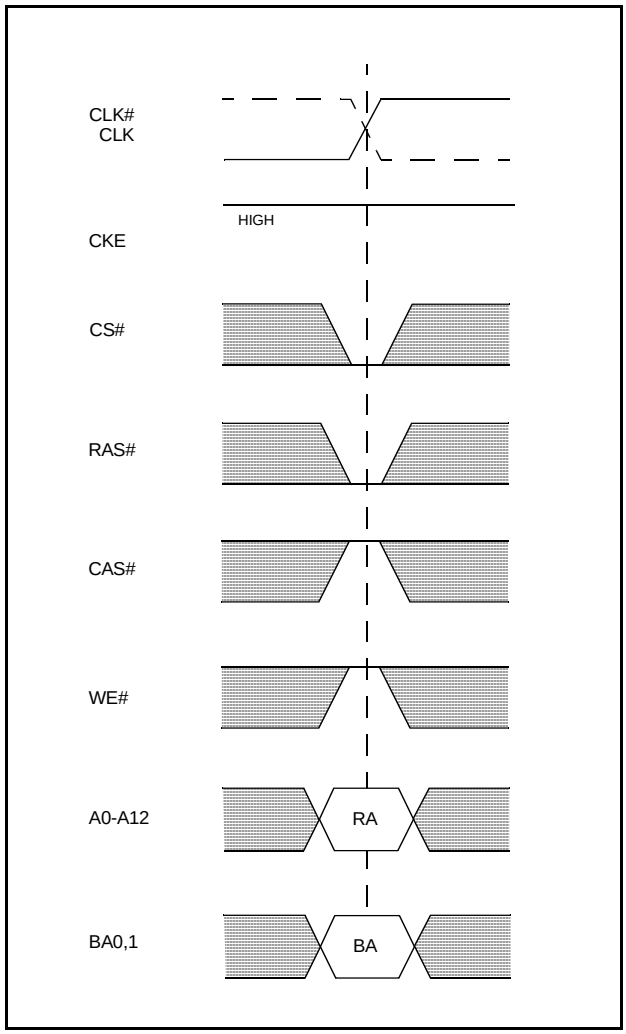


Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

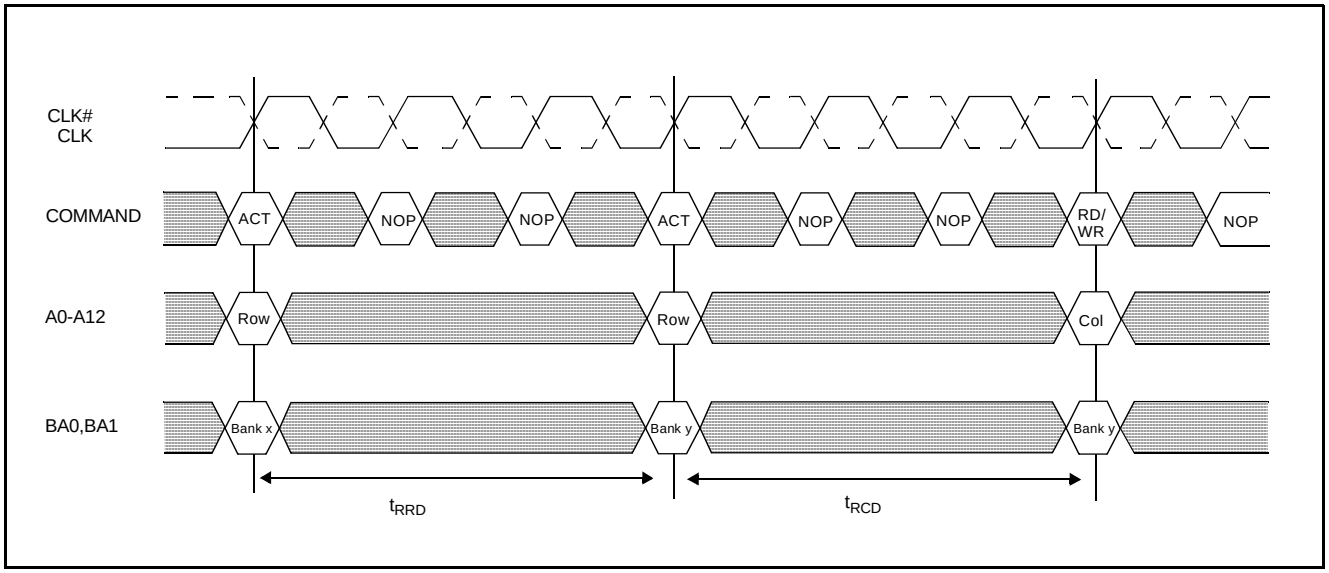


Figure 5
t_{RCD} AND t_{RRD} Definition

READs

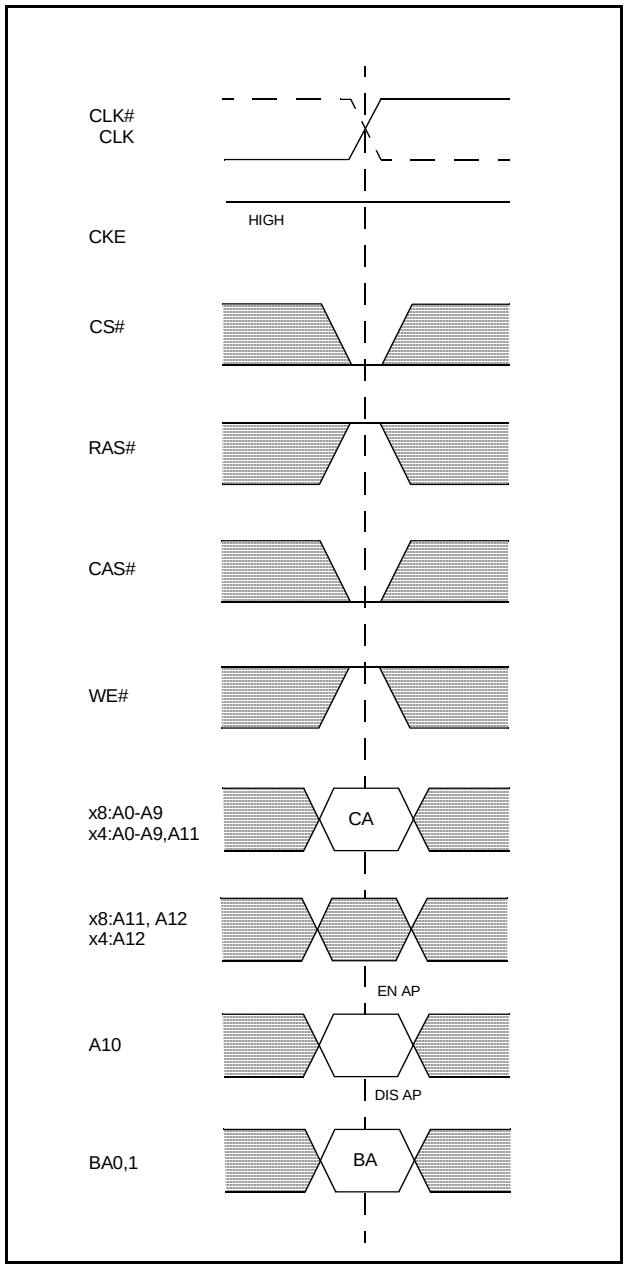
READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CLK and CLK#). Figure 7 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

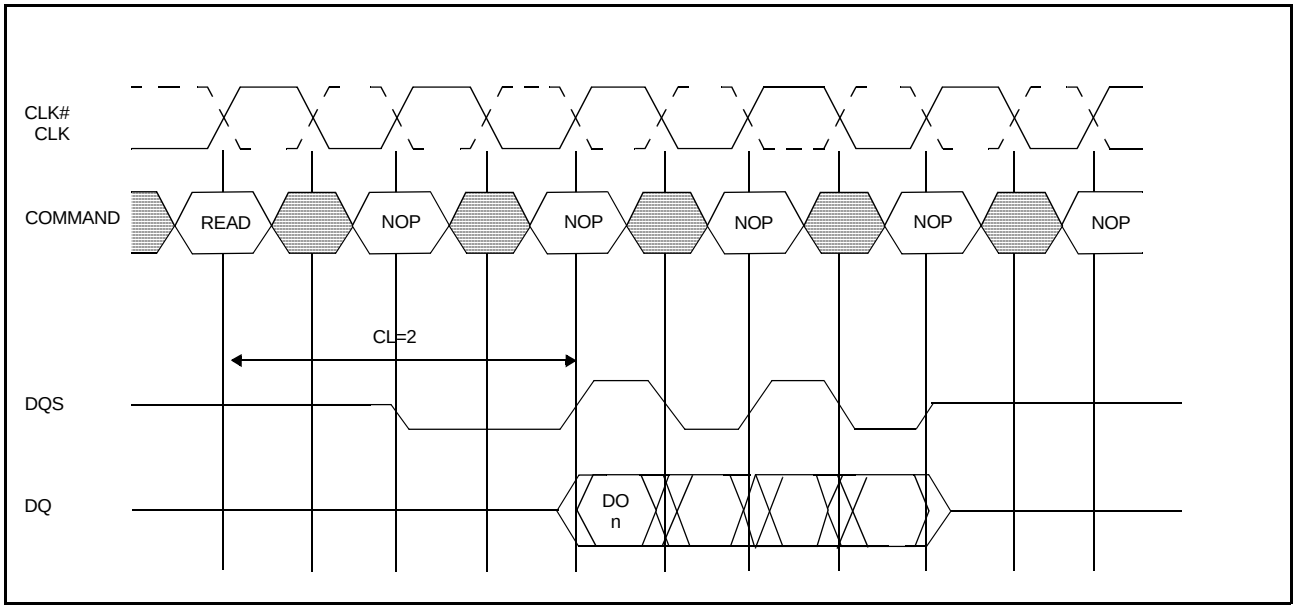
Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follow either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 8. A READ command can be initiated on any clock cycle

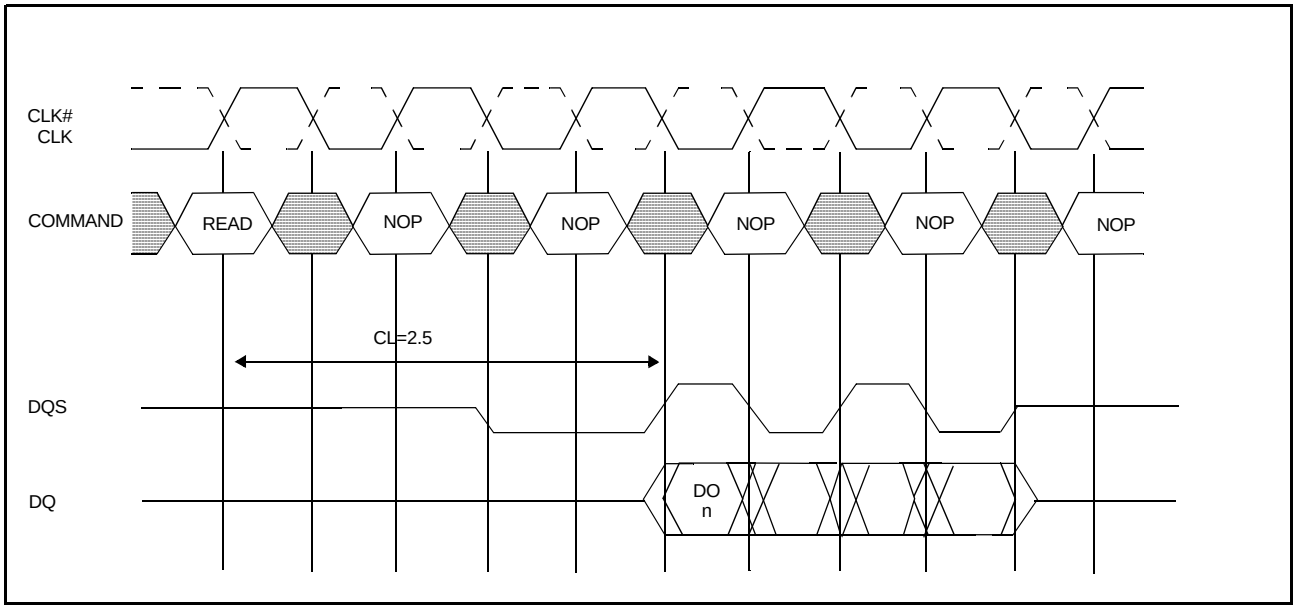


=DON'T CARE

CA = Column Address
BA = Bank Address
EN AP = Enable Autoprecharge
DIS AP = Disable Autoprecharge

Figure 6
READ COMMAND

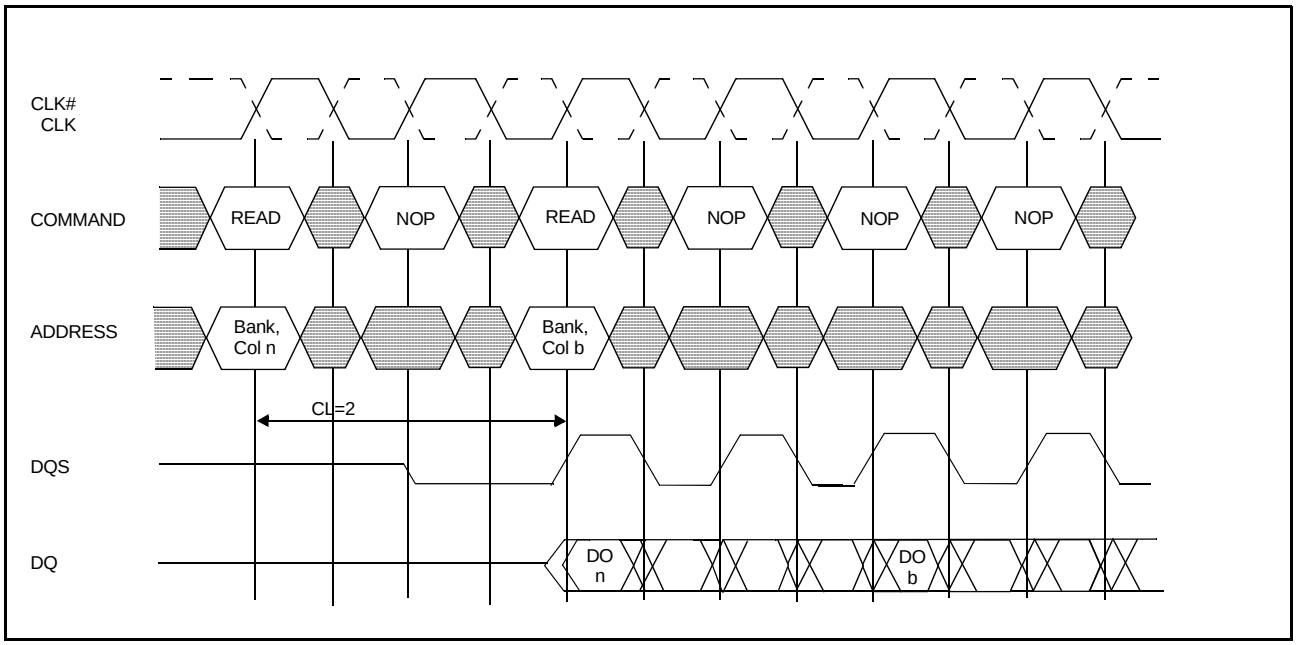


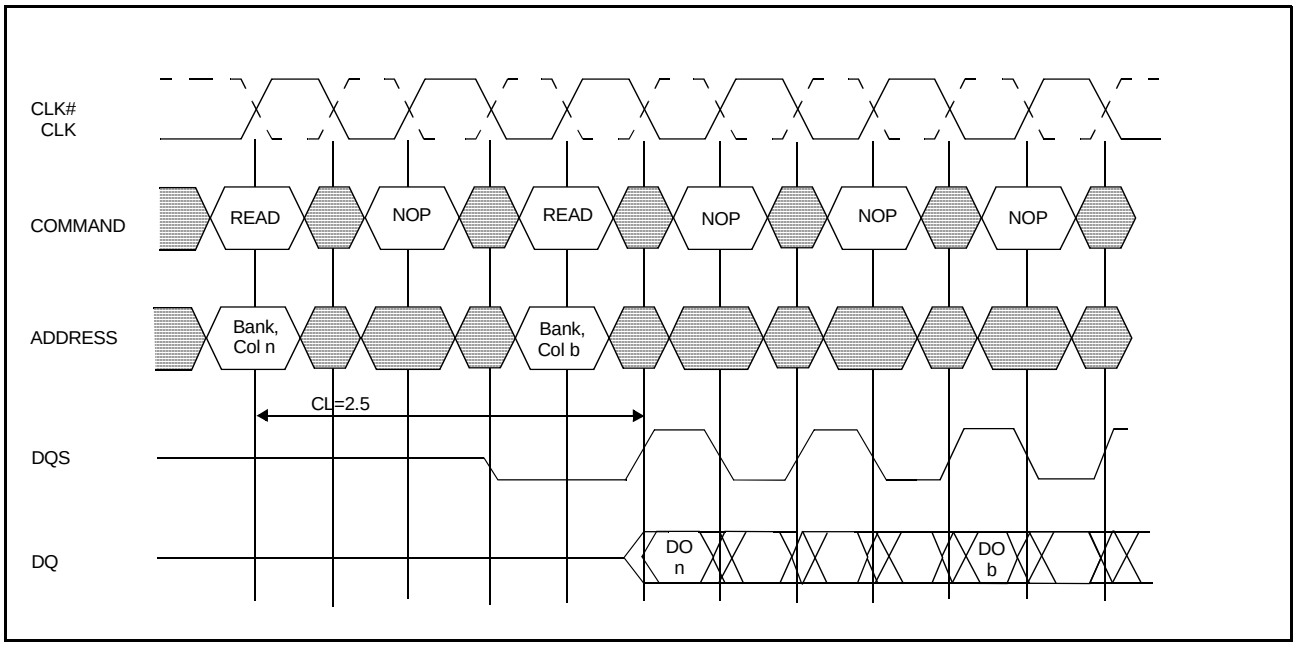


DON'T CARE

DO n=Data Out from column n
Burst Length=4
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 7
READ BURST

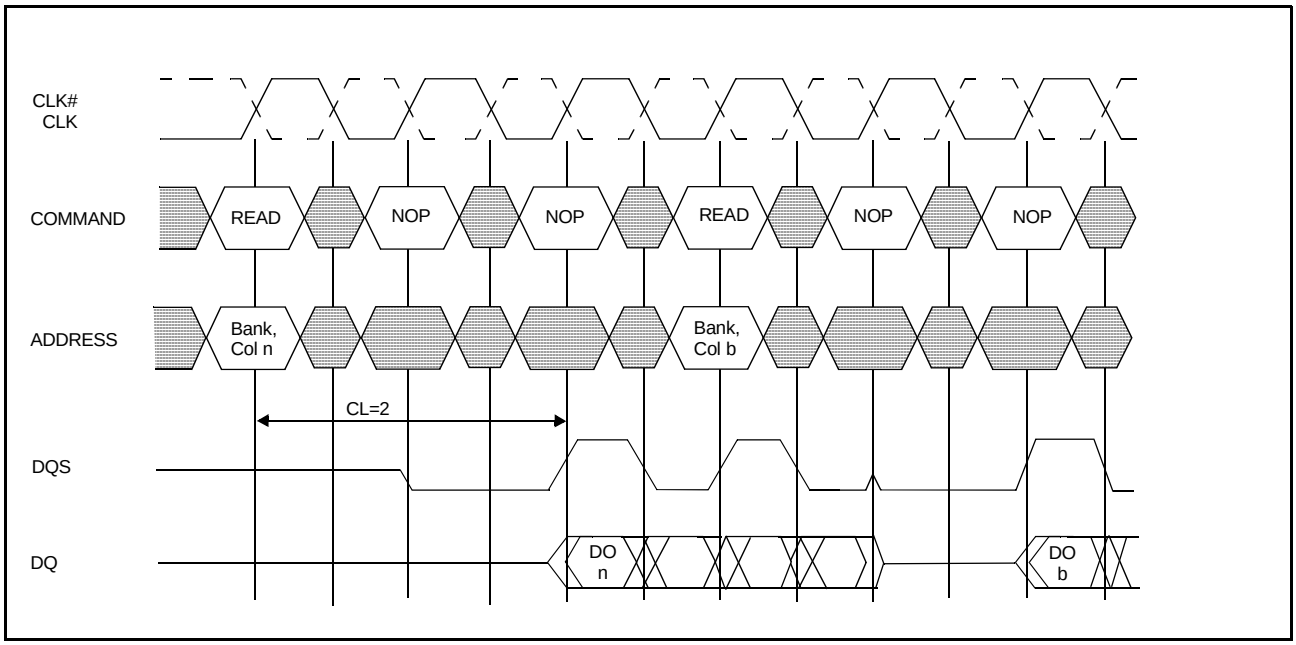


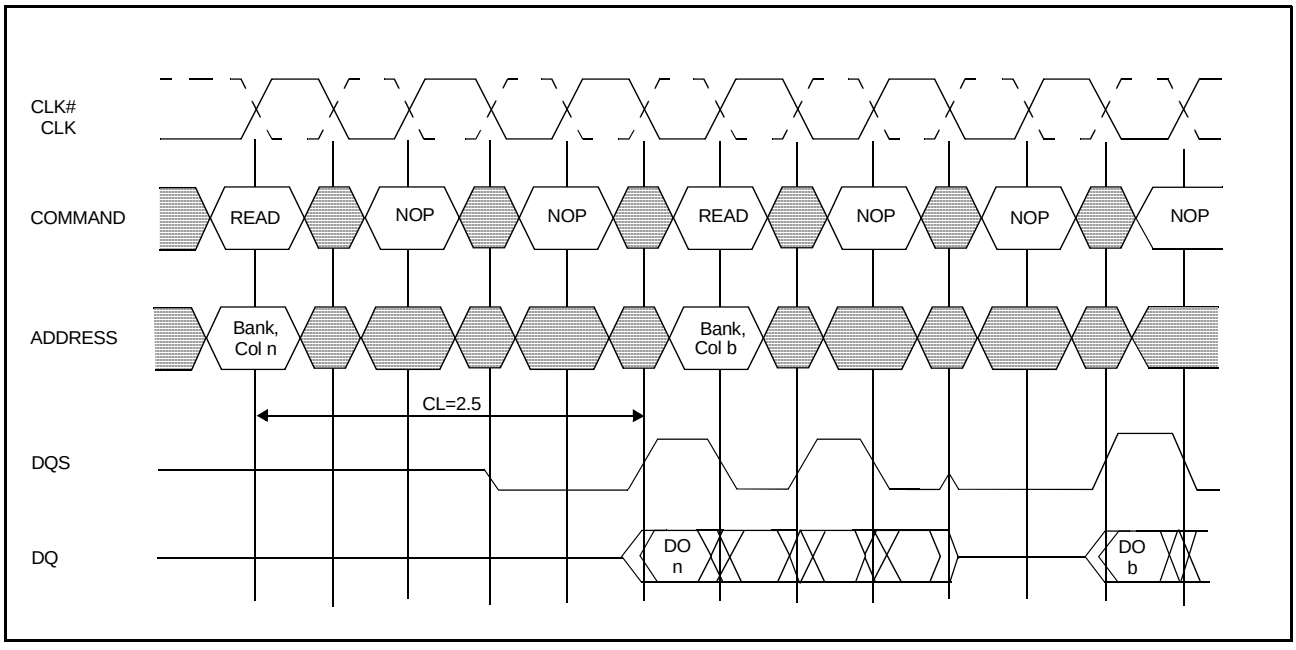


DON'T CARE

Do n (or b)= Data Out from column n (or column b)
Burst Length= 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

Figure 8
CONSECUTIVE READ BURSTS

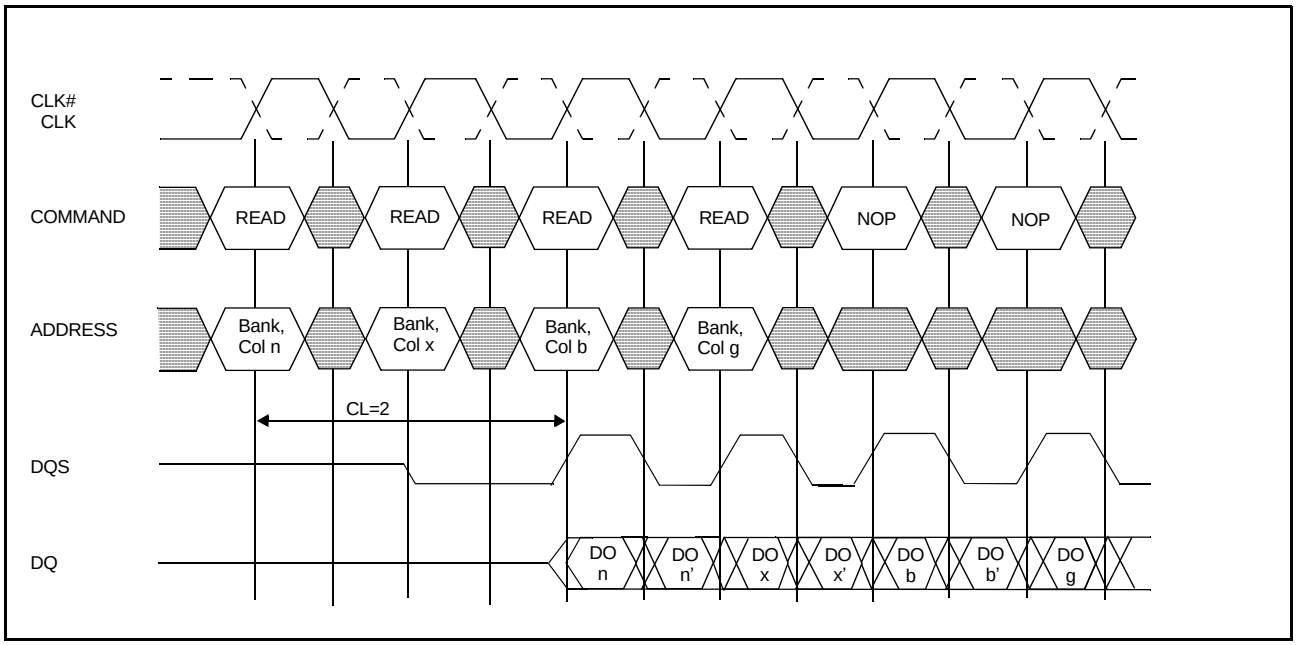


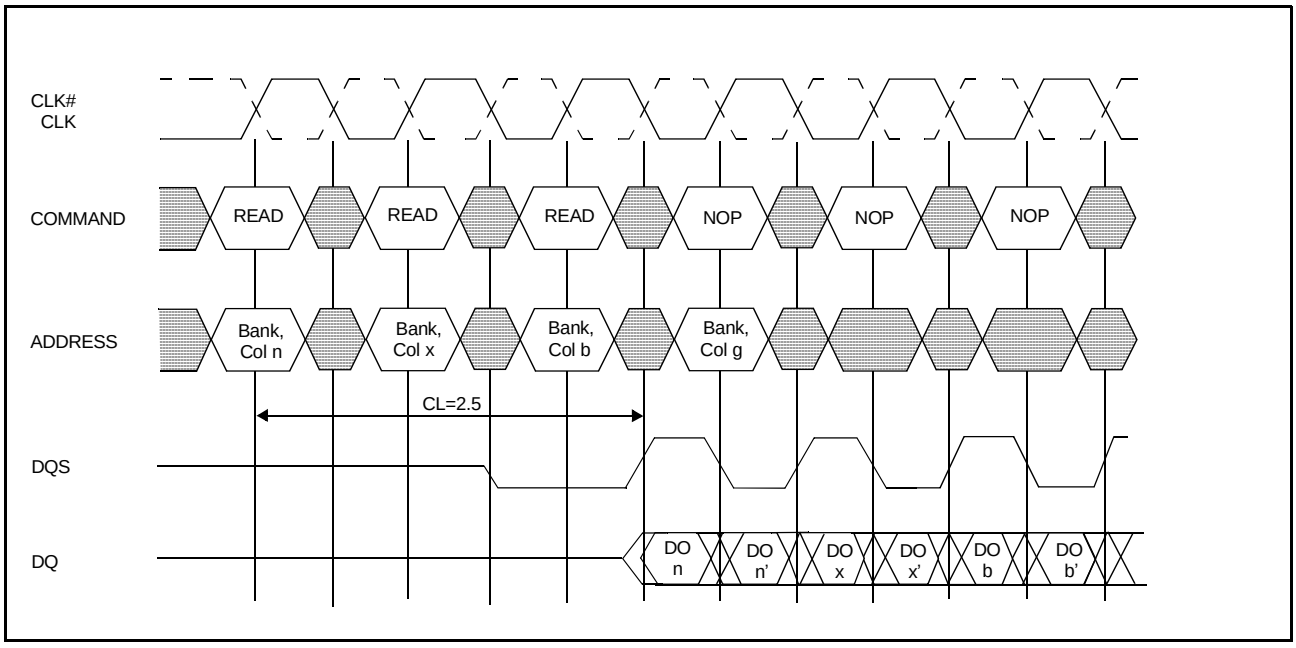


DON'T CARE

DO n (or b)=Data Out from column n (or column b)
Burst Length=4
3 Subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Figure 9
NON-CONSECUTIVE READ BURSTS





DON'T CARE

DO n, etc.= Data Out from column n, etc.
n' , etc.=odd or even complement of n, etc. (i.e. column address LSB inverted)
Burst Length=2,4 or 8 in cases shown
Reads are to active rows in any banks

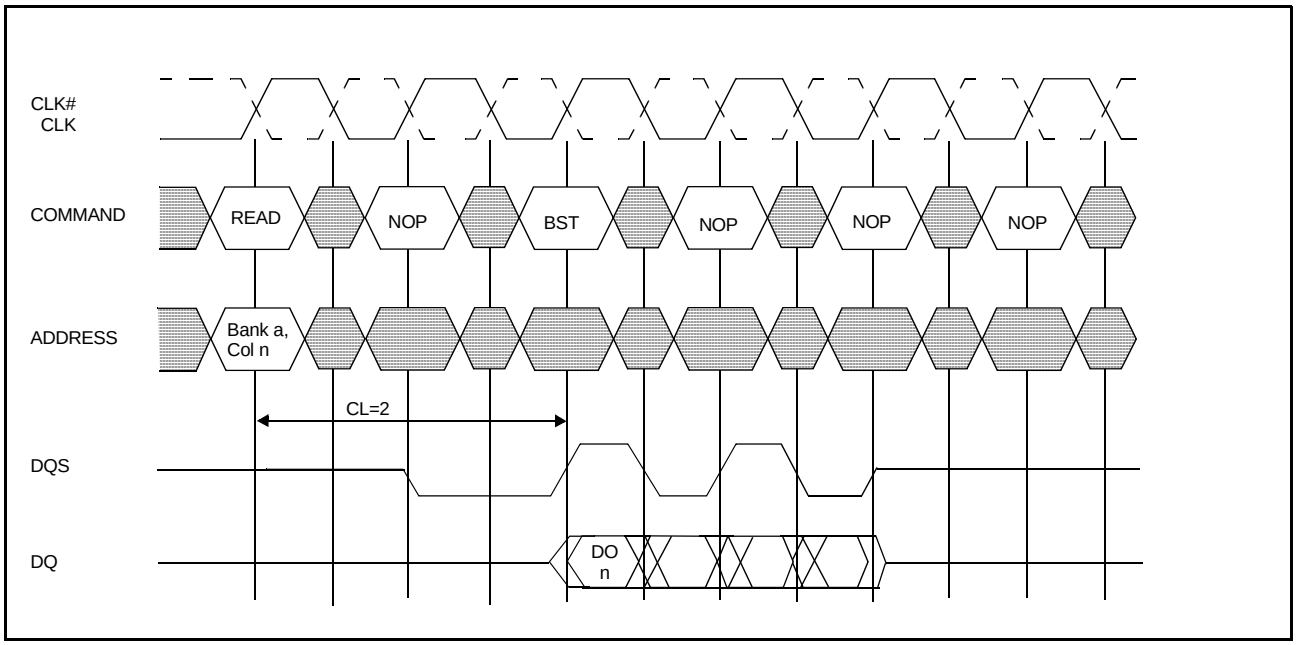
Figure 10
RANDOM READ ACCESSES

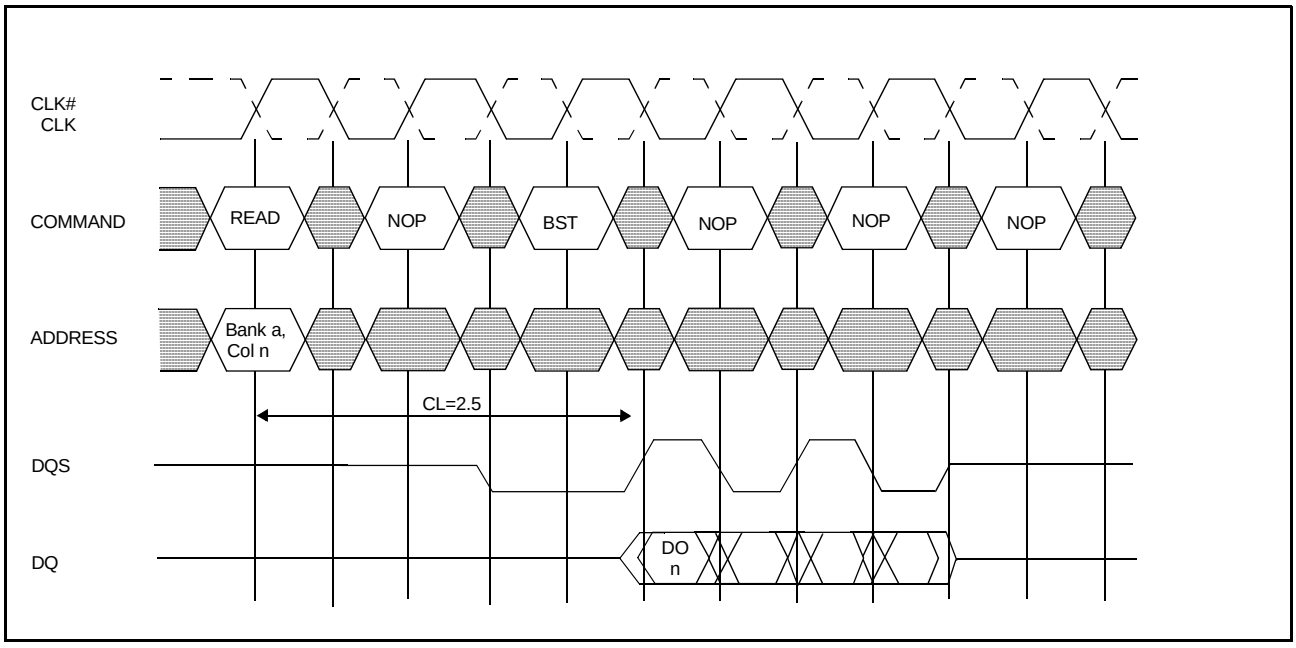
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e. the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITEs).

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element paires (pairs are required by the 2n prefetch architecture). This is shown if Figure 13 for READ latencies of 2,2.5 . Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion. a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the precharge command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

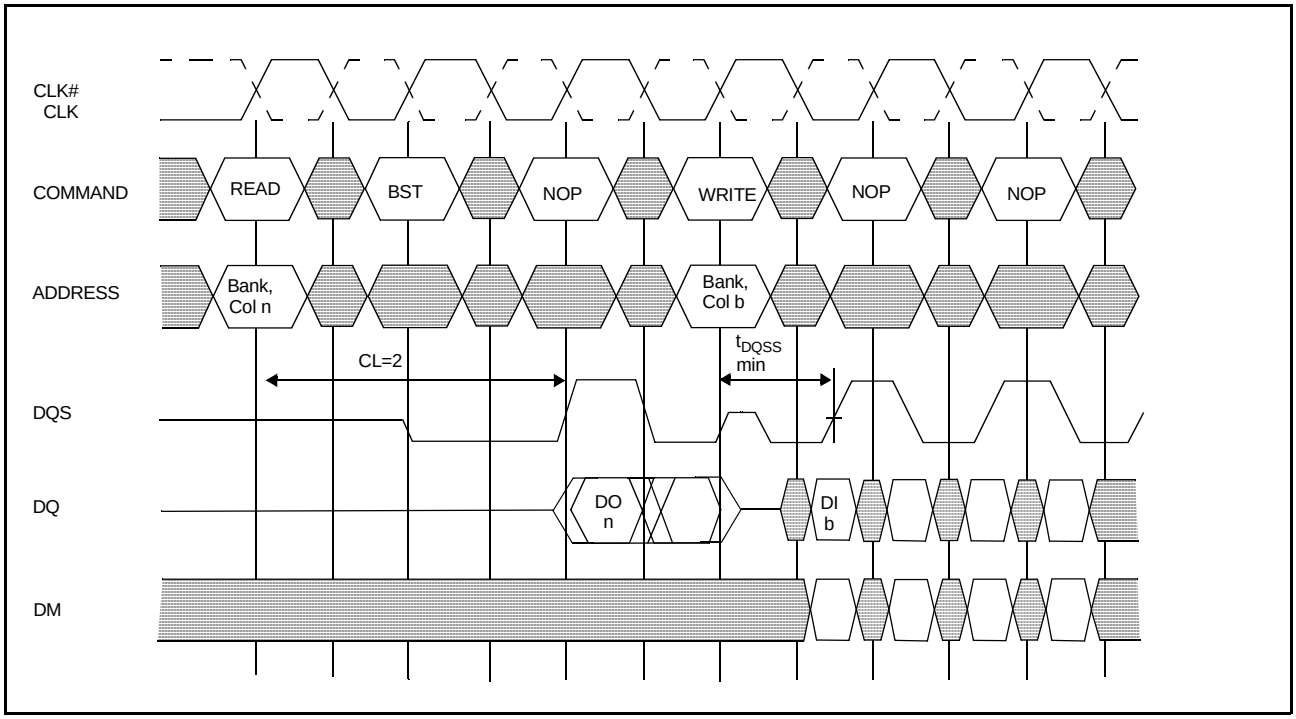


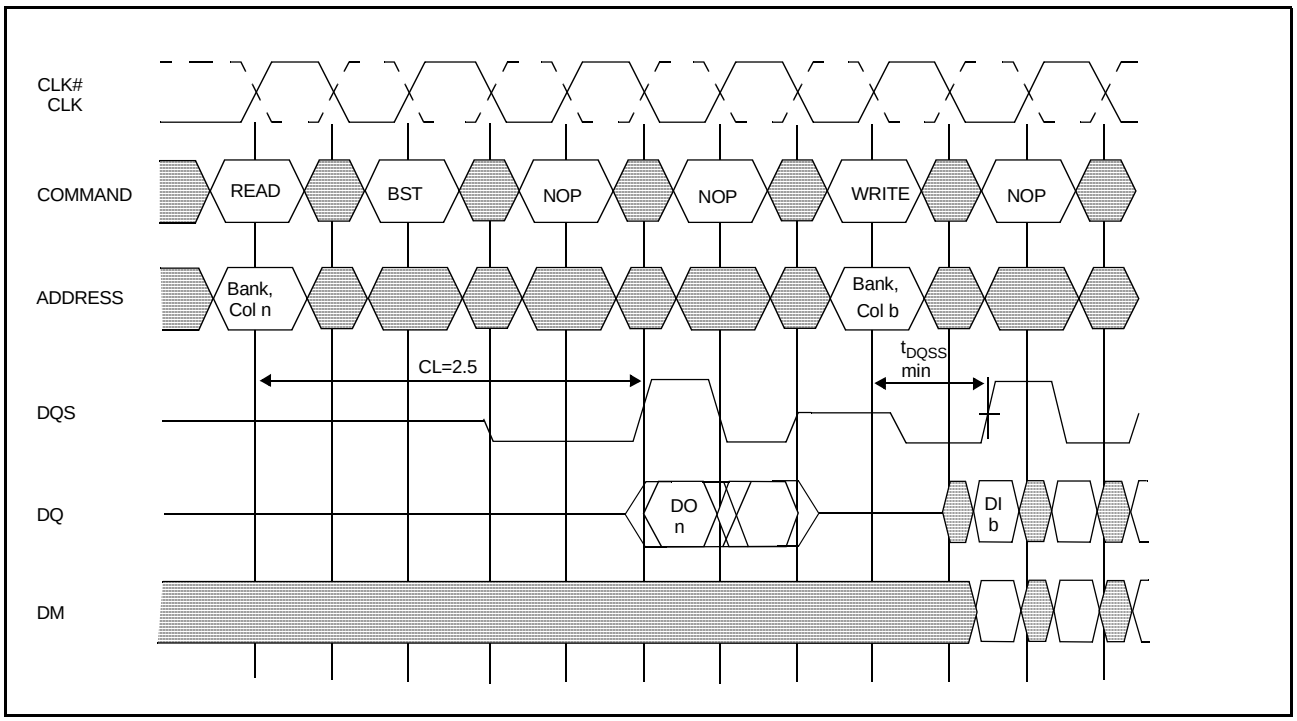


DON'T CARE

DO n=Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

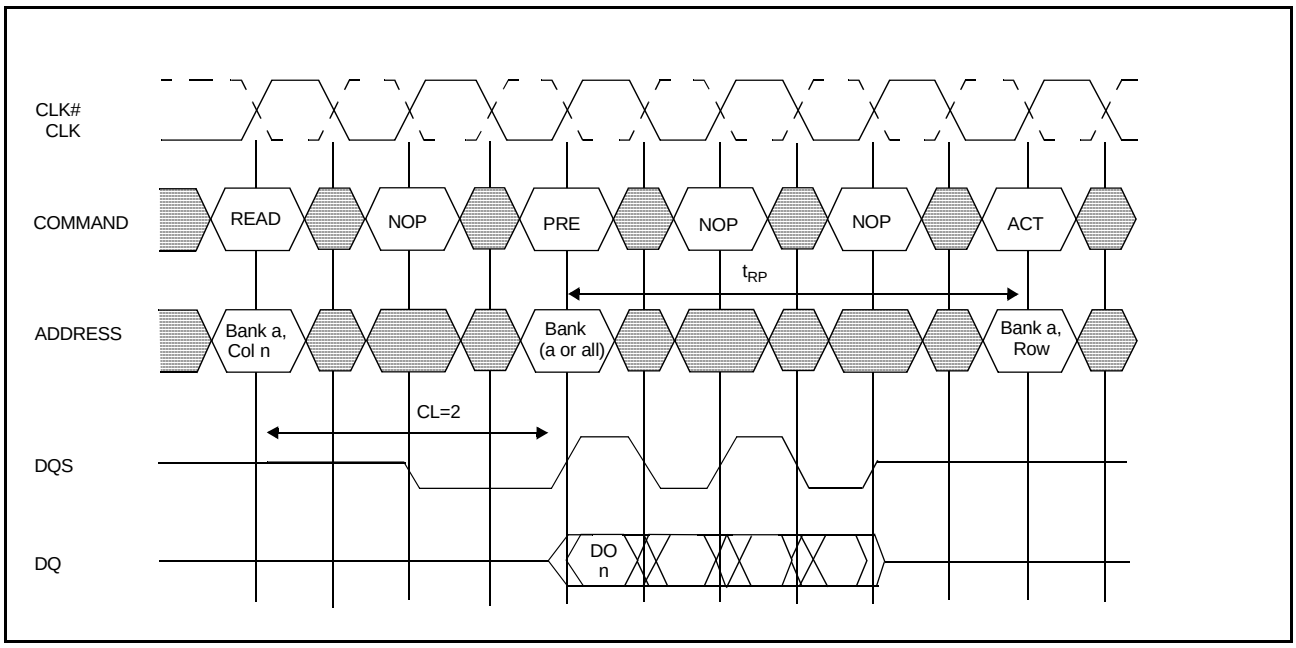
Figure 11
TERMINATING A READ BURST

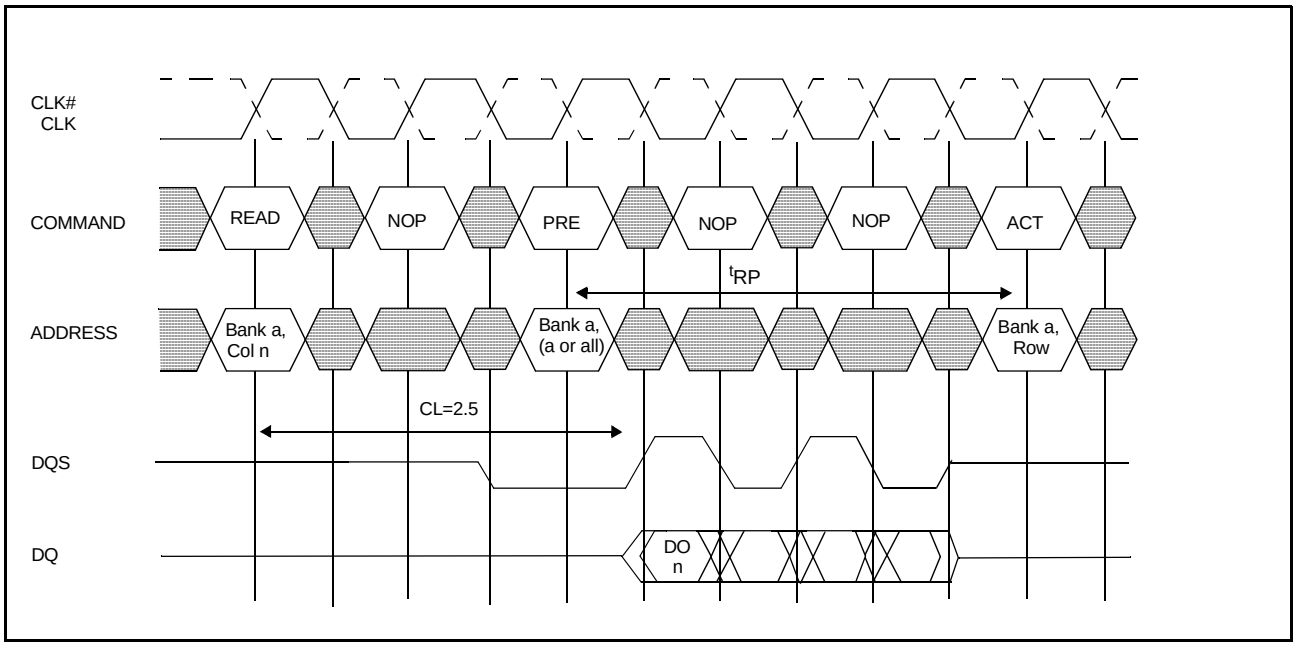




DO n (or b)=Data Out from column n (or column b)
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Figure 12
READ TO WRITE





DON'T CARE

DO n=Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 13
READ TO PRECHARGE

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in figure 14.

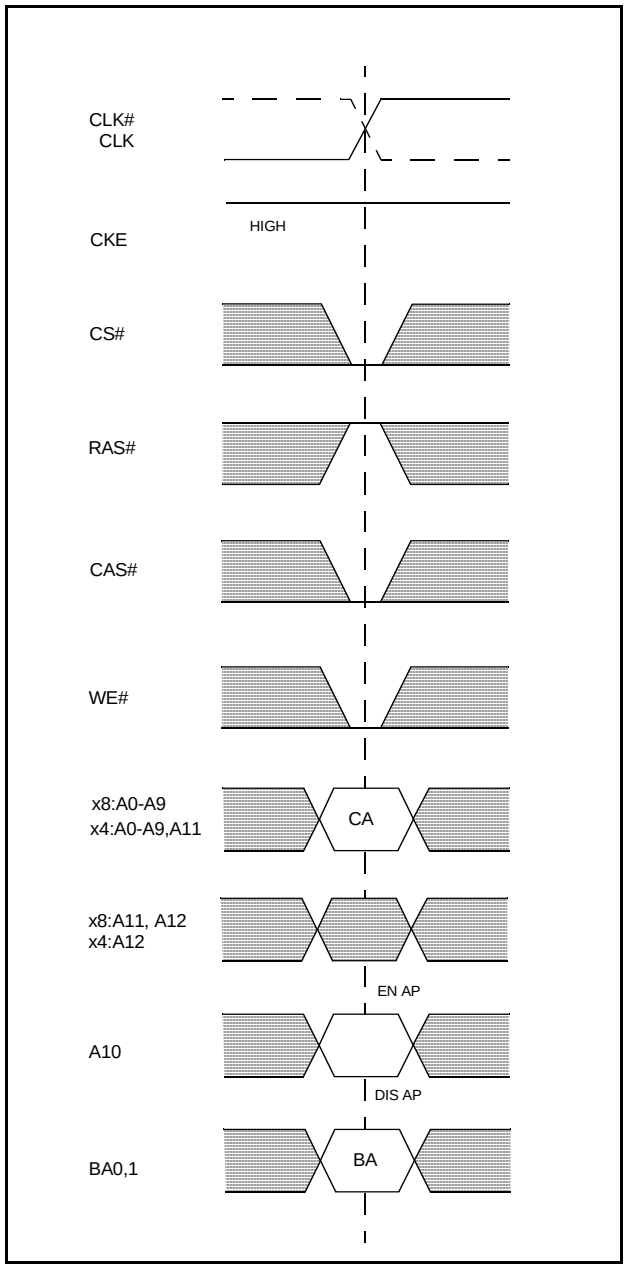
The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTOPRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTOPRECHARGE is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle), so most of the WRITE diagrams that follow are drawn for the two extreme cases (i.e. tDQSS MIN and tDQSS MAX). Figures 15 and 16 show the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figures 17 and 18 show concatenated bursts of 4. An example of non-consecutive WRITEs is shown in Figure 19. Full-speed random write accesses within a page or pages can be performed as shown in Figures 20 and 21.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figures 22 and 23.

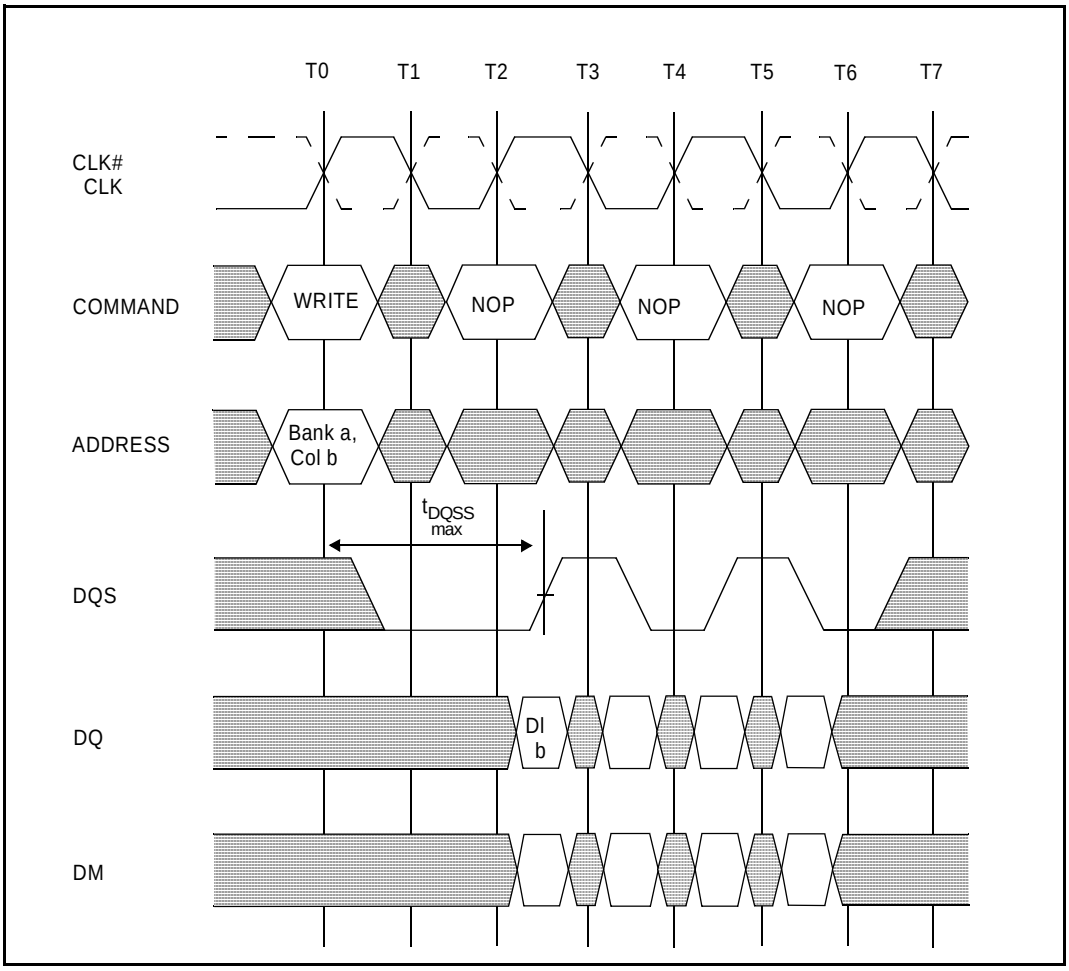
Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 24-27. Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in should be masked with DM (through one-half clock after the READ command).



=DON'T CARE

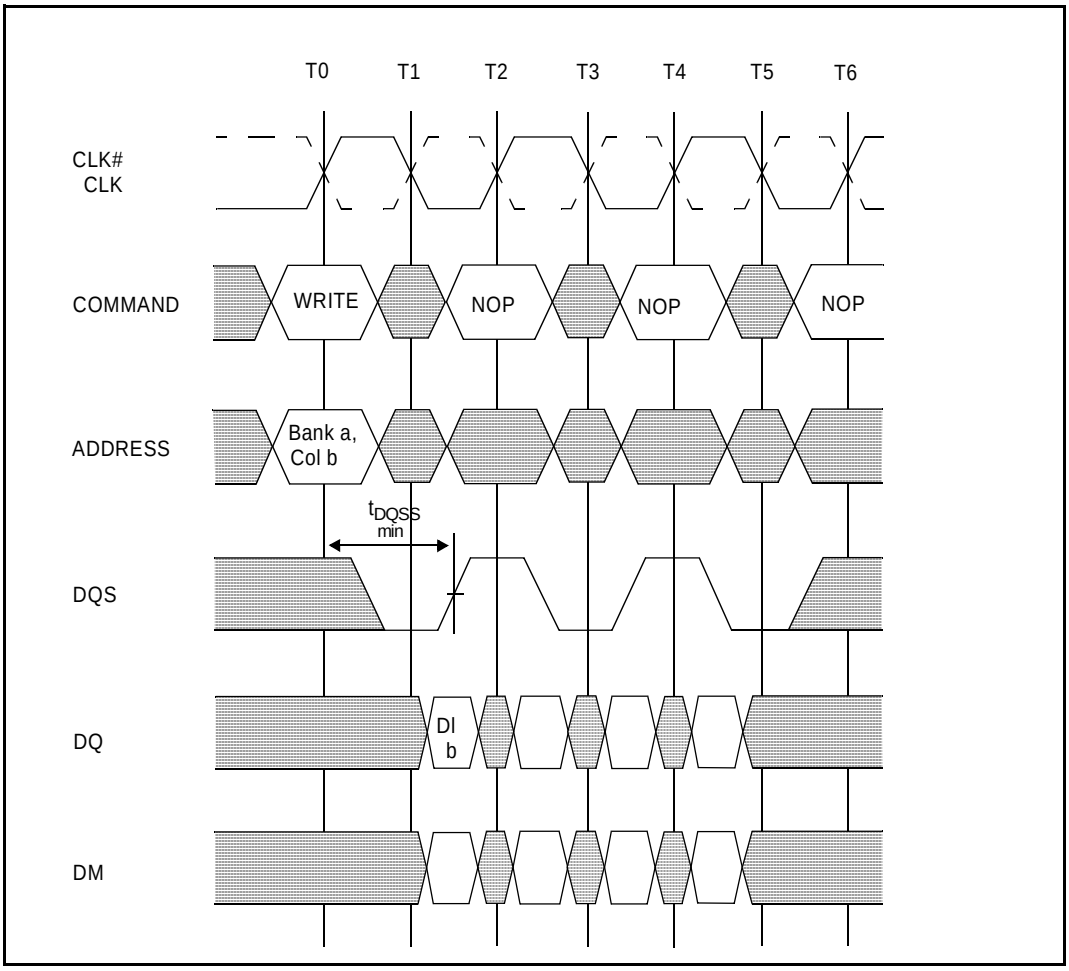
CA = Column Address
BA = Bank Address
EN AP = Enable Autoprecharge
DIS AP = Disable Autoprecharge

Figure 14
WRITE COMMAND



Dl b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following Dl b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 15
WRITE BURST - MAX DQSS



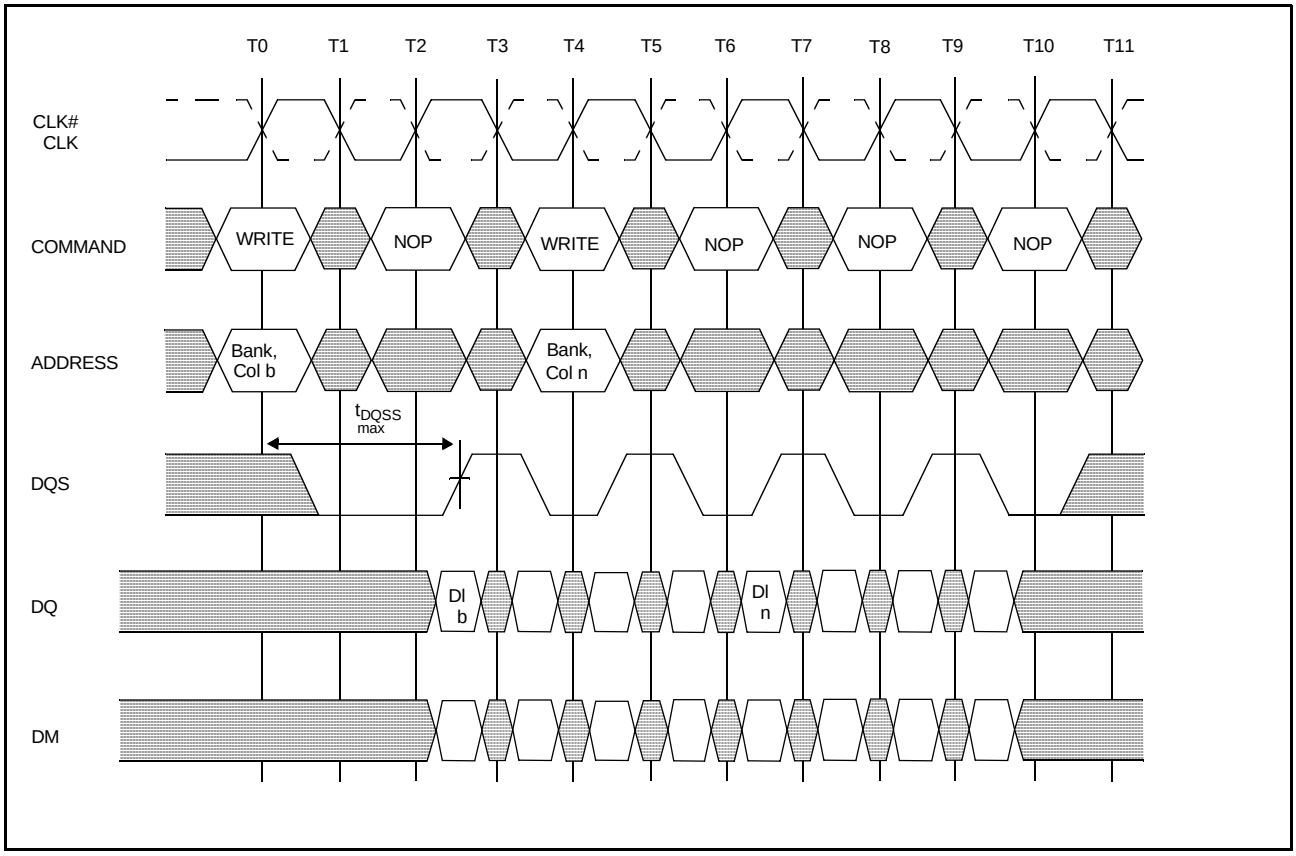
Dl b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following Dl b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 16
WRITE BURST - MIN DQSS

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE with out truncating the write burst, tWR should be met as shown in Figures 28 and 29.

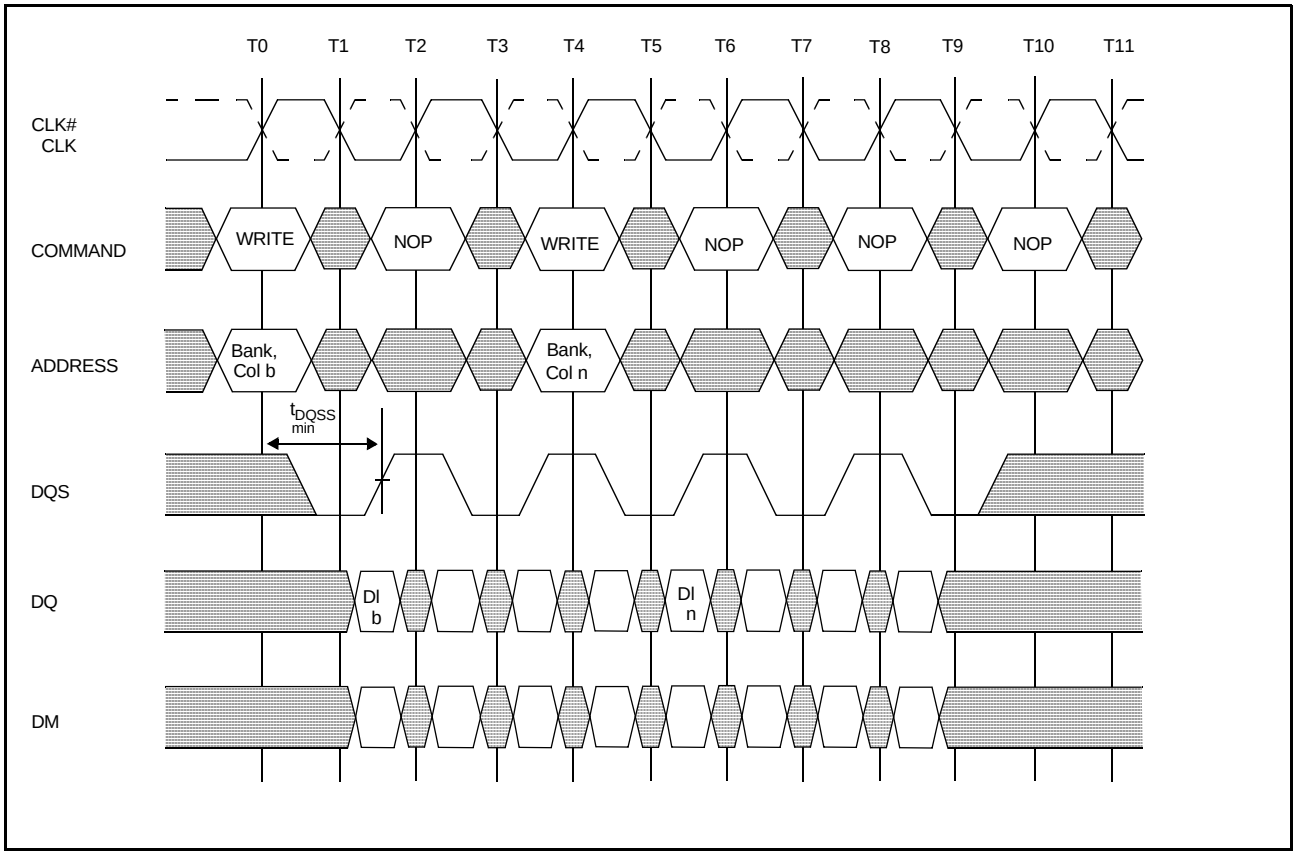
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 30-33. Note that only the data -in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM (through one-half clock after the READ command). Following the PRECHARGE command, a subsequent command to the same bank can not be issued until tRP is met.

In the case of a write burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same burst with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



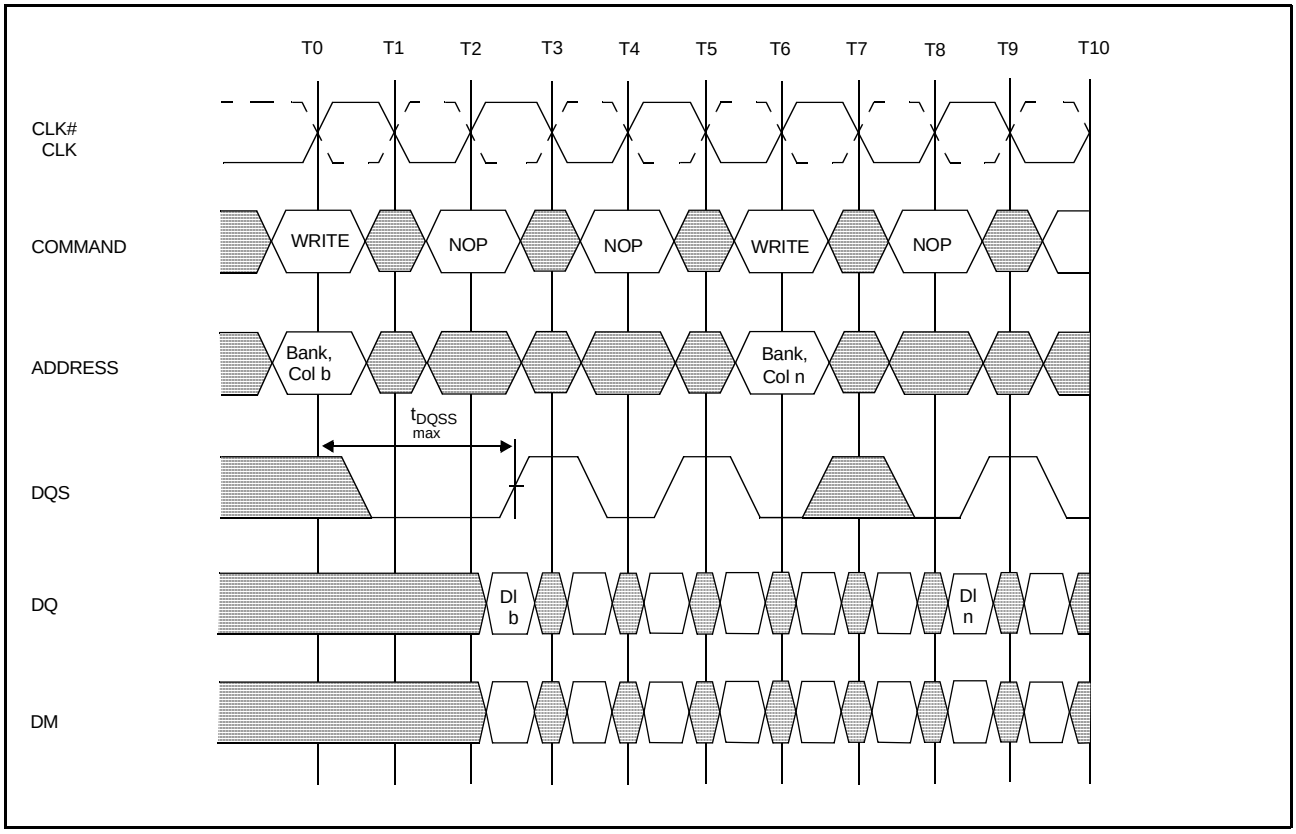
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A non-interrupted burst of 4 is shown
Each Write command may be to any bank

Figure 17
WRITE TO WRITE - MAX DQSS



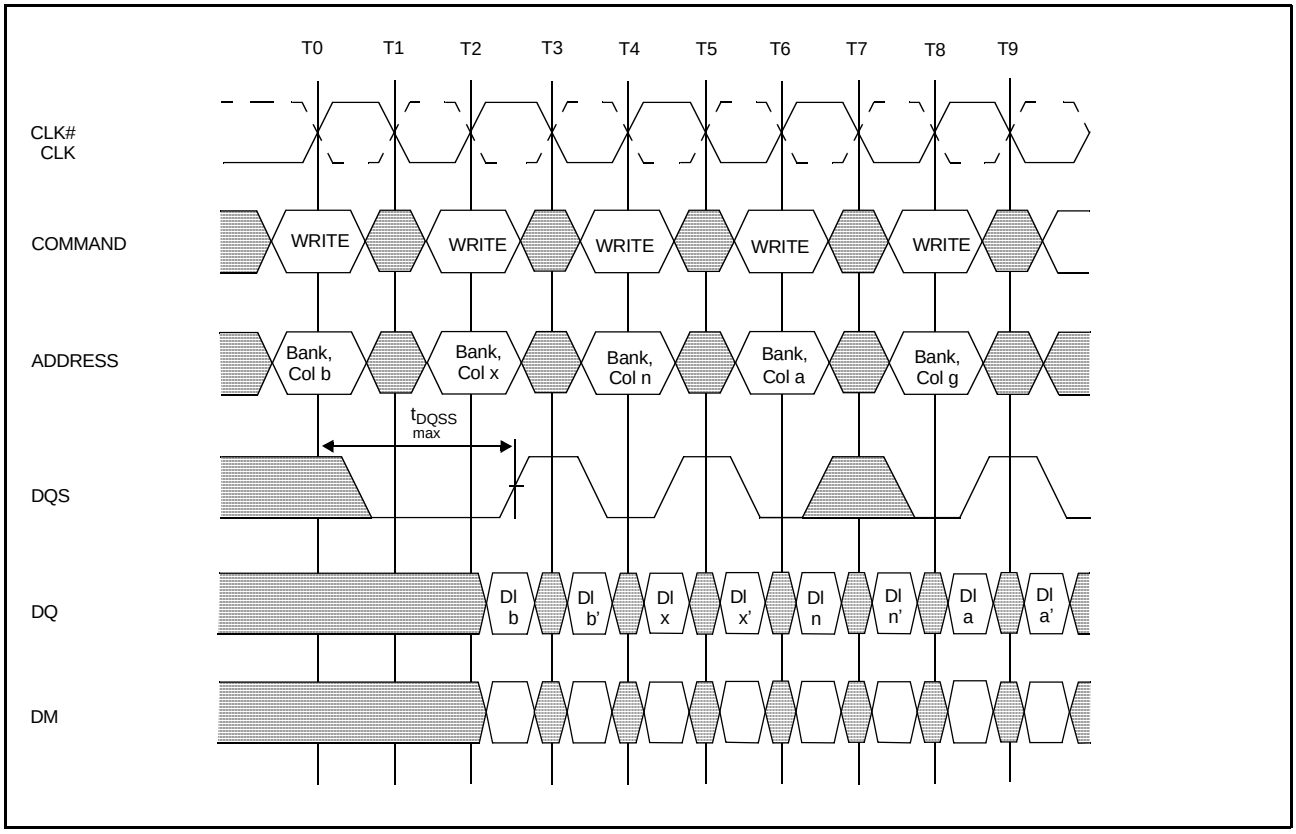
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A non-interrupted burst of 4 is shown
Each Write command may be to any bank

Figure 18
WRITE TO WRITE - MIN DQSS



DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A non-interrupted burst of 4 is shown
Each Write command may be to any bank

Figure 19
WRITE TO WRITE - MAX DQSS, NON-CONSECUTIVE

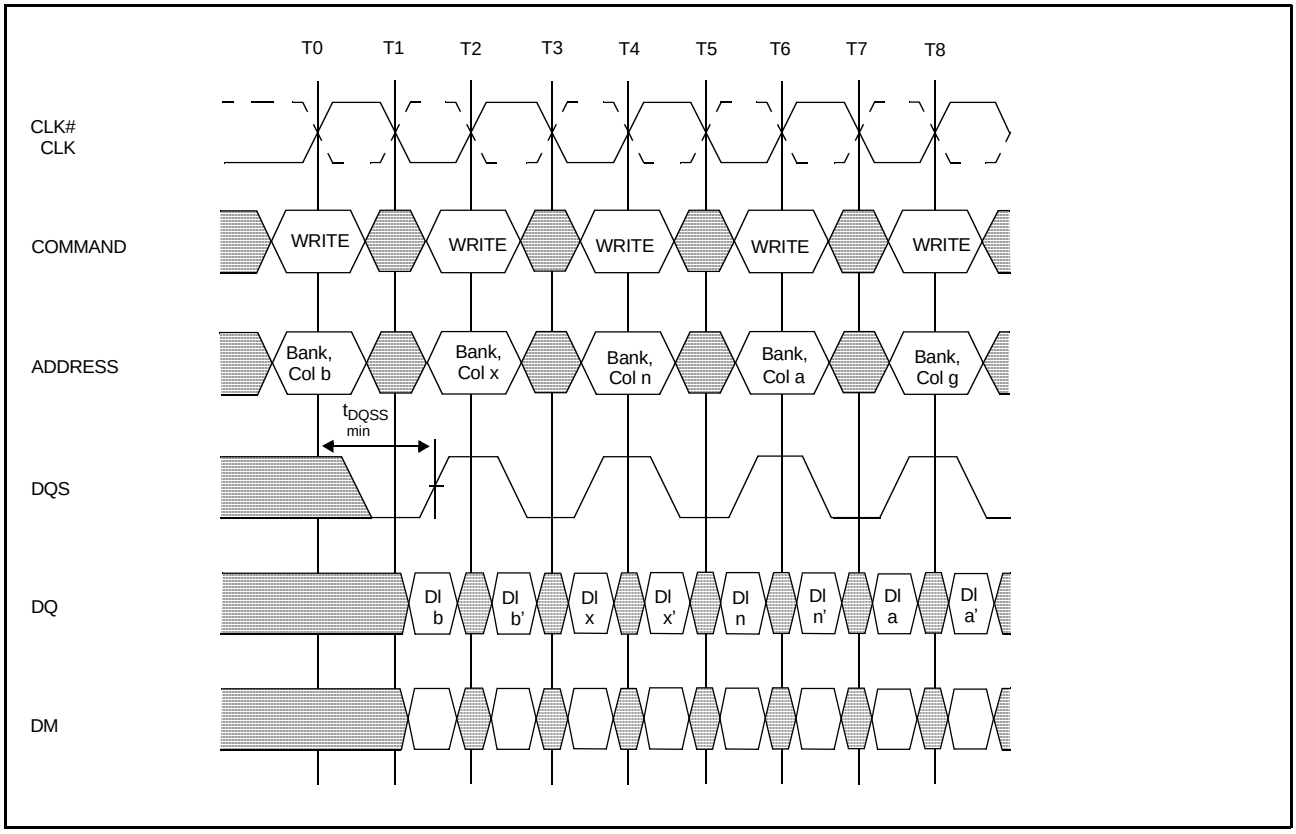


DON'T CARE

UNDEFINED

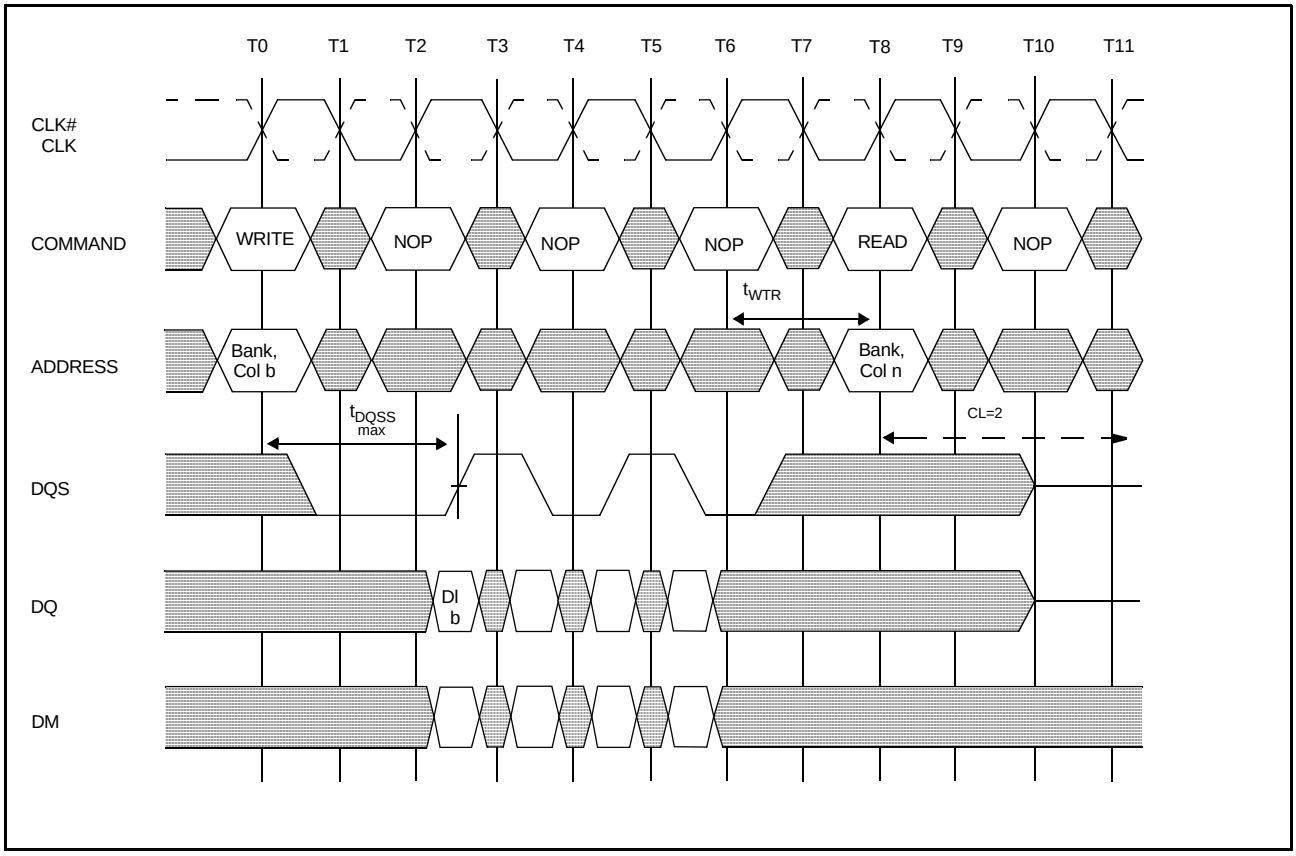
DI b, etc.=Data In for column b, etc.
b',etc.=odd or even complement of b, etc.(i.e. column address LSB inverted)
Programmed burst Length=2,4 or 8 in cases shown
Each Write command may be to any bank.

Figure 20
RANDOM WRITE CYCLES - MAX DQSS



DI b, etc.=Data In for column b, etc.
b',etc.=odd or even complement of b, etc.(i.e. column address LSB inverted)
Programmed burst Length=2,4 or 8 in cases shown
Each Write command may be to any bank.

Figure 21
RANDOM WRITE CYCLES - MIN DQSS

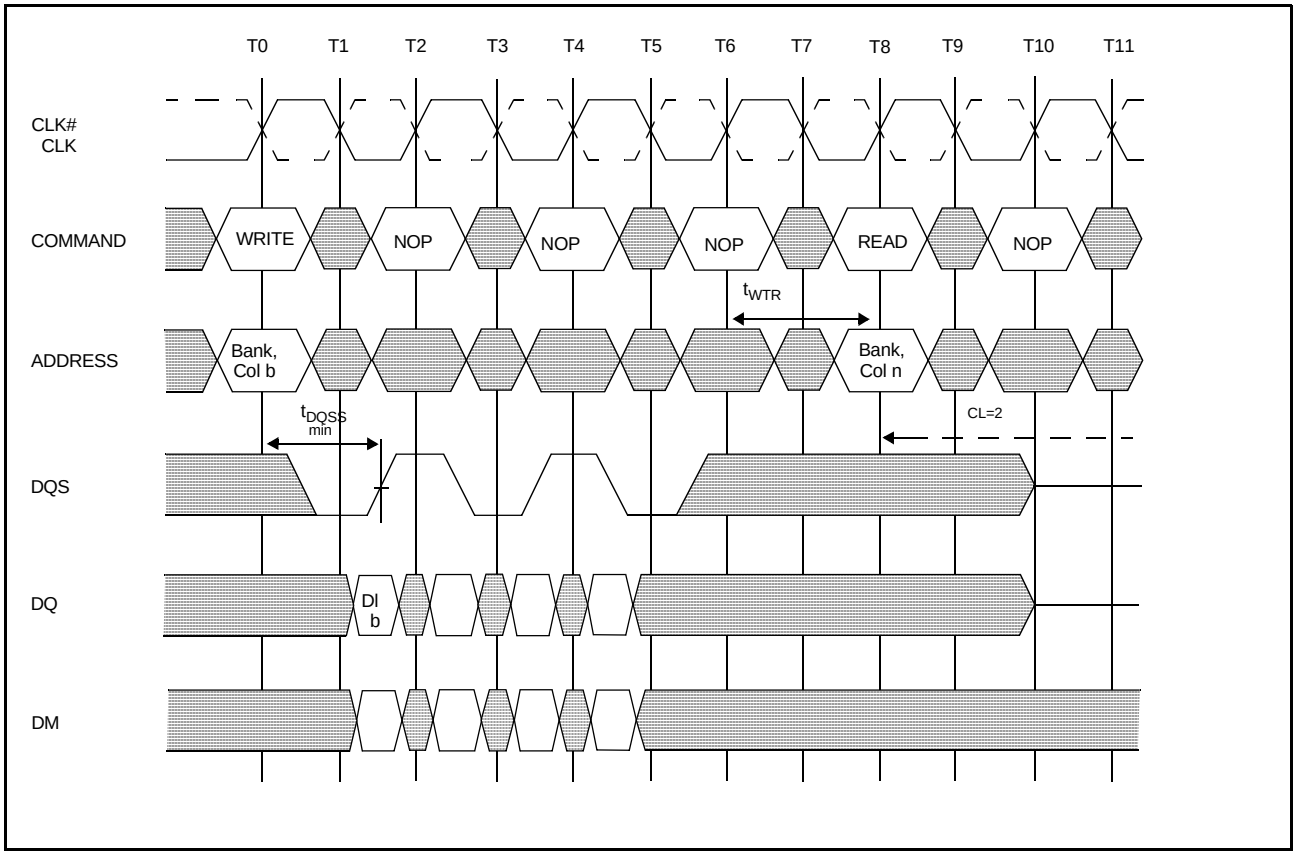


DON'T CARE

UNDEFINED

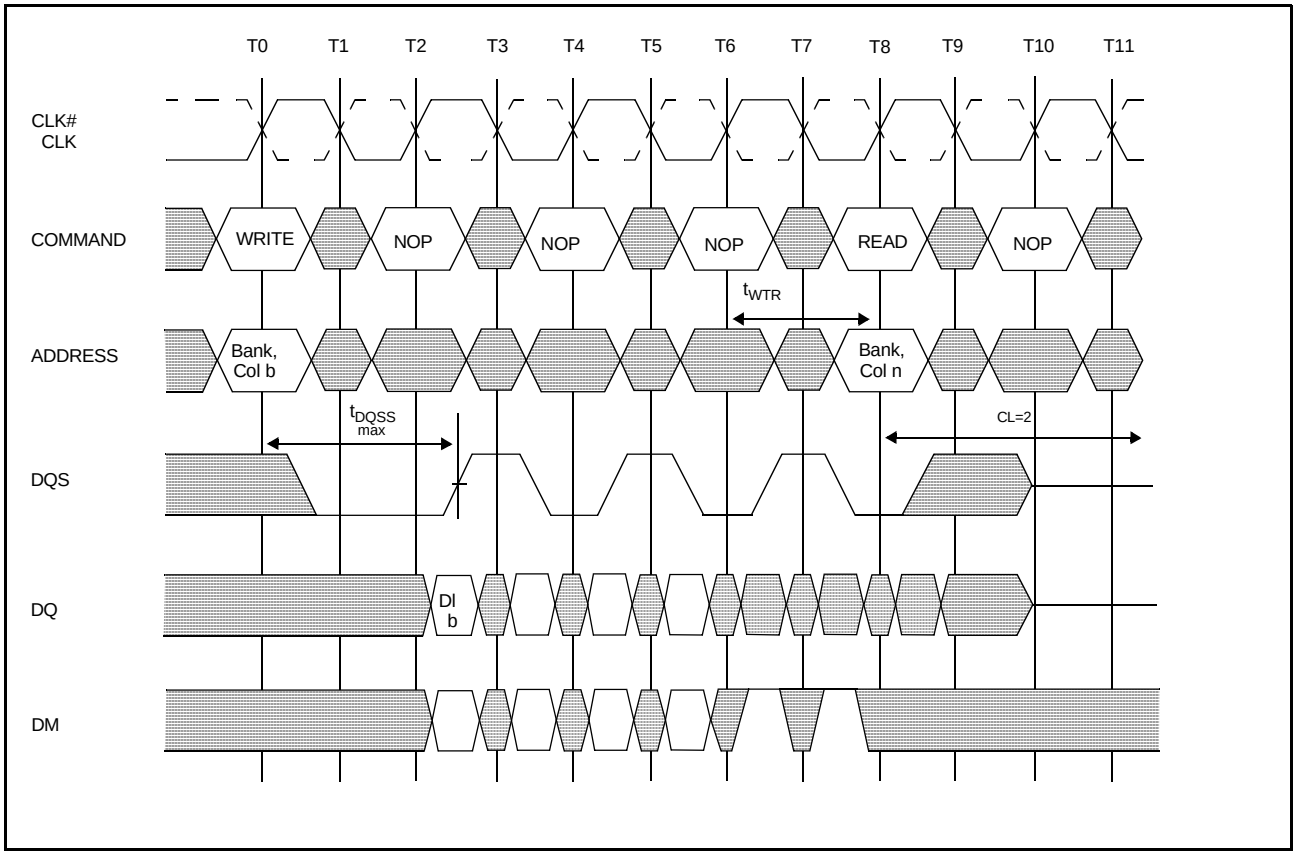
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 22
WRITE TO READ - MAX DQSS, NON-INTERRUPTING



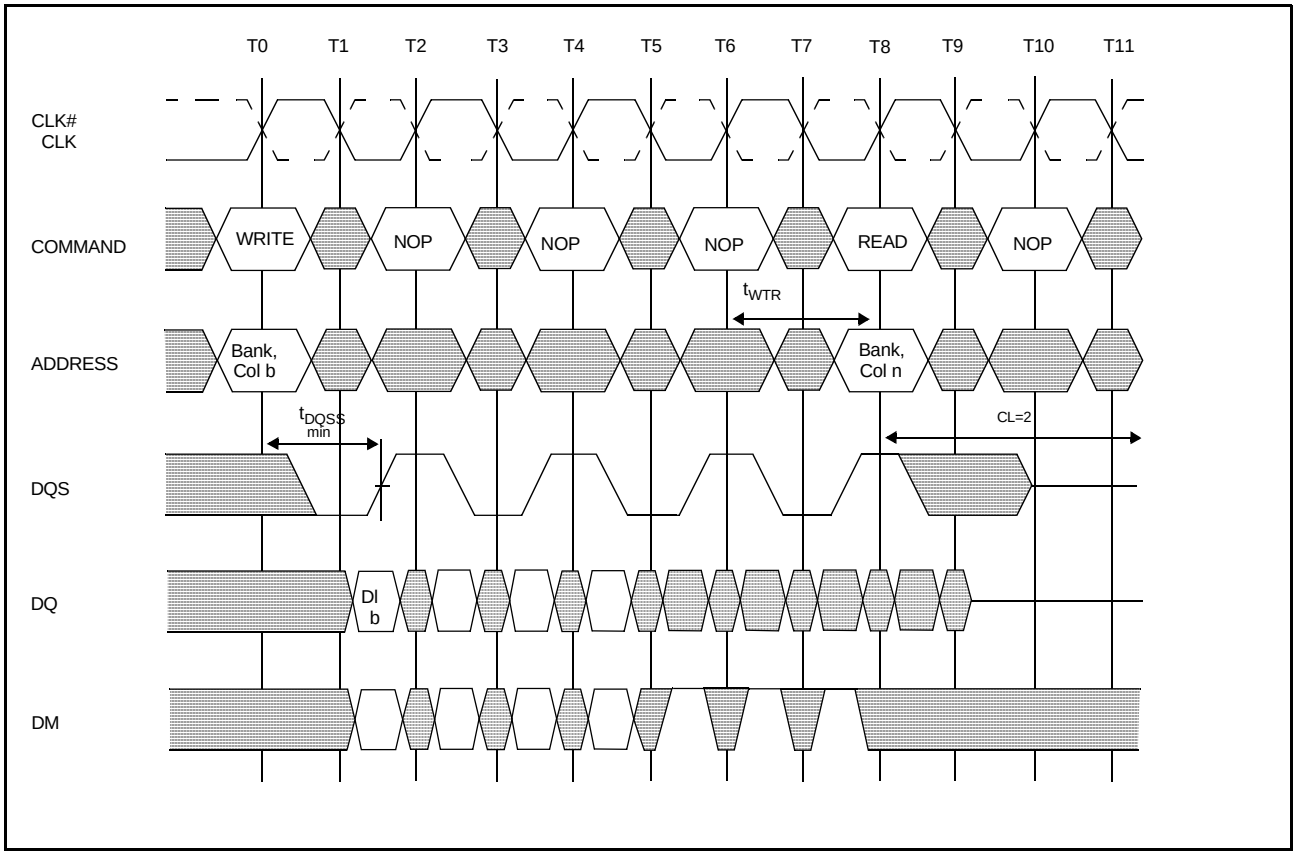
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 23
WRITE TO READ - MIN DQSS, NON-INTERRUPTING



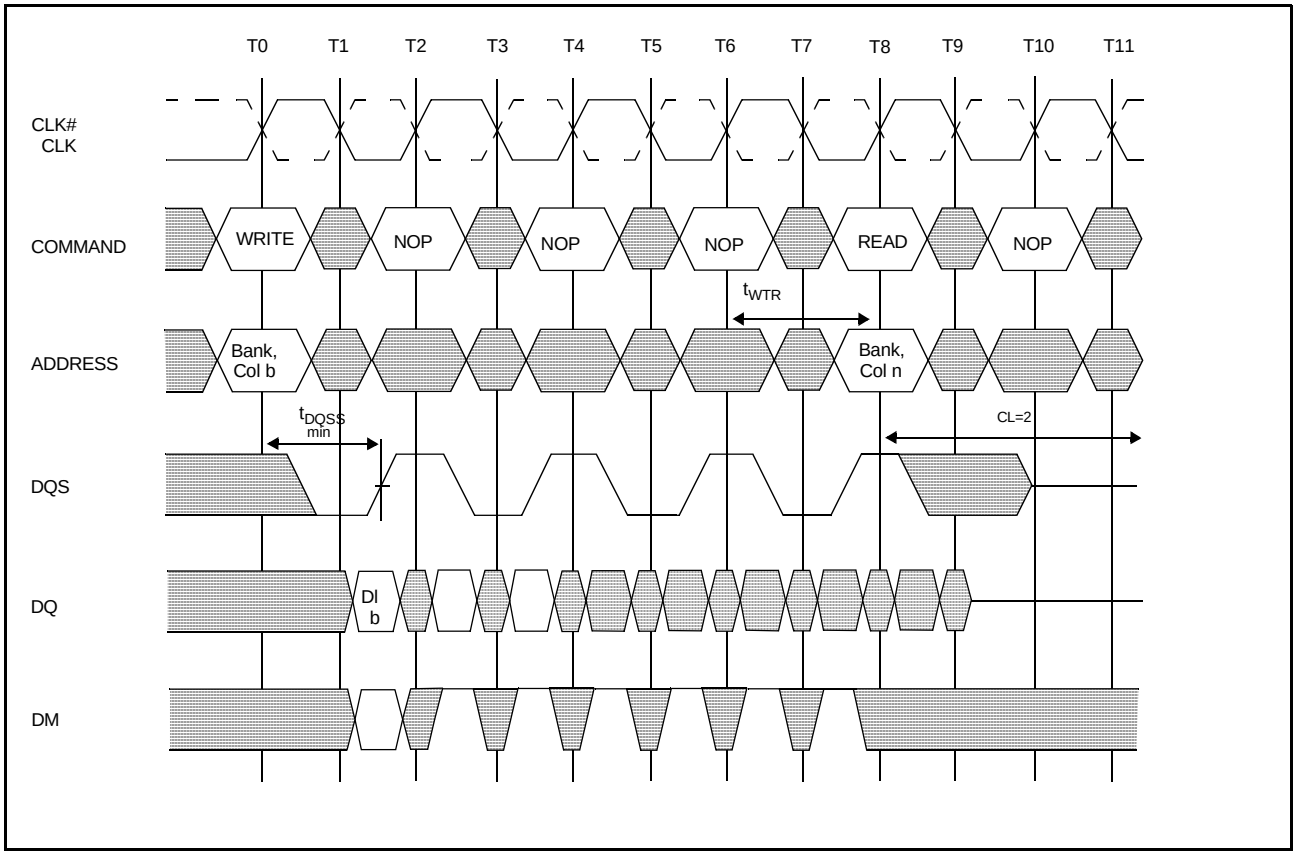
DI b=Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 24
WRITE TO READ - MAX DQSS, INTERRUPTING



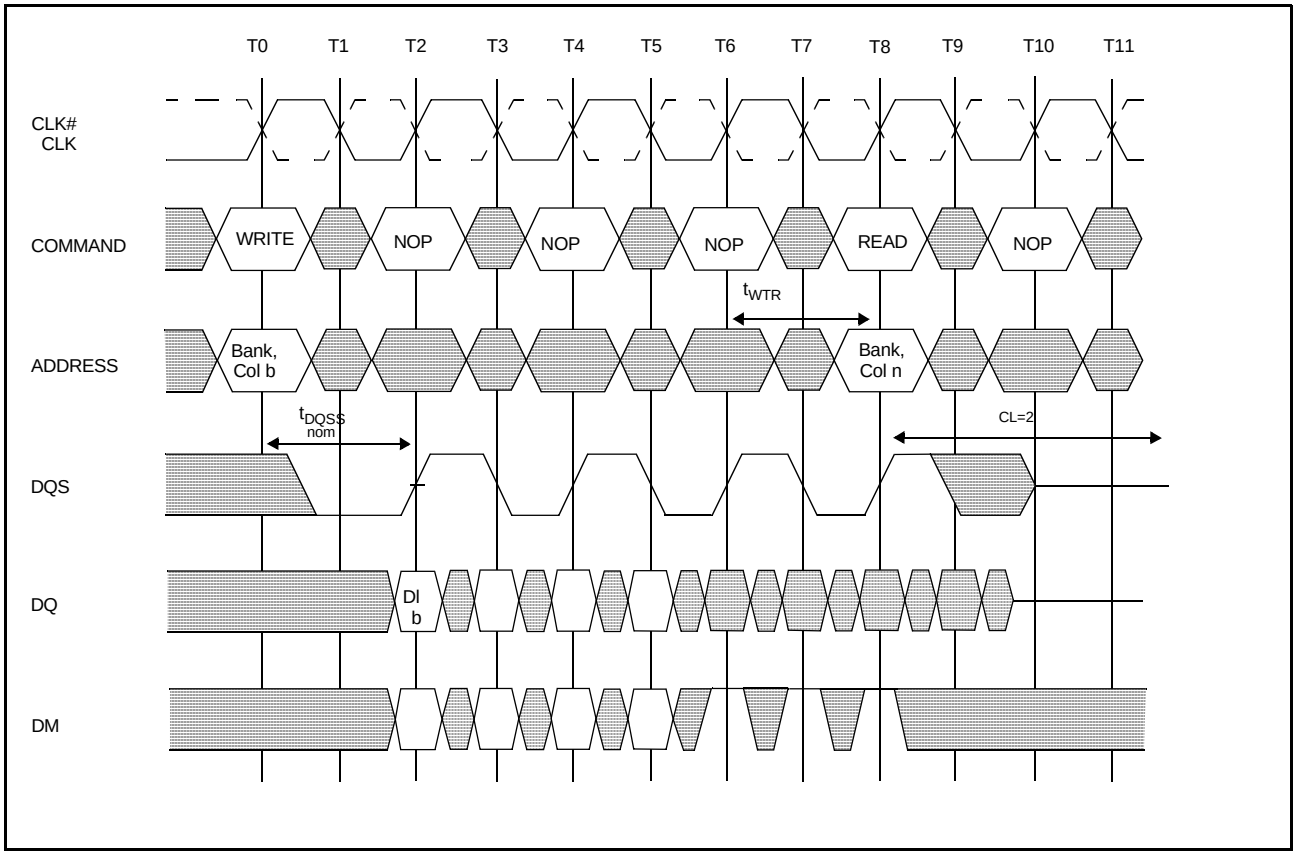
DI b=Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
t_{WTR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 25
WRITE TO READ - MIN DQSS, INTERRUPTING



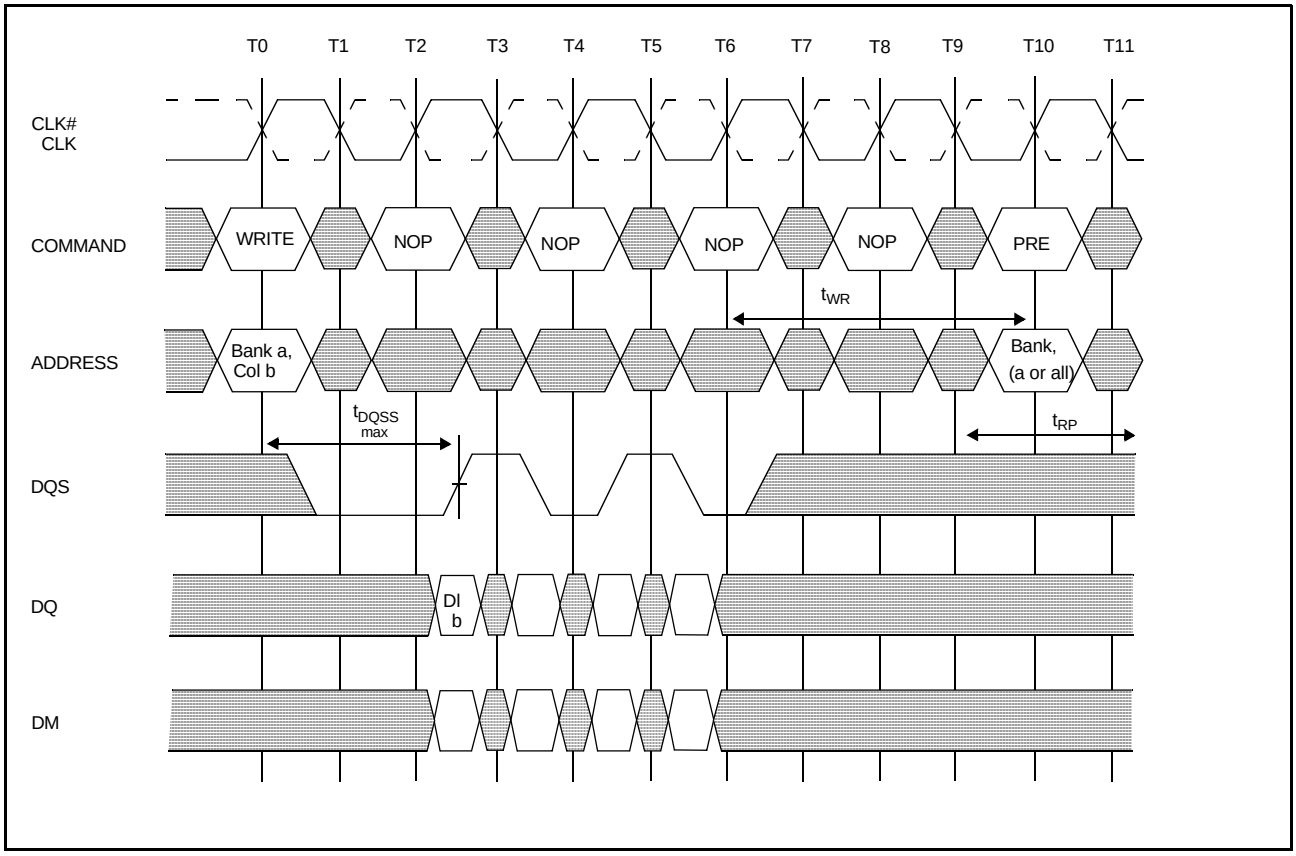
Dl b= Data In for column b
An interrupted burst of 8 is shown, 3 data elements are written
2 subsequent elements of Data In are applied in the programmed order following Dl b
t_{WTR} is referenced from the first positive CLK edge after the last desired Data in pair (not the last desired data in element)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 26
WRITE TO READ - MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



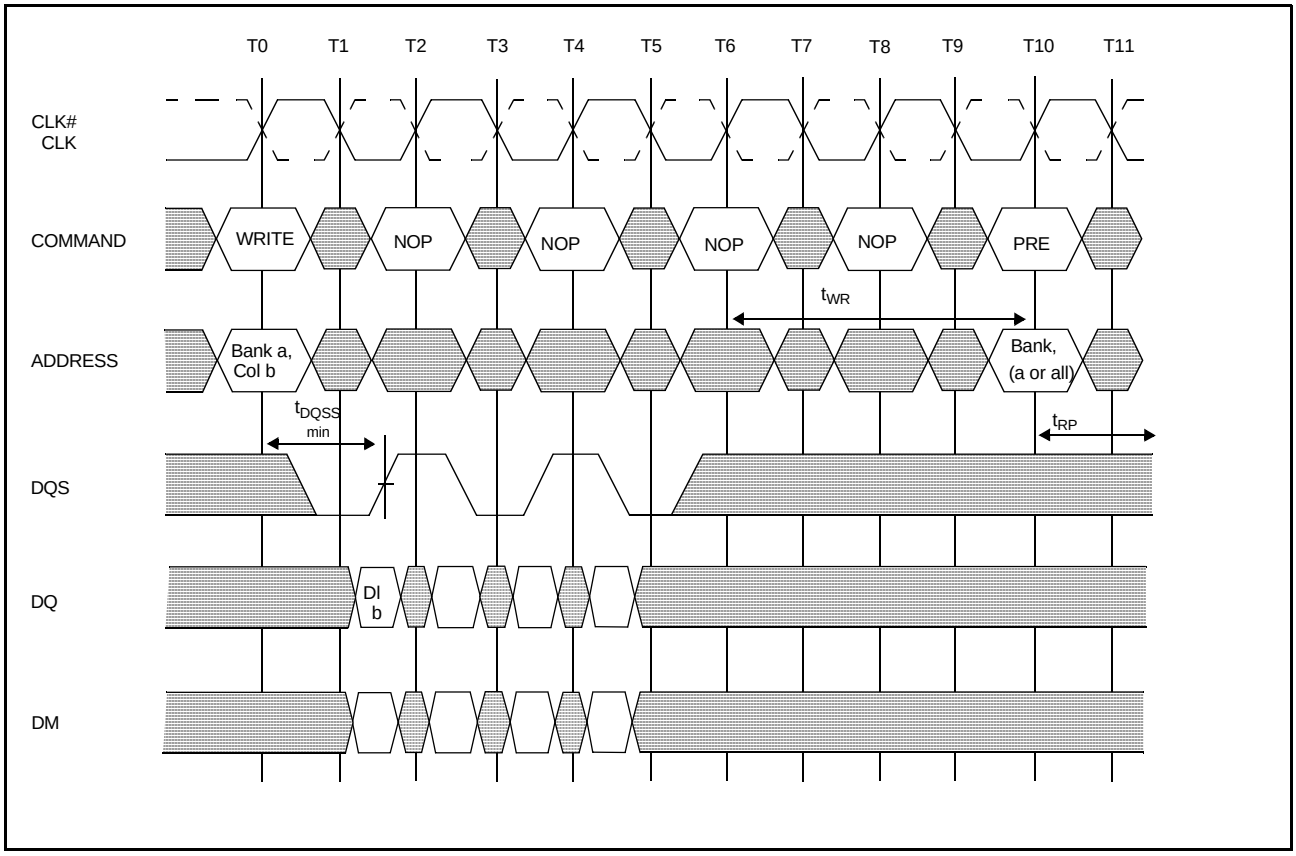
DI b= Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
t_{WTR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 27
WRITE TO READ - NOMINAL DQSS, INTERRUPTING



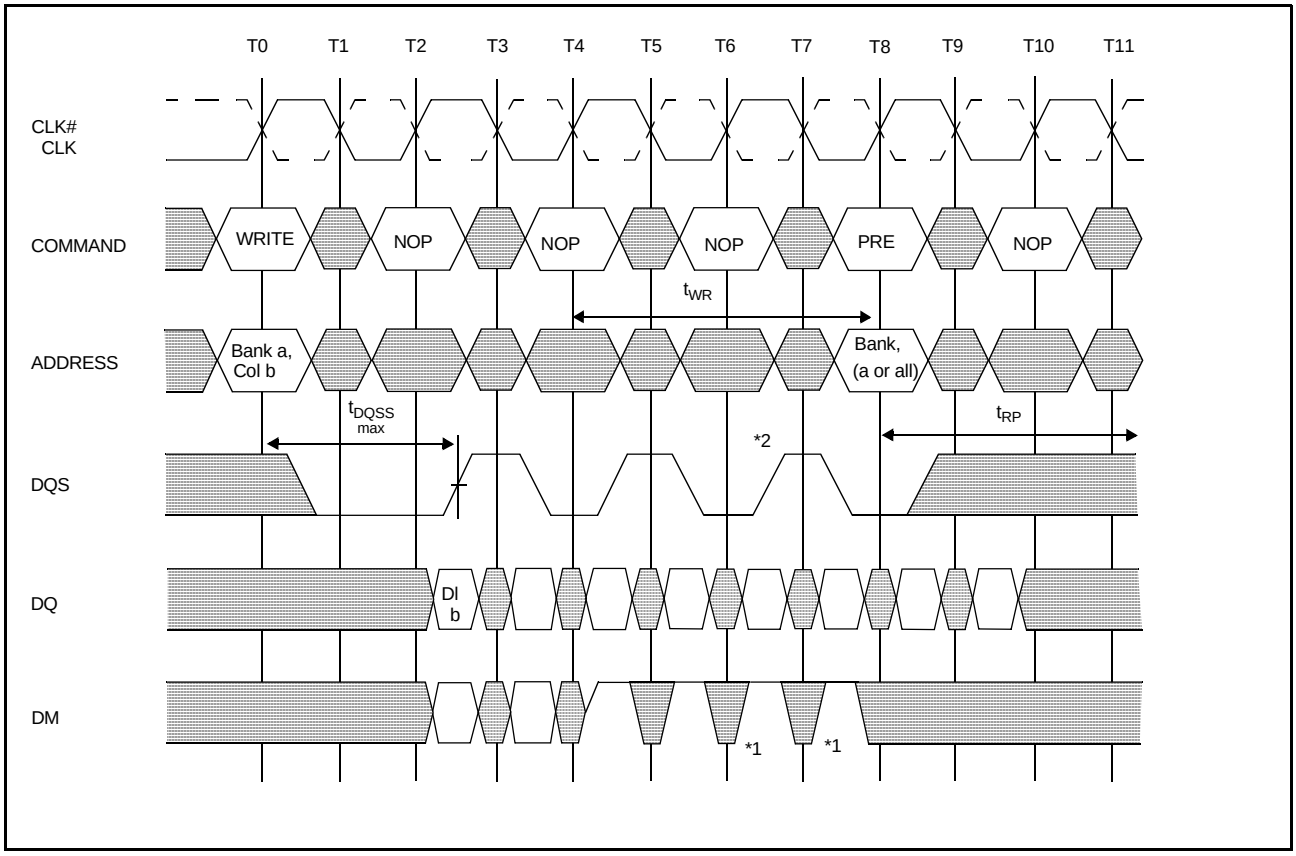
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WTR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 28
WRITE TO PRECHARGE - MAX DQSS, NON-INTERRUPTING



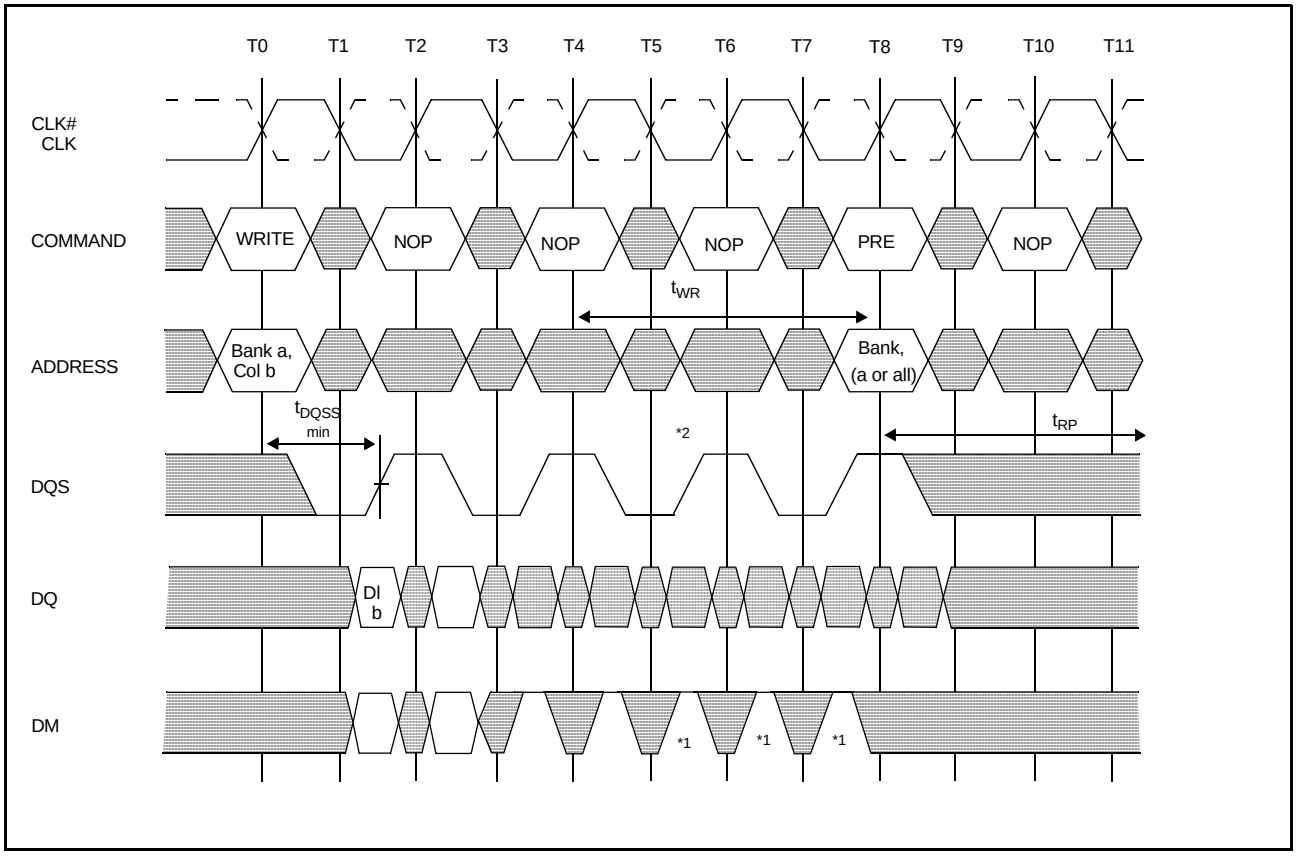
DI b=Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
t_{WR} is referenced from the first positive CLK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 29
WRITE TO PRECHARGE - MIN DQSS, NON-INTERRUPTING



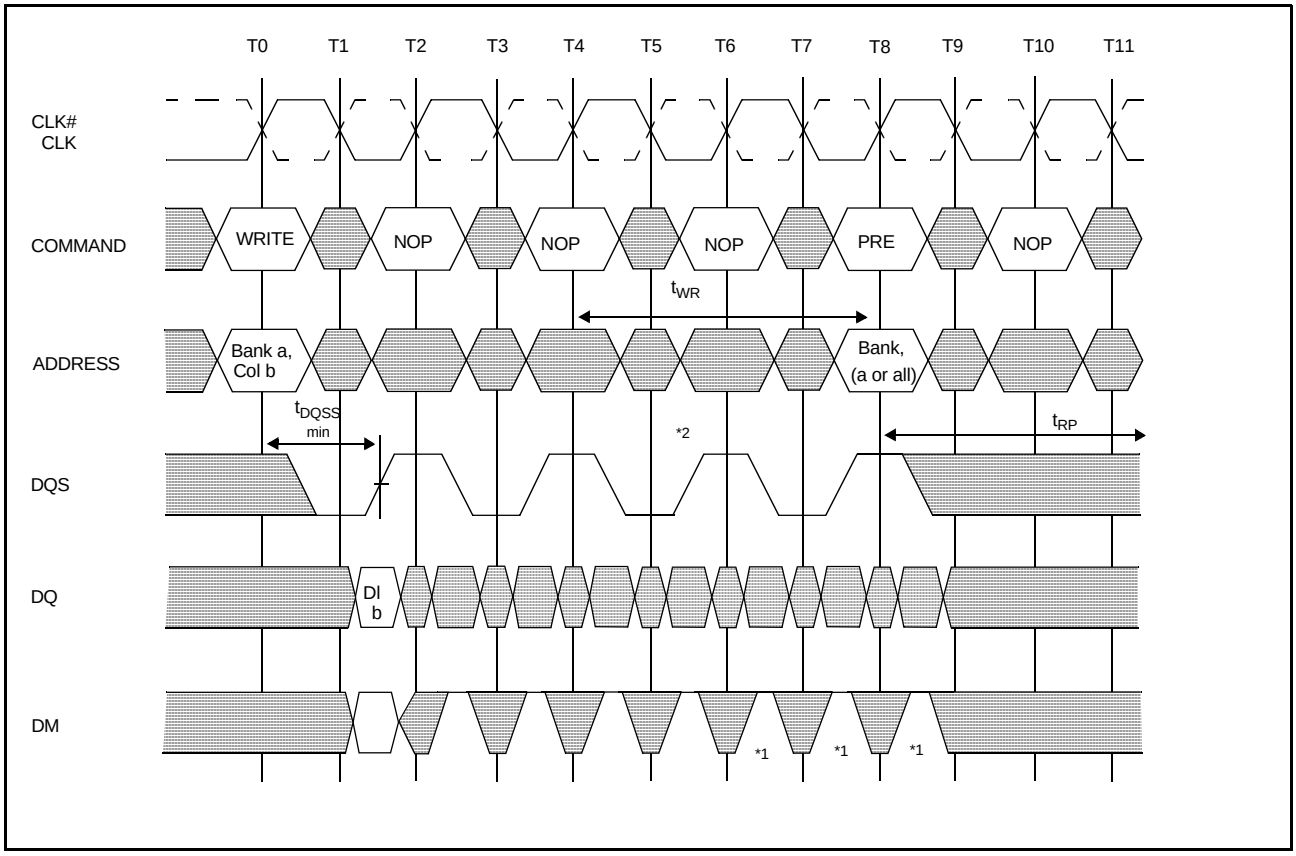
DI b =Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be don't care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes don't care at this point

Figure 30
WRITE TO PRECHARGE - MAX DQSS, INTERRUPTING



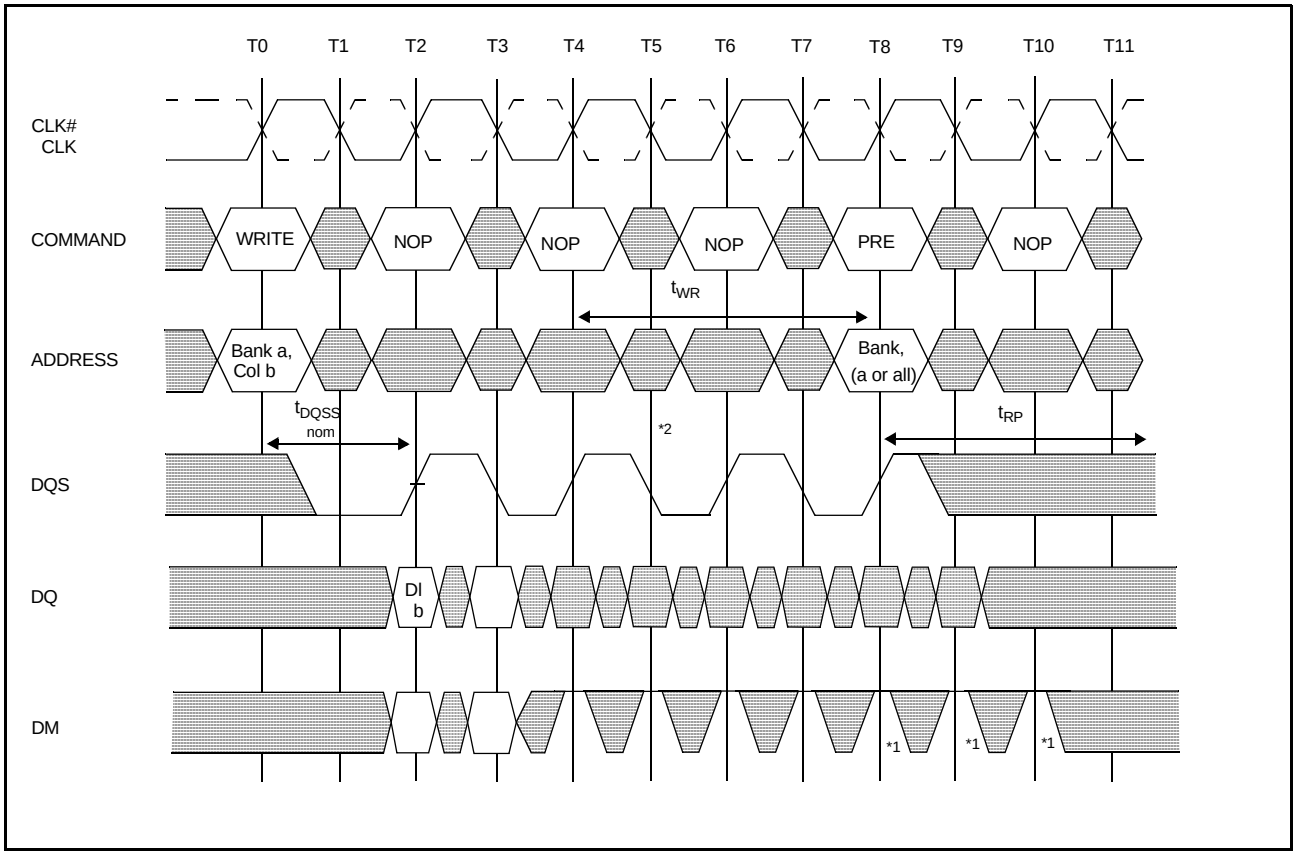
DI b=Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be don't care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes don't care at this point

Figure 31
WRITE TO PRECHARGE - MIN DQSS, INTERRUPTING



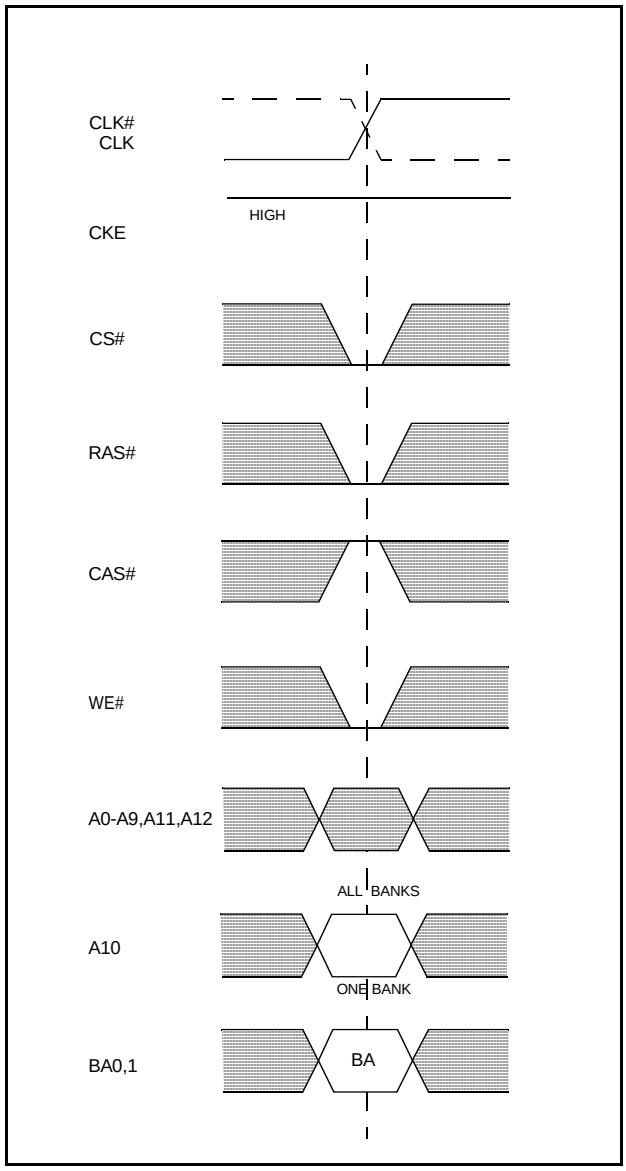
DI b=Data In for column b
An interrupted burst of 4 or 8 is shown, 1 data elements are written
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be don't care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes don't care at this point

Figure 32
WRITE TO PRECHARGE - MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



DI b=Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
t_{WR} is referenced from the first positive CLK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1=can be don't care for programmed burst length of 4
*2=for programmed burst length of 4, DQS becomes don't care at this point

Figure 33
WRITE TO PRECHARGE - NOMINAL DQSS, INTERRUPTING



BA=Bank Address (if A10 LOW, otherwise don't care')

Figure 34
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0,BA1 select the bank. When all banks are to be precharged, inputs BA0,BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power down; if power-down occurs when there is a row active in either bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CLK, CLK# and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering Power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. In either case, CKE LOW and a stable clock signal should be maintained at the inputs of the DDR SDRAM, and all other input signals are “Don’t Care”. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited when CKE is registered HIGH, and a command may be applied be applied one clock cycle later.

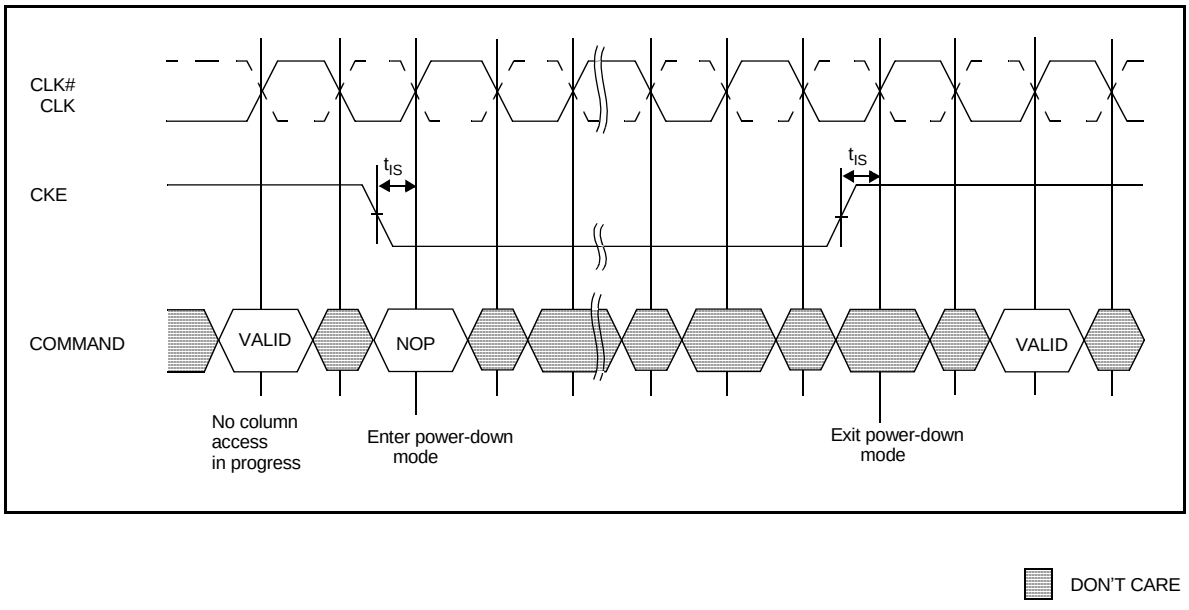


Figure 35
POWER-DOWN

TRUTH TABLE 2-CKE

(Notes: 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMAND_n$	$ACTION_n$	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DSEL or NOP	Exit Power-Down	5
		Self Refresh	DSEL or NOP	Exit Self Refresh	6
H	L	All Banks Idle	DSEL or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DSEL or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFERESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKE_n is the logic state of CKE at clock edge n, CKE_{n-1} was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. $COMMAND_n$ is the command registered at clock edge n, and $ACTION_n$ is result of $COMMAND_{n-}$

4. All states and sequences not shown are illegal or reserved.

5.Exiting power-down at clock edge n will put the device in the “all banks idle” state in time for clock edge n+1

6. Exiting self refresh at clock edge n will put the device in the “all banks idle” state once ^tXNR or ^tXRD is met. DSEL or NOP commands should be issued on any clock edges occurring during the ^tXNR or ^tXRD period. A minimum of two NOP commands must be provided during ^tXNR or ^tXRD period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3-Current State Bank n - Command to Bank n

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS #	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	COMMAND INHBIT (NOP/continue previous operation	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	L	H	L	PRECHARGE (truncate READ burst, start PRE-CHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRE-CHARGE)	8, 11

NOTE:

1. This table applies when CKEn-1 was HIGH and CKEn Is HIGH (see Truth Table 2) and after tXNR or tXRD has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state, Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/ accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank, DSEL or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.

   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write w/Auto Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DSEL or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFERESH command and ends when ^{t}RC is met. Once ^{t}RC is met, the DDR SDRAM will be in the "all banks idle" state.

   Accessing Mode

   Register: Starts with registration of a MODE REGISTER SET command and ends when ^{t}MRS has been met. Once ^{t}MRS is met, the DDR SDRAM will be in the "all banks idle" state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; required that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.

TRUTH TABLE 4-Current State Bank n - Command to Bank m

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS #	CAS #	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	COMMAND INHBIT (NOP/continue previous operation	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Read Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	3, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	3, 7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKE_{n-1} was HIGH and CKE_n Is HIGH (see Truth Table 2) and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions:

Idle: The bank has been precharged, and ^{t}RP has been met.

Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

Read with Auto Precharge Enabled: See following text, note 3a, 3b and 3c

Write with Auto Precharge Enabled: See following text, note 3a, 3b and 3c

3a. For devices which do not support the optional concurrent auto precharge feature, the read with auto precharge enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. The precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins.
During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g. following a Read with Auto Precharge by a Write command to another bank is subject to the same data path limitations as when following a Read by a Write).

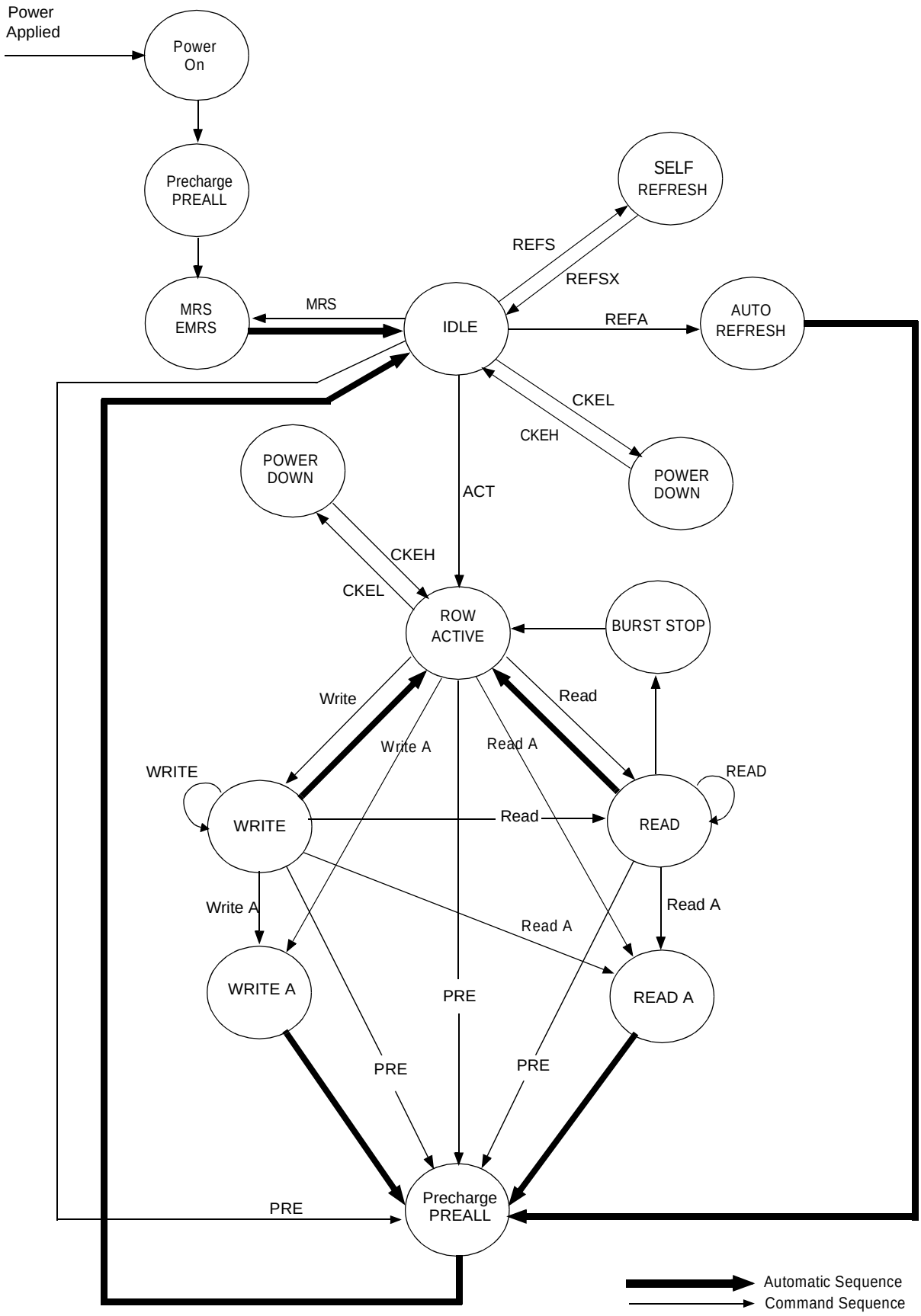
3b. For devices whlich do support the optional concurrent auto precgarge feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRETE data must be avoided.)

3c. The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below, for both cases of concurrent auto precharge supported or

Form command	To command (different bank, non-interrupting command)	Minimu m delay, without concurrent AP support	Minimum delay, with concurrent AP support	Units
Write w/AP	Read or Read w/AP	1 + (BL/2) + (tWR/tCK) (rounded up)	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	1 + (BL/2) + (tWSR/tCK) (rounded up)	BL/2	tCK
	Precharge or Activate	1		tCK
Read w/AP	Read or Read w/AP	BL/2		tCK
	Write or Write w/AP	CL(rounded up) + (BL/2)		tCK
	Precharge or Activate	1		tCK

4. AUTO REFERESH, MODE REGISTER SET and PRECHARGE ALL commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output.

Simplified state Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to Vss	V_{DD}	-0.5 ~ 3.7	V
Voltage on VDDQ relative to Vss	V_{DDQ}	-0.5 ~ 3.7	V
Voltage on input pin relative to Vss	V_{IN}	-0.5 ~ V_{DD}+0.5V	V
Voltage on I/O pin relative to Vss	$V_{I/O}$	-0.5 ~ V_{DDQ}+0.5	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation (Ta=25°C)	P_D	1.0	W
Operating temperature (ambient)	T_{OPT}	0 ~ 70	°C
Storage temperature (plastic)	PRE	-65 ~ 150	°C

Recommended DC Operating Conditions (Ta=0~70°C, unless otherwised noted)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	2.3	2.5	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	1.25V	0.51 x V_{DDQ}	V	5
I/O Termination Voltage (system)	V_{TT}	V_{REF}-0.04	VREF	V_{REF}+0.04	V	6
Input high Voltage, all inputs	$V_{IH(DC)}$	V_{REF}+0.18	-	V_{DDQ}+0.3	V	
Input Low voltage, all inputs	$V_{IL(DC)}$	-0.3	-	V_{REF}-0.18	V	
Input Voltage Level, CLK and CLK# inputs	$V_{IN(DC)}$	-0.3	-	V_{DDQ}+0.3	V	
Input Differential Voltage, CLK and CLK# inputs	$V_{ID(DC)}$	0.36	-	V_{DDQ}+0.6	V	7

Capacitance

(Ta=0~70°C, V_{DD}=V_{DDQ}=2.5 ± 0.2V, V_{SS}=V_{SSQ}=0V, f=100MHz, unless otherwised noted)

Parameter	Symbol	Min	Max	Delta Cap (Max)	Unit	NOTES
Input capacitance: CLK, CLK#	C_{11}	2	3	0.25	pF	11
Input capacitance (all input pins except data pins)	C_{12}	2	3	0.5	pF	11
Data input/output capacitance: DQs, DQS, DM	$C_{I/O}$	4.0	5.0	0.5	pF	11

Recommended Electrical Characteristic and D.C. Operating Conditions

(V_{DD}=V_{DDQ}= 2.5V ± 0.2V, V_{SS}=V_{SSQ}=0V, Output Open, Ta=0~70°C, unless otherwised noted)

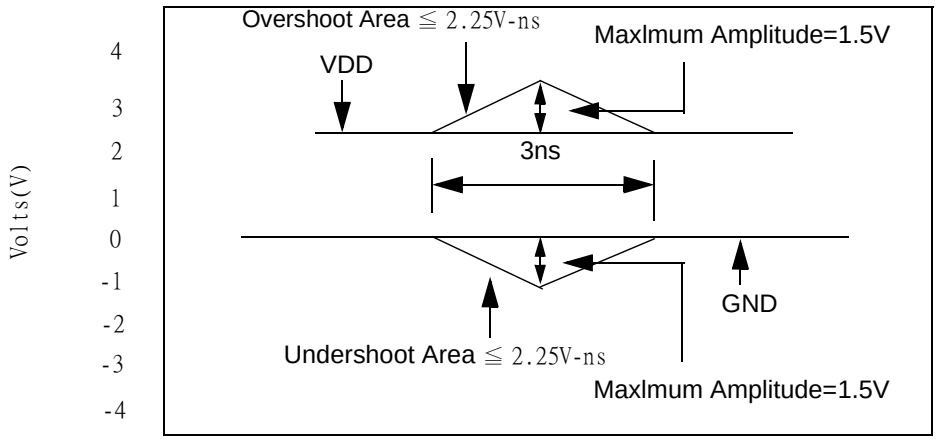
Description/test condition	Symbol	Max				Unit	Notes
		-66	-7L	-75	-8		
OPERATING CURRENT : One Bank ; Active-Precharge ; tRC=tRC MIN ; tCK=tCK MIN ; DQ, DM and DQS inputs changing twice per clock cycle ; address and control inputs changing once per clock cycle	ICC0	115	110	110	105	mA	
OPERATING CURRENT : One Bank ; Active-Read-Precharge ; Burst=2 ; tRC=tRC MIN ; tCK=tCK MIN ; Iout=0mA ; address and control inputs changing once per clock cycle	ICC1	120	115	115	110		
PRECHANGE POWER DOWN STANDY CURRENT : All banks idle ; power down mode ; CKE<= VIL(MAX) ; tCK=tCK MIN	ICC2P	20	20	20	15		
IDLE STANDBY CURRENT : /CS >= VIH(MIN) ; All banks idle ; CKE>= VIH(MIN) ; tCK=tCK MIN ; address and control inputs changing once per clock cycle	ICC2F	30	30	30	30		
ACTIVE POWER DOWN STANDBY CURRENT : One bank active ; power down mode ; CKE<= VIL(MAX) ; tCK=tCK MIN	ICC3P	30	30	30	25		
ACTIVE STANDBY CURRENT : /CS > =VIH(MIN) ; CKE>= VIH(MIN) ; One bank ; Active-Precharge ; tRC=tRAS MAX ; tCK=tCK MIN ; DQ, DM, and DQS inputs changing twice per clock cycle ; address and other control inputs changing once per clock cycle	ICC3N	60	60	60	55		
OPERATING CURRENT : Burst=2 ; Reads ; Continuous burst ; One bank active ; Address and control inputs changing once per clock cycle ; tCK=tCK MIN ; Iout=0mA	ICC4R	170	165	165	155		
OPERATING CURRENT : Burst=2 ; Writes ; Continuous burst ; One bank active ; Address and control inputs changing once per clock cycle ; tCK=tCK MIN ; DQ, DM, and DQS inputs changing twice per clock cycle	ICC4W	145	140	140	135		
AUTO REFRESH CURRENT : tRC=tRFC (MIN)	ICC5	190	185	185	175		
SELF REFRESH CURRENT: CKE<=0.2V	ICC6	3	3	3	3		
Random Read Current : 4 banks active read with activate every 20ns, AP (Auto Precharge) read every 20ns, BL =4, tRCD =3, IOUT =0mA, DQ, DM and DQS inputs changing twice per clock cycle; 50% addresses changing once per clock cycle	ICC7	250	235	235	185		20

AC Operating Conditions (Ta=0~70°C, V_{DD}=V_{DDQ}=2.5 ± 0.2V, V_{SS}=V_{SSQ}=0V, unless otherwise noted)

Description	Parameter	Min.	Max.	Unit	NOTES
Input High Voltage	V_{IH}(AC)	V_{REF}+0.35		V	
Input Low Voltage	V_{IL}(AC)		V_{REF}-0.35	V	
Input Differential Voltage, CLK and CLK# inputs	V_{ID}(AC)	0.7	V_{DDQ}+0.6	V	7
Input Crossing Point Voltage, CLK and CLK# inputs	V_{IX}(AC)	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V	8
Input Leakage Current Any input, 0V<=V_{IN}<=V_{DD}, V_{REF} pin 0V<=V_{IN}<=1.35V (All other pins not under test=0V)	I_I	-2	2	μA	
Output Leakage Current (DQs are disabled ; 0V<=Vout<=V_{DDQ})	I_{OZ}	-5	5	μA	
Output High Current (V_{out}=1.95V)	I_{OH}	-15.2		mA	
Output Low current (V_{out}=0.35V)	I_{OL}	15.2		mA	

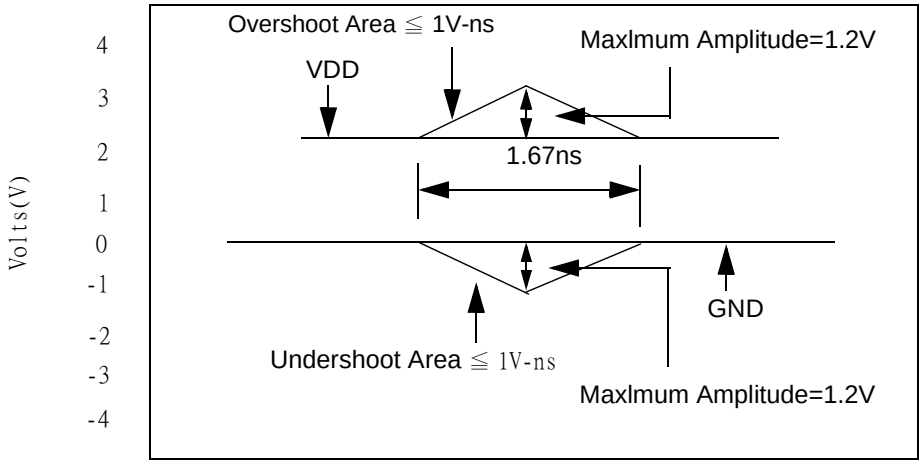
Overshoot / Undershoot specification for /CS, CKE, BA0-BA1, A0-A12, /RAS, /CAS & /WE pins

Parameter	Specification	Notes
Maximum peak amplitude allowed for overshoot	1.5 V	
Maximum peak amplitude allowed for undershoot	1.5 V	
Duration of pulse	≦ 3ns	
Overshoot/Undershoot area	≦ 2.25 V-ns	



Overshoot/Undershoot specification for CK, /CK, DQ, DQS & DM pins

Parameter	Specification	Notes
Maximum peak amplitude allowed for overshoot	1.2 V	
Maximum peak amplitude allowed for undershoot	1.2 V	
Duration of pulse	≦ 1.67ns	
Overshoot/Undershoot area	≦ 1V-ns	



AC Characteristics:

Test Conditions: (Ta=0 to 70°C V_{DDQ}=2.5V ± 0.2V , V_{DD}= 2.5V ± 0.2V)

A.C. Parameter		Symbol	-66		-7L		-75		-8		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
DQ output valid data delay time from CLK/CLK#		t_{AC}	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
DQS output valid data delay time from CLK/CLK#		t_{DQSCK}	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock cycle time	CL=2.5	t_{CK}	6.6	15	7.5	15	7.5	15	8	15	ns	
	CL=2	t_{CK}	7.5	15	7.5	15	10	15	10	15	ns	
DQ and DM input hold time relative to DQS		t_{DH}	0.5		0.5		0.5		0.6		ns	
DQ and DM input setup time relative to DQS		t_{DS}	0.5		0.5		0.5		0.6		ns	
Clock half period		t_{HP}	tCL min or tCH min		tCL min or tCH min		tCL min or tCH min		tCL min or tCH min		ns	
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		1.75		2		ns	
Data-out high impedance from CLK/CLK#		t_{HZ}	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	14
Data-out low impedance from CLK/CLK#		t_{LZ}	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	14
DQS-DQ Skew (for DQS and associated DQ signals)		t_{DQSQ}		+0.5		+0.5		+0.5		+0.6	ns	
Output DQS valid window		t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	
Data hold skew factor		t_{QHS}		+0.75		+0.75		+0.75		+1.0	ns	
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
MODE REGISTER SET COMMAND cycle time		t_{MRD}	2		2		2		2		t_{CK}	
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		0.35		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		0.35		t_{CK}	
DQS falling edge to CK setup time		t_{DSS}	0.2		0.2		0.2		0.2		t_{CK}	
DQS falling edge to CK hold time		t_{DSH}	0.2		0.2		0.2		0.2		t_{CK}	
Write preamble setup time		t_{WPRES}	0		0		0		0		ns	16
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	15
Write preamble		t_{WPRE}	0.25		0.25		0.25		0.25		t_{CK}	
Input hold time(Address / Control)	fast slew rate	t_{IH}	0.9		0.9		0.9		1.1		ns	19
	slow slew rate		1.1		1.1		1.1		1.1			
Input setup time(Address / Control)	fast slew rate	t_{IS}	0.9		0.9		0.9		1.1		ns	19
	slow slew rate		1.1		1.1		1.1		1.1			
Read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	

A.C. Parameter	Sym-bol	-66		-7L		-75		-8		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Row active time	t_{RAS}	40	120 K	45	120 K	45	120 K	50	120 K	ns	
Row cycle time	t_{RC}	60		65		65		70		ns	
Auto refersh to Active/Auto refresh command period	T_{RFC}	70		75		75		80		ns	
ACTIVE to READ or WRITE delay	t_{RCD}	20		20		20		20		ns	
Refresh period (8192 rows)	t_{REF}		64		64		64		64	ms	
PRECHARGE command period	t_{RP}	20		20		20		20		ns	
ACTIVE to ACTIVE delay time	t_{RRD}	15		15		15		15		ns	
Write recovery time	t_{WR}	15		15		15		15		ns	
Auto Prechange write recovery+precharge time	t_{DAL}	t_{WR}/ t_{CK} + t_{RP} / t_{CK}		t_{WR}/ t_{CK} + t_{RP} / t_{CK}		t_{WR}/ t_{CK} + t_{RP} / t_{CK}		t_{WR}/ t_{CK} + t_{RP} / t_{CK}		t_{CK}	
Write data In to Read Command Delay	t_{WTR}	1		1		1		1		t_{CK}	
Exit SELF REFRESH to non-READ command	t_{XNR}	70		75		75		80		ns	
Exit SELF REFRESH to READ command	t_{XRD}	200		200		200		200		t_{CK}	
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8		7.8	μs	17

Notes

1. All voltages are referenced to V_{SS}.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics, may be conducted at nominal reference / supply voltage levels. However, the specifications and device operations are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use the VIL TO VIH swing of up to 1.5V in the test environment. Input timing is still referenced to VREF (or to the crossing point for CK // CK) , and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minmum slew rate for the input signals is 1V/ns in the range between VIL(AC) AND VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*Vddq of the transmitting device , and to track variations in the DC level of the same. Peak-to -peak noise on VREF may not exceed +-2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*Vddq of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized.
11. This parameter is sampled. Vddq=2.5V+-0.2V, Vdd=2.5V+-0.2V, f=100MHz, Ta=2.5^{0}C, VOUT(DC)=Vddq/2, VOUT(PEAK TO PEAK) = 25mv. DM inputs are grouped with I/O pins-reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
12. The CLK // CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and / CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE<=0.3Vddq is recognized as LOW.
14. tHZ and tLZ transitions occur in the same access time windows as vaild data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

16.The specific requirement is that DQS be valid(HIGH, LOW , or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and satisfies the input slew rate specifications. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW, if a previous wtrite was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

17.A maximum of eight AUTO REFRESH commands can be asserted to any given DDR SDRAM device.

18.tXPRD should be 200 tCLK when the clocks are unstable during the power down mode.

19.For command /address and CK & /CK slew rate >1.0V/ns.

20.IDD7: Operating current is measured under the conditions

(1) Four Bank are being interleaved with tRC(min), burst mode, address and control inputs on NOP edge are not changing. Iout=0mA.

(2) Timing Patterns

-DDR 200(-10) (100MHz, CL=2): tCK=10ns, CL=2, BL=4 , tRRD=2*tCK, tRCD=3*tCK,Read wtih auto-prechagre

Setup: A0 N A1 R0 A2 R1 A3 R2

Read: A0 R3 A1 R0 A2 R1 A3 R2 - repeat the same timing with randon address changing

50% of data changing at every transfer.

-DDR266B(-75) (133MHz, CL=2.5) : tCK=7.5ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK,

Read with autoprecharge

Setup:A0 N A1 R0 A2 R1 A3 R2 N R3

Read: A0 N A1 R0 A2 R1 A3 R2 N R3 - repeat the same timing with random address changing

50% of data changing at every transfer

-DDR266A(-7L)(133MHz, CL=2) : tCK=7.5ns, CL=2, BL=4, tRRD=2*tCK, tRCD=3*tCK,

Read with autoprecharge

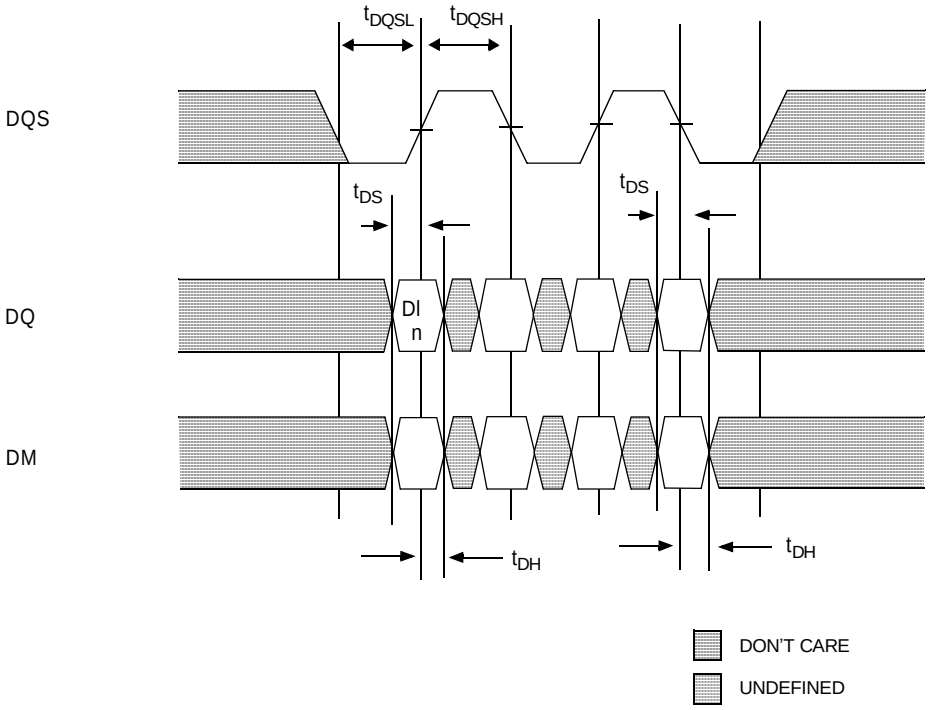
Setup: A0 N A1 R0 A2 R1 A3 R2 N R3

Read: A0 N A1 R0 A2 R1 A3 R2 N R3-repeat the same timing with random address changing

50% of data changing at every tranfer

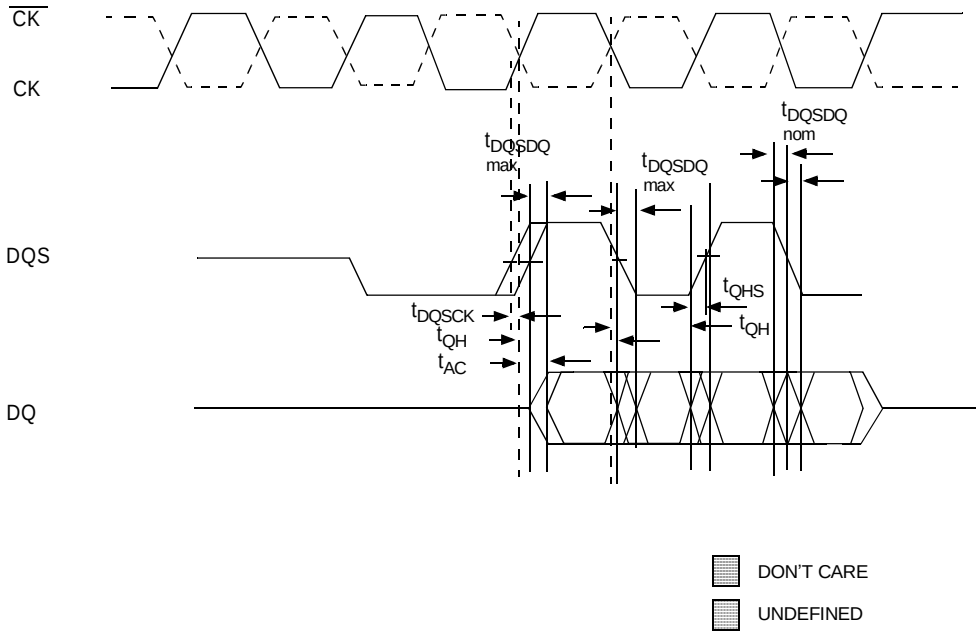
*Legend: A=Activate, R=Read, P=Precharge, N=NOP

DATA INPUT TIMING



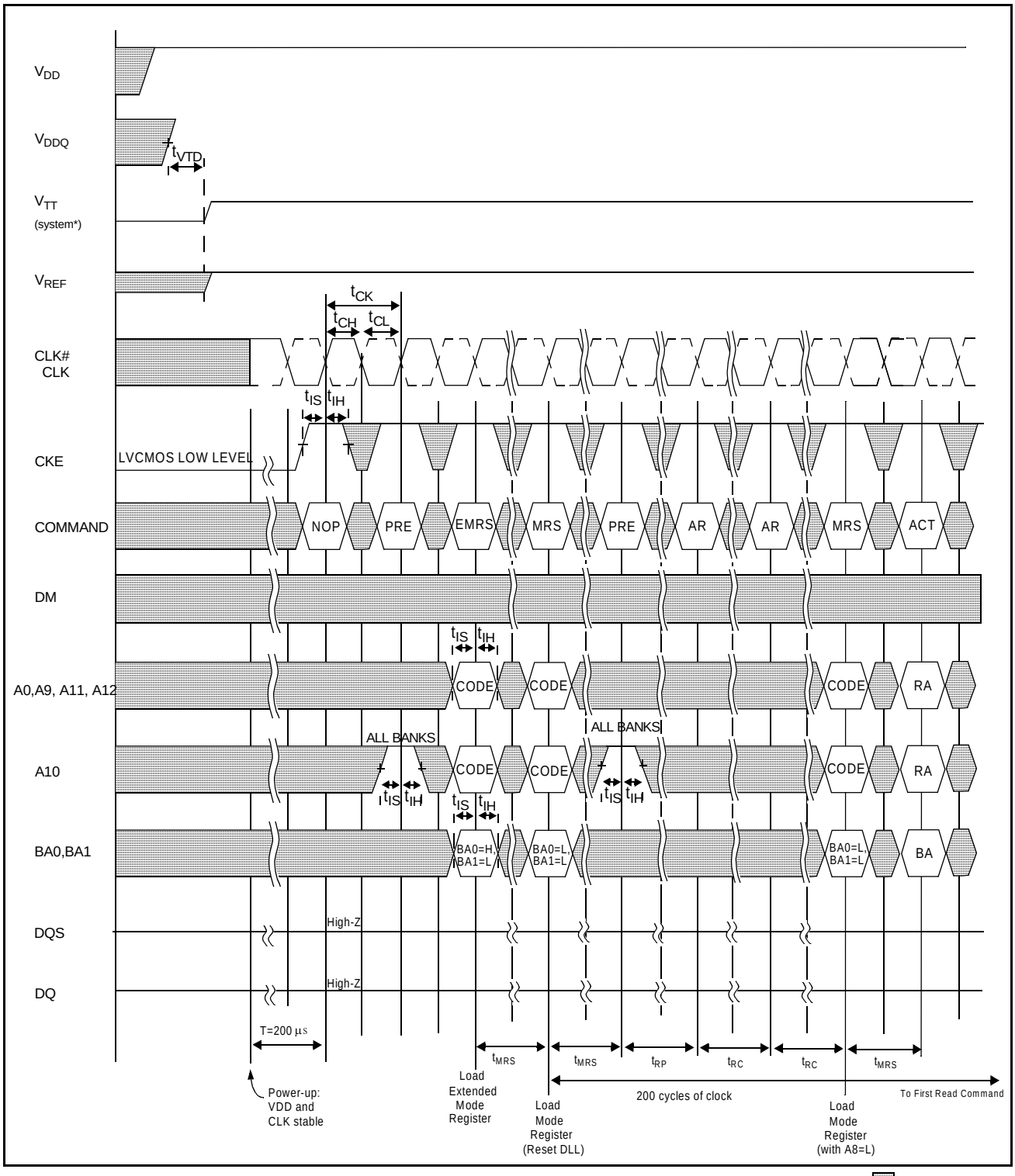
Dl n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following Dl n

DATA OUTPUT TIMING



Burst Length=4 in the case shown

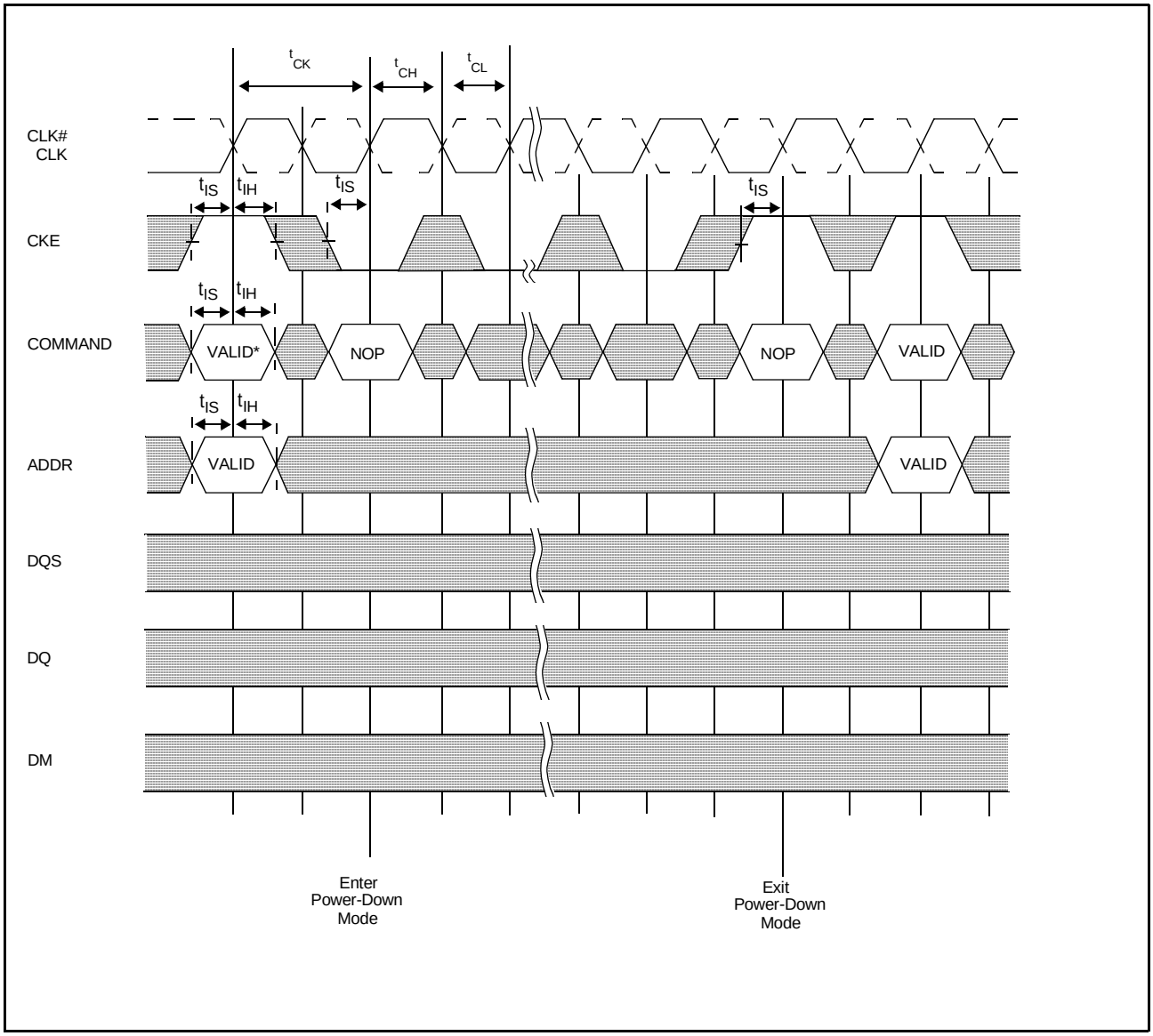
INITIALIZE AND MODE REGISTER SET



•=VTT is not applied directly to the device, however t_{VTD} must be greater than or equal to zero to avoid device latch-up.

••=t_{MRS} is required before any command can be applied, and 200 cycles of CLK are required before a READ command can be applied.

POWER-DOWN MODE

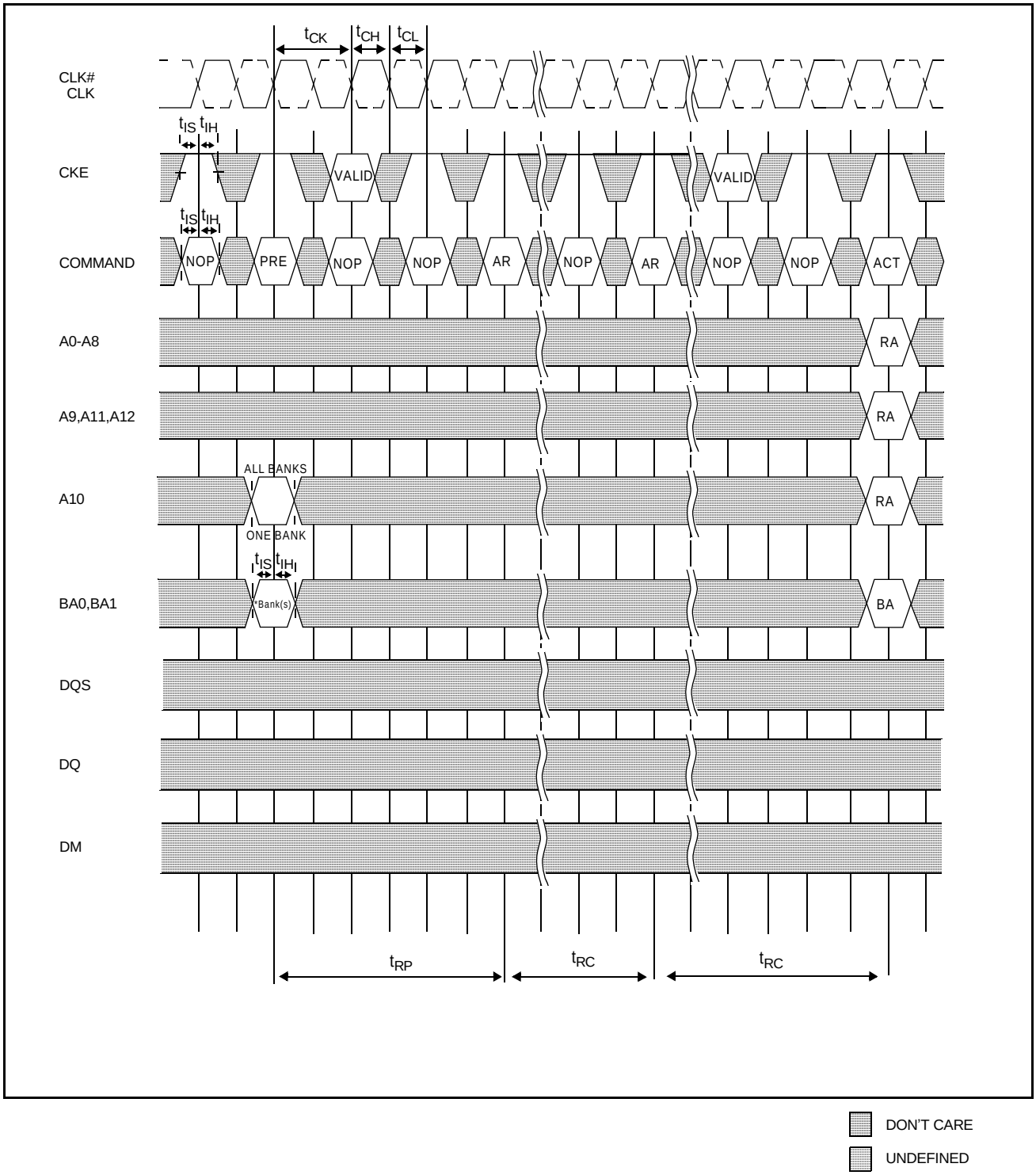


DON'T CARE

UNDEFINED

No column accesses are allowed to be in progress at the time Power-Down in entered
*= If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at lease one row is already active) then the Power-Down mode shown is Active Power Down.

AUTO REFRESH MODE



DIS AP = Disable Autoprecharge

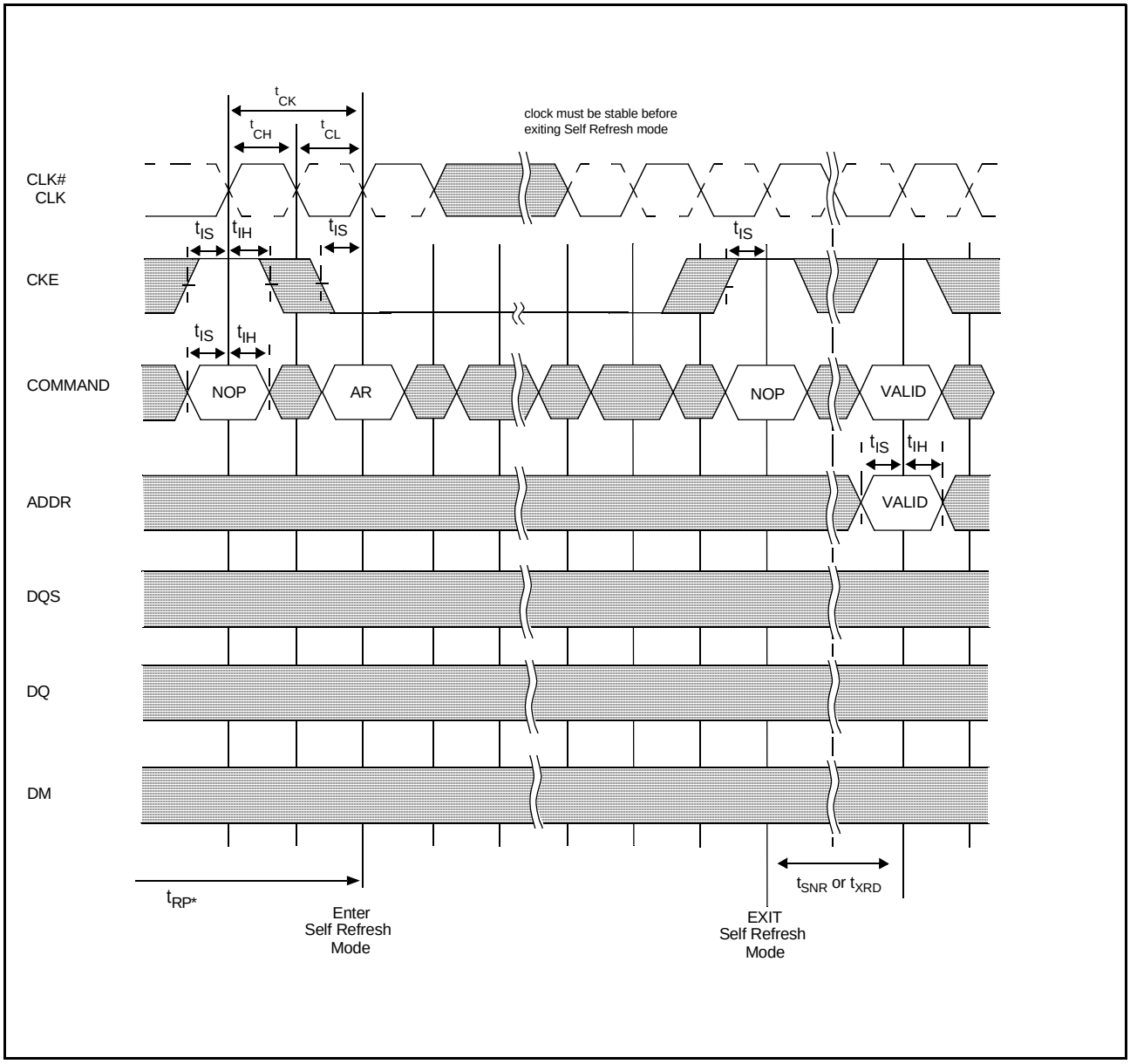
*=*Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active(i.e. must pre-charge all active banks)

PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address, AR=AUTOREFRESH

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

DM, DQ and DQS signals are all "Don't Care"/High-Z for operations shown

SELF REFRESH MODE

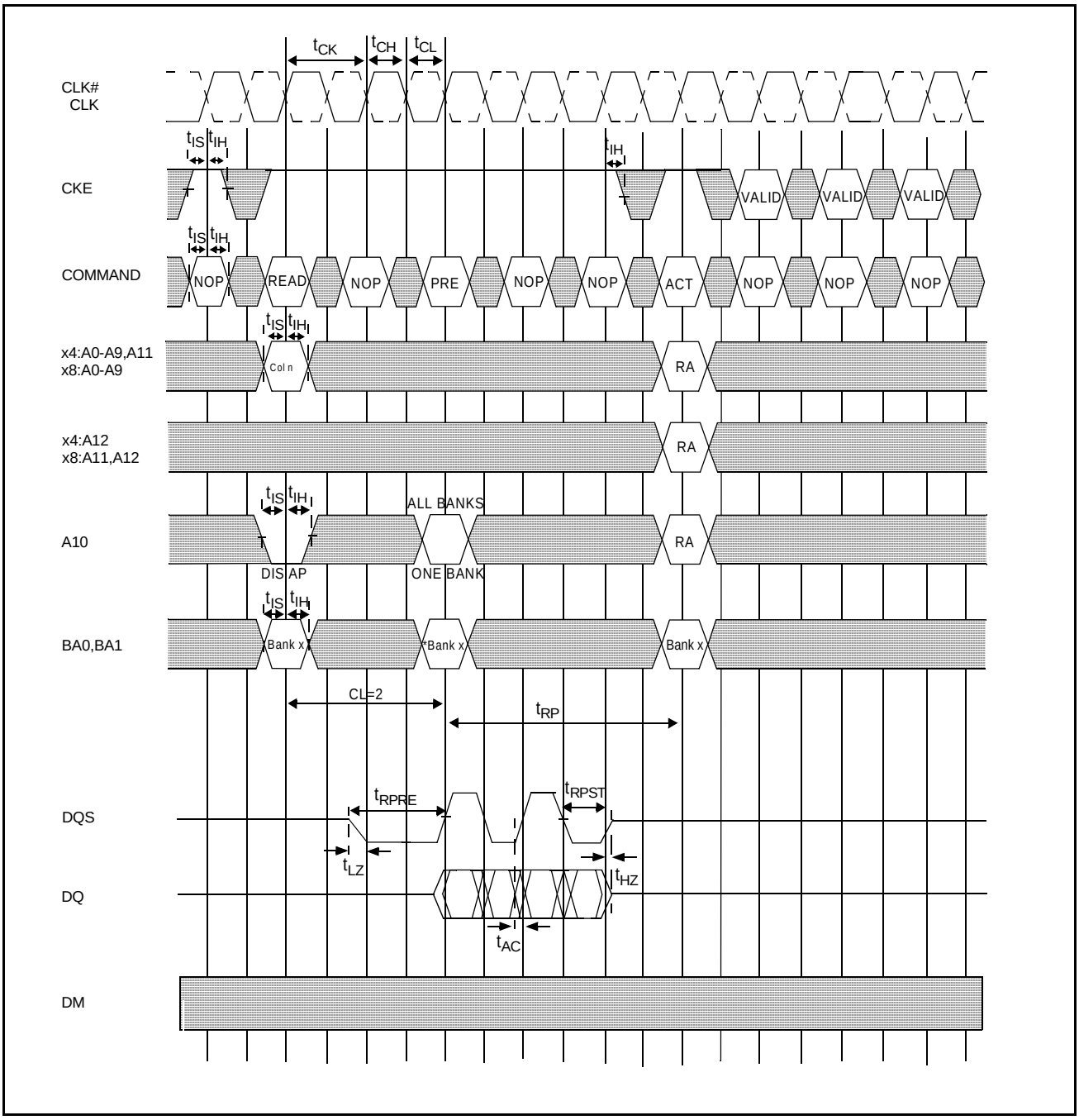


*=Device must be in the "All banks idle" state prior to entering Self Refresh mode

**=t_{SNR} is required before any non-READ command can be applied, and t_{XRD} is required before a READ command can be applied.

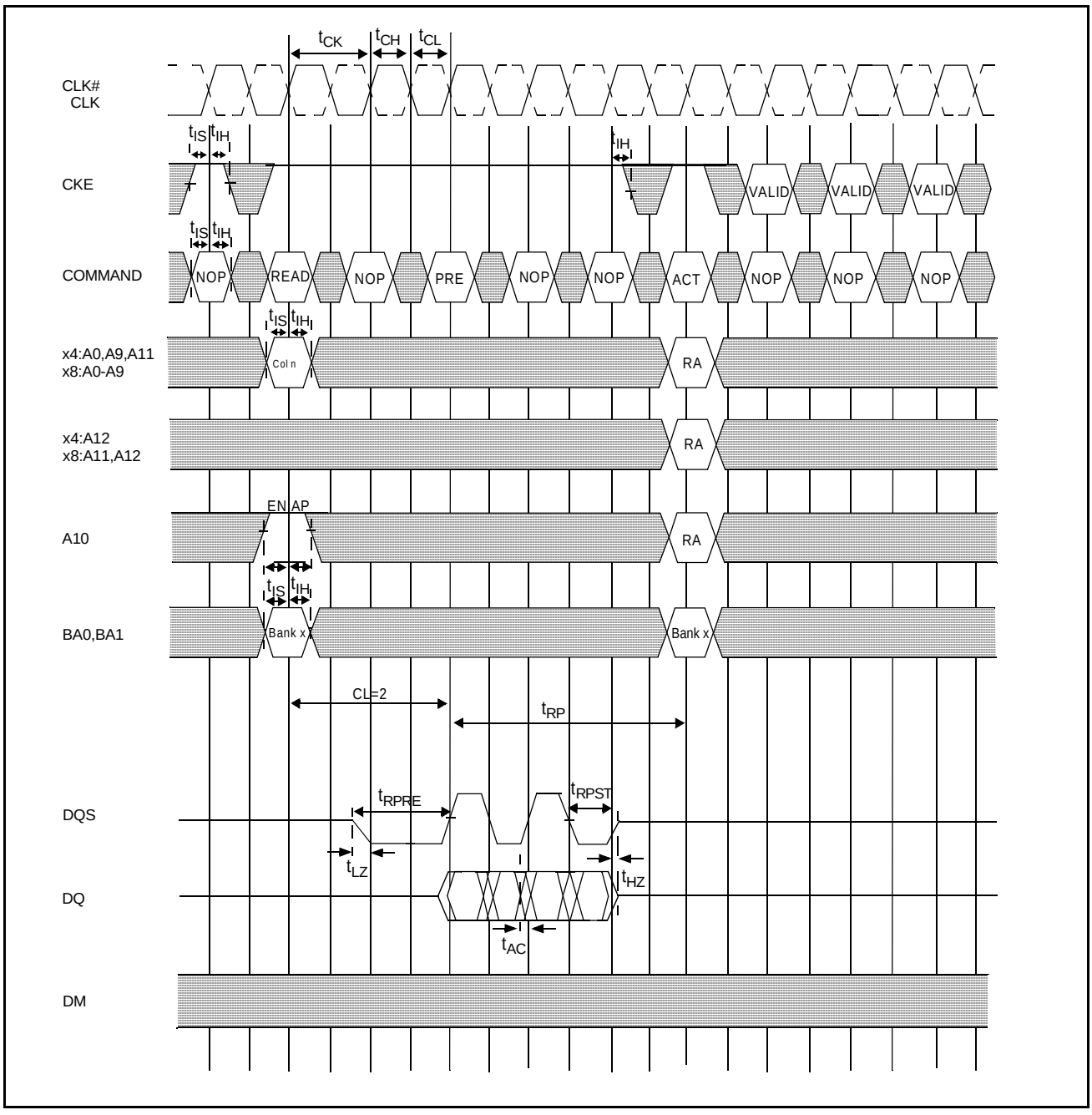
The minimum time in Self Refresh mode is t_{RAS} MIN.

READ-WITHOUT AUTO PRECHARGE



DO n=Data Out from column n
Burst Length=4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following Do n
DIS AP= Disable Autoprecharge
*="Don't Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE,RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

READ-WITH AUTO PRECHARGE

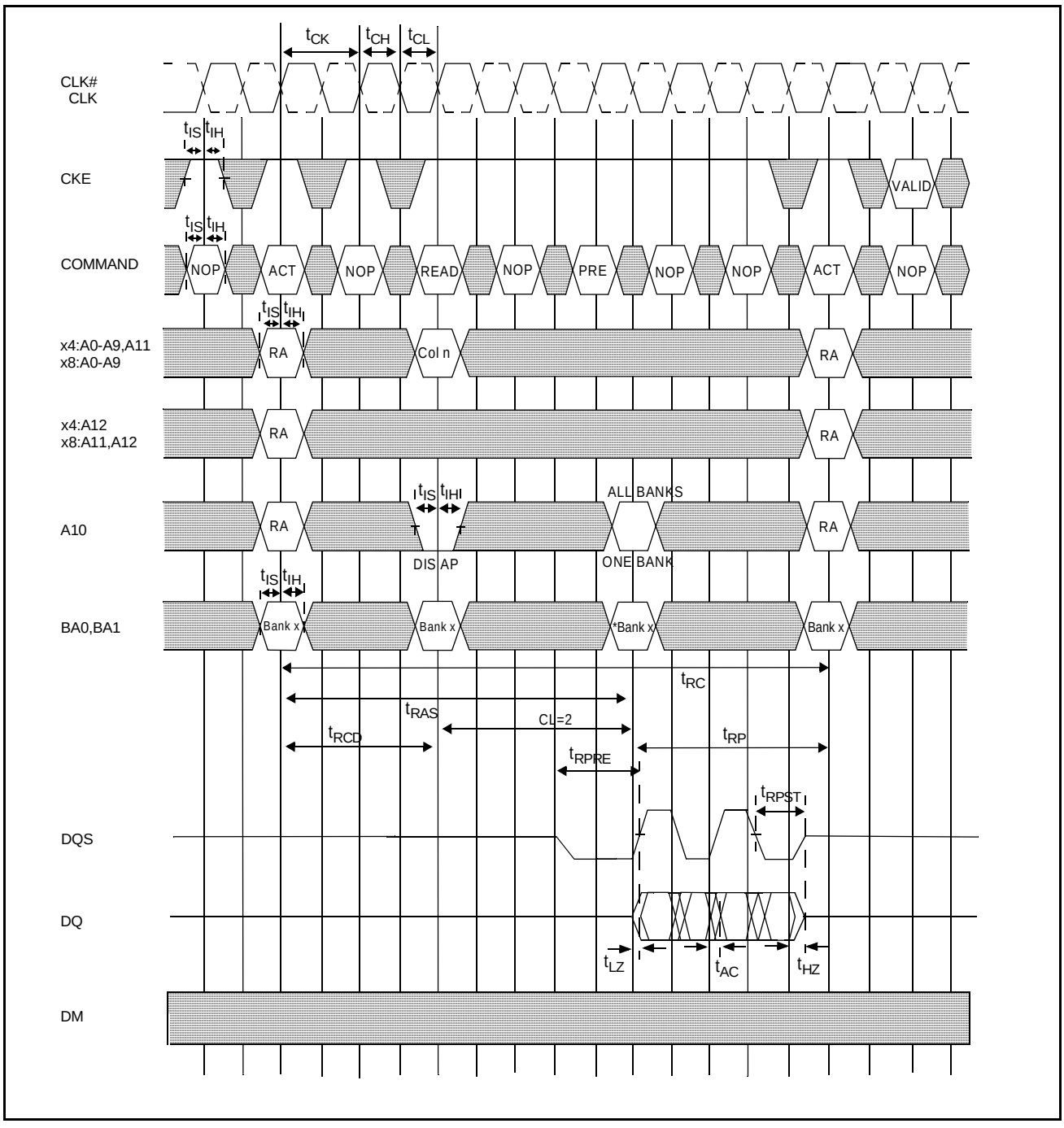


DON'T CARE

UNDEFINED

DO n=Data Out from column n
Burst Length=4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP=Enable Autoprecharge
ACT=ACTIVE, RA=Row Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

BANK READ ACCESS

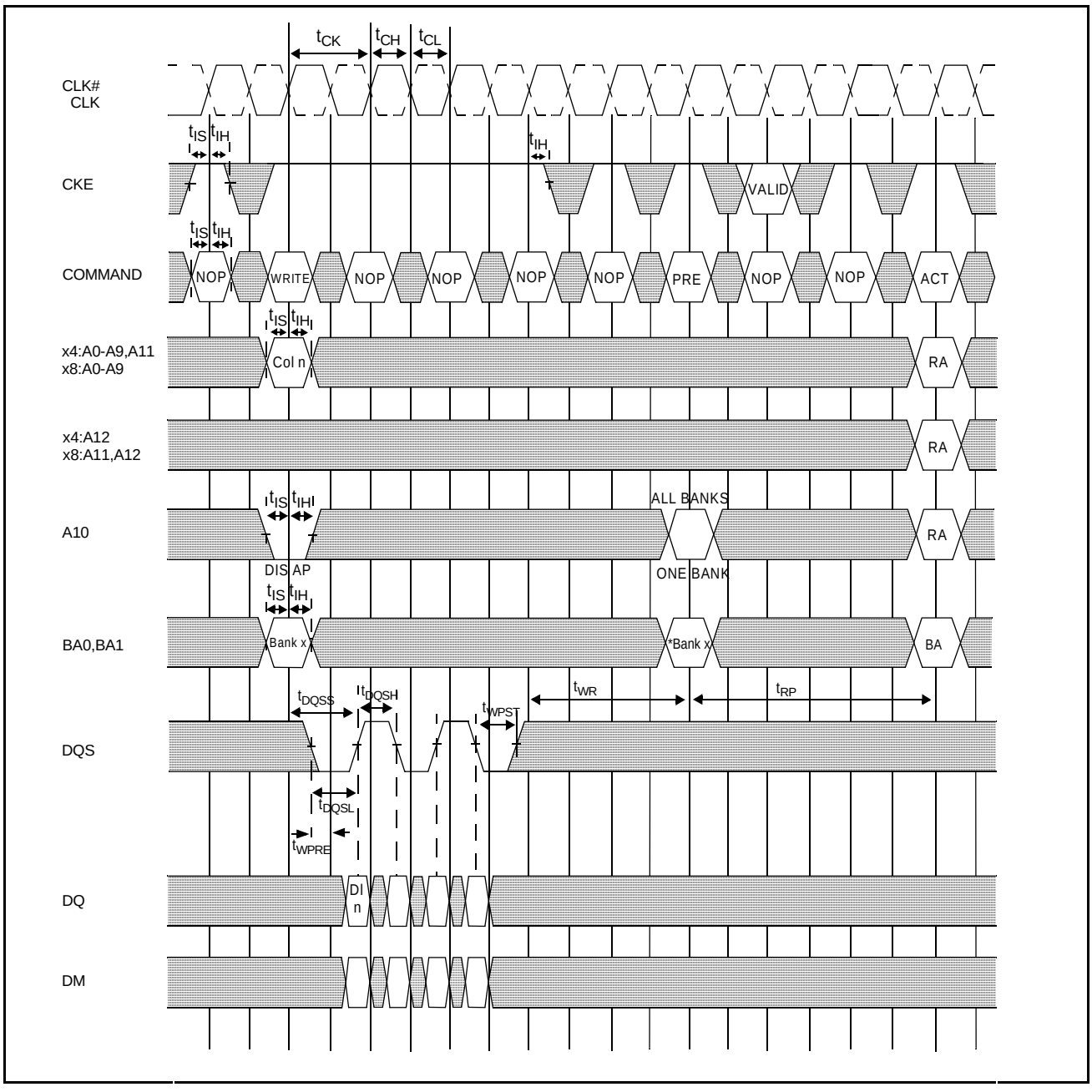


DON'T CARE

UNDEFINED

DO n=Data Out from column n
Burst Length=4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP=Disable Autoprecharge
*="Don't Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

WRITE-WITHOUT AUTO PRECHARGE

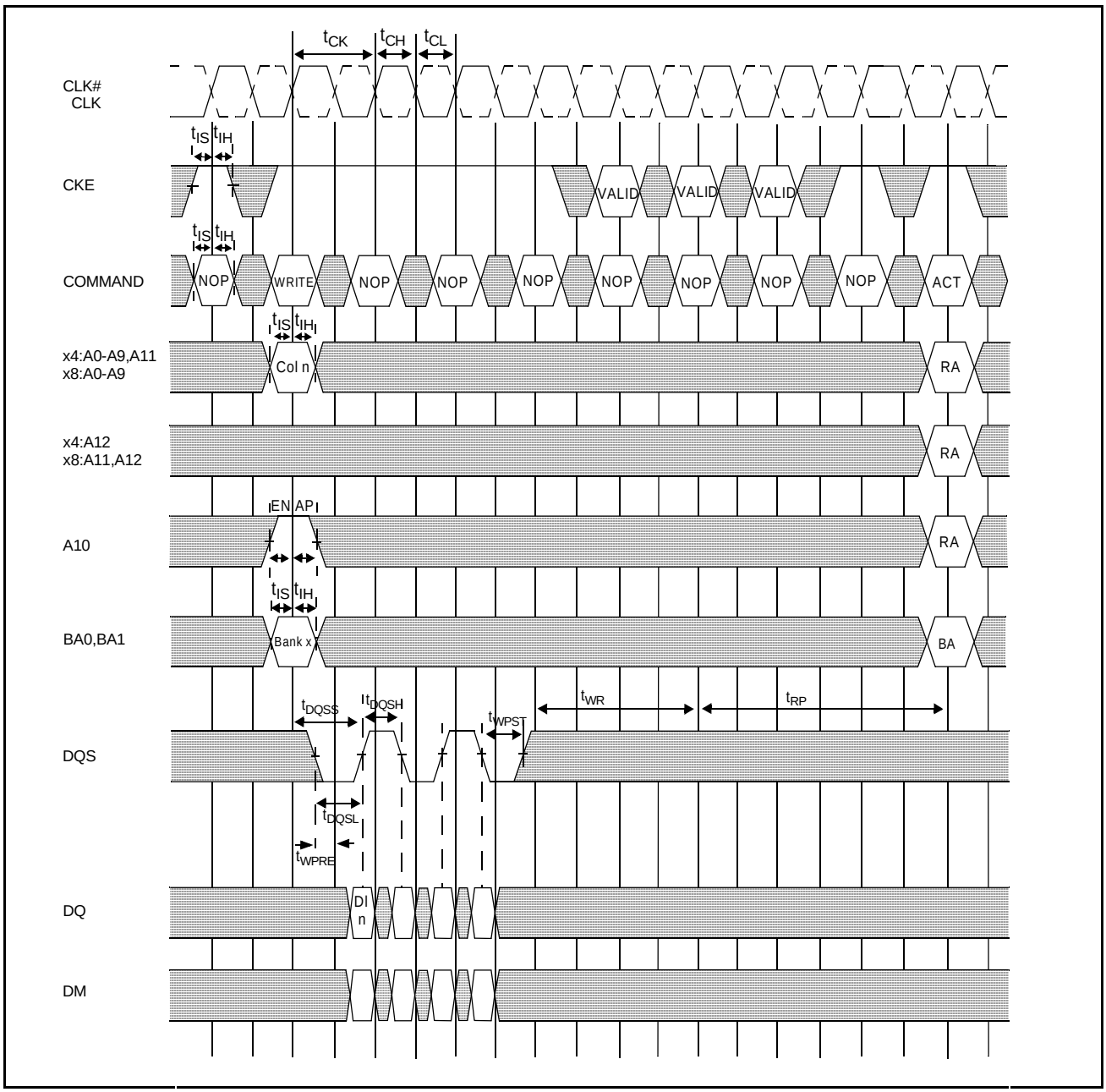


DON'T CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP=Disable Autoprecharge
*="Don't Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

WRITE-WITH AUTO PRECHARGE

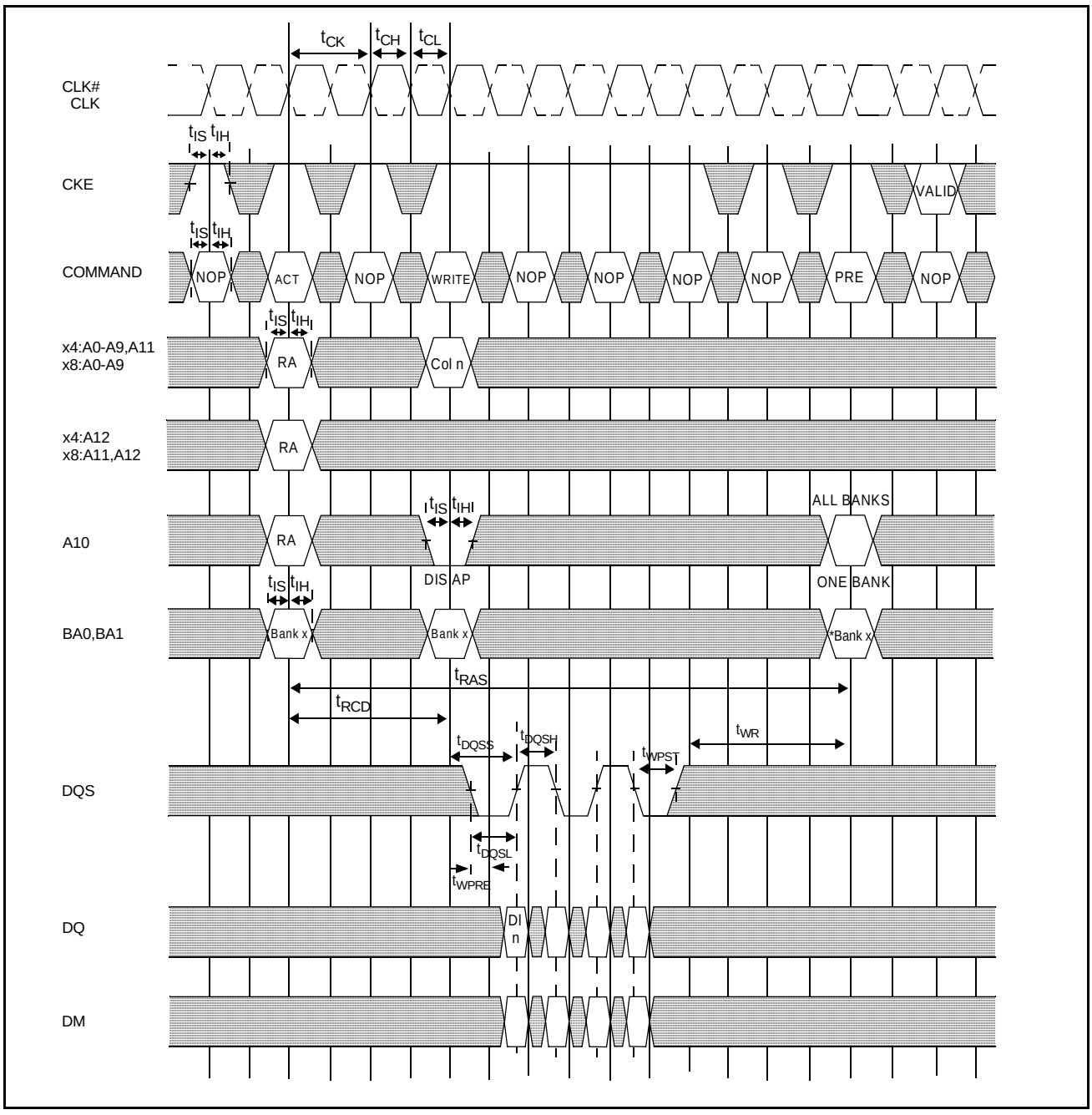


DON'T CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP=Disable Autoprecharge
*="Don't Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

BANK WRITE ACCESS

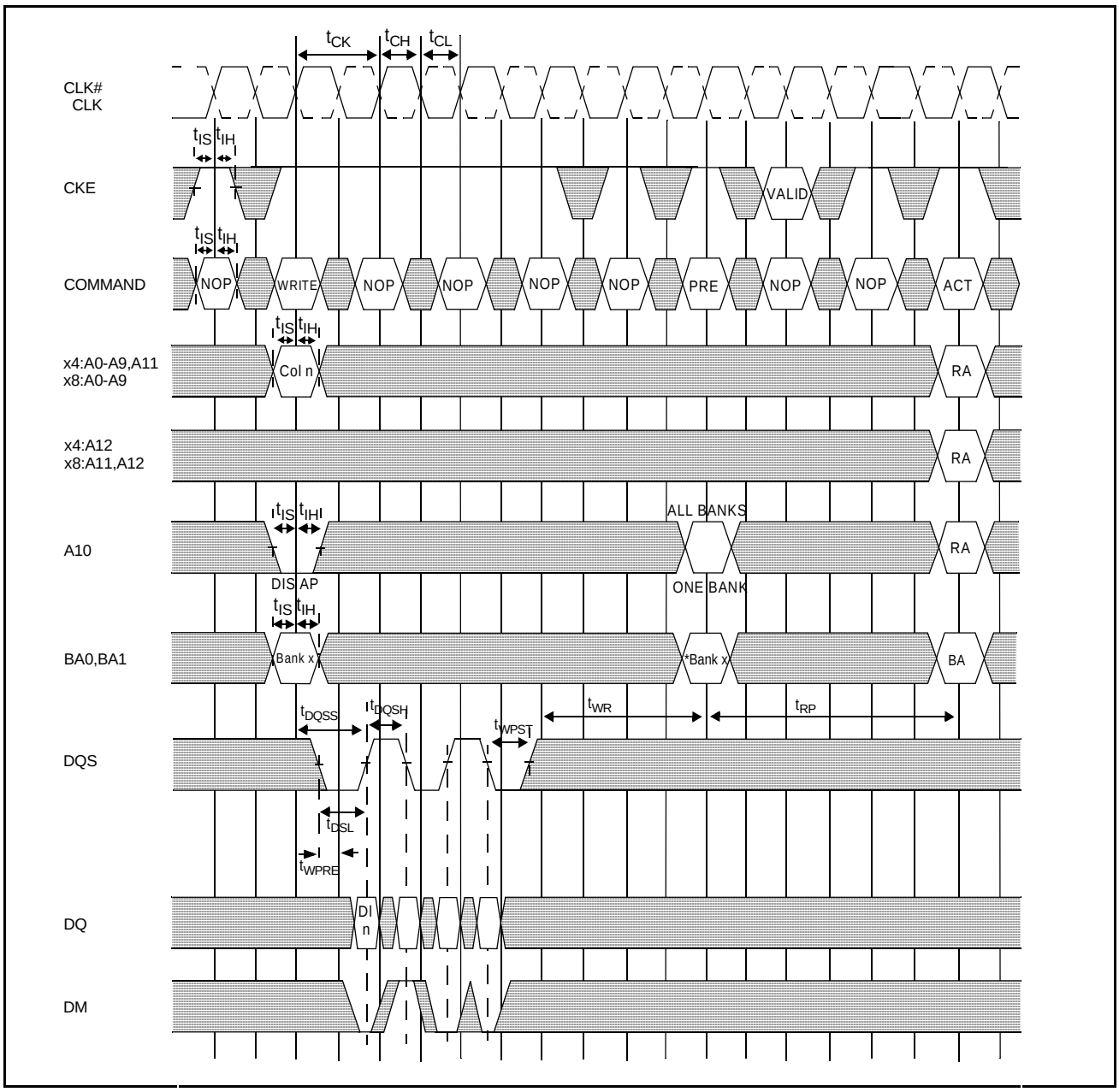


DON'T CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n
DIS AP=Disable Autoprecharge
*="Don't Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

WRITE-DQM OPERATION



DON'T CARE

UNDEFINED

DI n=Data In for column n
Burst Length=4 in the case shown
3 subsequent elements of Data In are provided in the programmed order following DI n (The second element of the four is masked)
DIS AP=Disable Autoprecharge
*="Don't Care", if A10 is HIGH at this point
PRE=PRECHARGE, ACT=ACTIVE, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be possible at these times

Ordering information

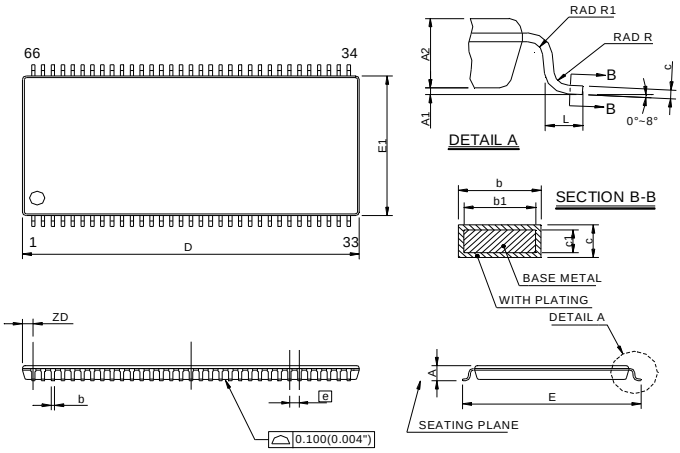
Part Number	Cycle time	Package
VG3725640(80)2AT-66	6.6 ns (150MHz 2.5/3/3) 7.5 ns (133MHz 2/3/3)	400mil, 66-Pin TSOP II 0.65mm Lead Pitch
VG3725640(80)2AT-7L	7.5 ns (133MHz 2/3/3) 7.5 ns (133MHz 2.5/3/3)	
VG3725640(80)2AT-75	7.5 ns (133MHz 2.5/3/3) 10 ns (100MHz 2/2/2)	
VG3725640(80)2AT-8	8 ns (125MHz 2.5/3/3) 10 ns (100MHz 2/2/2)	

VG37256402AT-7

- VG : VIS Memory Product
- 37 : Technology/Design Rule, 37: DDR
- 256 : 256Mb density
- 40 : Device Configuration, 40:x4, 80: x8
- 2 : Interface Type, 2: SSTL_2
- A : Mask/Design Version
- T : Package Type, T: TSOPII
- 7 : Cycle time, i.e. t_{CK}

Packaging Information

• 400mil, 66-Pin TSOP II



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.22	---	0.38	0.009	---	0.015
b1	0.22	0.30	0.33	0.009	0.012	0.013
c	0.12	---	0.21	0.005	---	0.008
c1	0.12	0.125	0.16	0.005	0.005	0.006
D	22.09	22.22	22.35	0.870	0.875	0.880
e	0.65 BASIC			0.026 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.12	---	0.35	0.005	---	0.014
R1	0.12	---	---	0.005	---	---
ZD	0.71 REF			0.028 REF		

NOTE: 1. CONTROLLING DIMENSION : MILLIMETERS
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.
MOLD PROTRUSION SHALL NOT EXCEED 0.15mm (0.006”) PER SIDE
DIMENSION E1 DOES NOT INCLUDE INTER LEAD PROTRUSION.
INTER LEAD PROTRUSION SHALL NOT EXCEED 0.25mm (0.01”) PER SIDE
3. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSIONS/INTRUSION.
ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD TO
BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm.
DAM BAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER
THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.