1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- **Independently-Programmable Rise and Fall Times**
- **Low Output Impedance ..... 7Ω Typ**
- **High Speed t_R, t_F ..... <30 nsec with 1000 pF Load**
- **Short Delay Times ..... < 30 nsec**
- **Wide Operating Range ..... 4.5V to 18V**
- **Latch-Up Protected ..... Will Withstand >500 mA Reverse Current (Either Polarity)**
- **Input Withstands Negative Swings Up to –5V**

APPLICATIONS

- **Motor Controls**
- **Driving Bipolar Transistors**
- **Driver for Nonoverlapping Totem Poles**
- **Reach-Up/Reach-Down Driver**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4404COA	8-Pin SOIC	0°C to +70°C
TC4404CPA	8-Pin PDIP	0°C to +70°C
TC4404EOA	8-Pin SOIC	– 40°C to +85°C
TC4404EPA	8-Pin PDIP	– 40°C to +85°C
TC4404MJA	8-Pin CerDIP	– 55°C to +125°C
TC4405COA	8-Pin SOIC	0°C to +70°C
TC4405CPA	8-Pin PDIP	0°C to +70°C
TC4405EOA	8-Pin SOIC	– 40°C to +85°C
TC4405EPA	8-Pin PDIP	– 40°C to +85°C
TC4405MJA	8-Pin CerDIP	– 55°C to +125°C

GENERAL DESCRIPTION

The TC4404 and TC4405 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the totem-pole output have been left separated so that individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of drain-current-limiting resistors in the pull-up and/or pull-down sections, allowing the user to define the rates of rise and fall for a capacitive load; or a reduced output swing, if driving a resistive load, or to limit base current, when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 nsec for a 1000-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-ON/fast-OFF operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for an OFF device.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other TelCom drivers. They allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-OFF. By proper positioning of the resistor, either npn or pnp transistors can be driven.

For driving many loads in low-power regimes, these drivers, because they eliminate shoot-through currents in the output stage, require significantly less power at higher frequencies, and can be helpful in meeting low-power budgets.

Because neither drain in an output is dependent on the other, these devices can also be used as open-drain buffer/drivers where both drains are available in one device,

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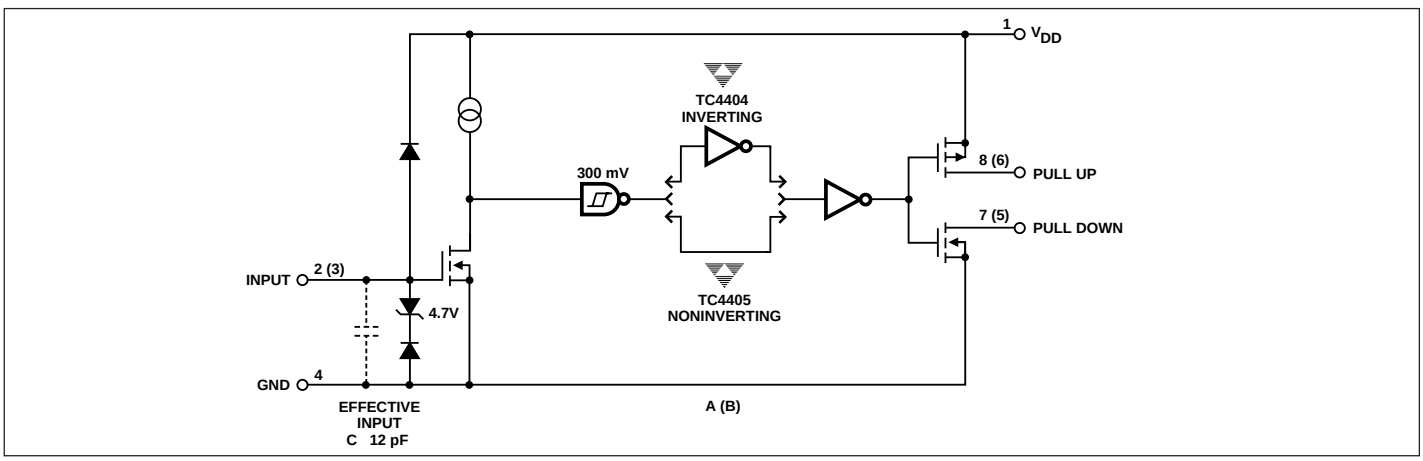
FUNCTIONAL BLOCK DIAGRAM



thus minimizing chip count. Unused open drains should be returned to the supply rail that their device sources are connected to (pull-downs to ground, pull-ups to V_{DD}), to prevent static damage. In addition, in situations where timing resistors or other means of limiting crossover currents are used, like drains may be paralleled for greater current carrying capacity.

These devices are built to operate in the most demanding electrical environments. They will not latch up under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Package Power Dissipation ($T_A \leq 70°C$)
- Plastic 730mW
- CerDP 800mW
- SOIC 470mW

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

Specifications measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	7	10	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle < 2%, t ≤ 300µsec	—	1.5	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	100	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle < 2%, t ≤ 300µsec	> 500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	25	30	nsec
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	25	30	nsec
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	15	30	nsec
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	32	50	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	4.5	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	

NOTE: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS: Specifications measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

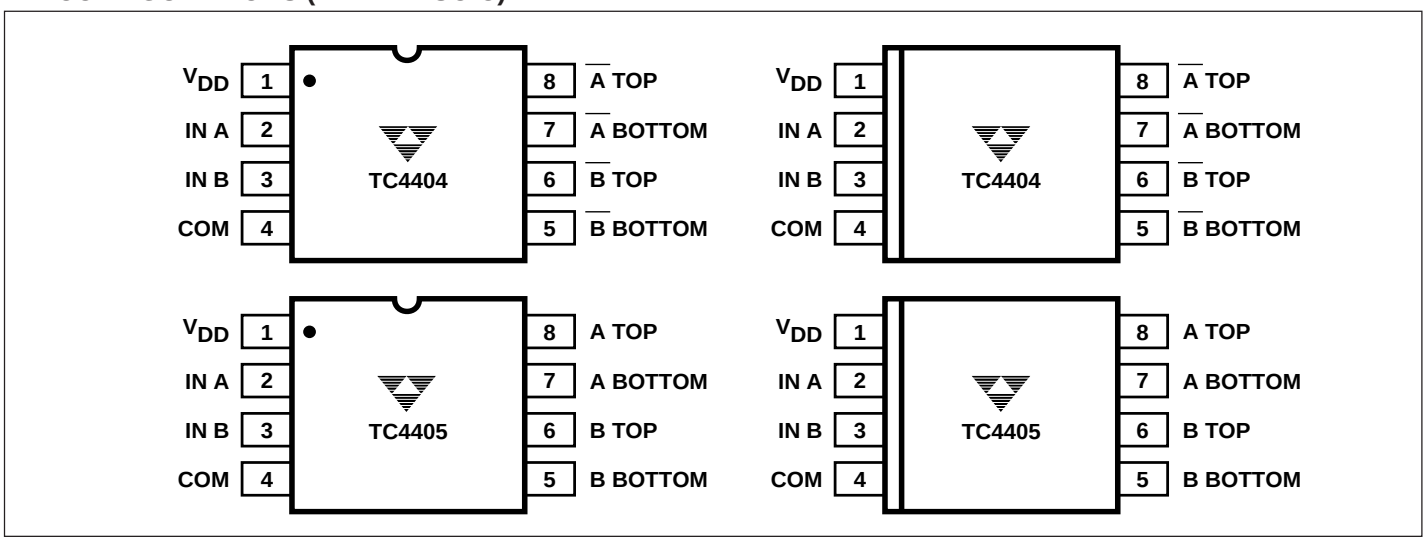
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-0V \le V_{IN} \le V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	9	12	Ω
I_{PK}	Peak Output Current (Any Drain)	Duty cycle <2%, t ≤ 300µsec	—	1.5	—	A
I_{DC}	Continuous Output Current (Any Drain)		—	—	100	mA
I_R	Latch-Up Protection (Any Drain) Withstand Reverse Current	Duty cycle <2%, t ≤ 300µsec	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	—	40	nsec
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	—	40	nsec
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	—	40	nsec
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	—	60	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	

NOTE 1. Switching times guaranteed by design.

Circuit Layout Guidelines

Avoid long power supply and ground traces (added inductance causes unwanted voltage transients). Use power and ground planes wherever possible. In addition, it is advisable that low ESR bypass capacitors (4.7µF or 10µF tantalum) be placed as close to the driver as possible. The driver should be physically located as close to the device it is driving as possible to minimize the length of the output trace.

PIN CONFIGURATIONS (DIP AND SOIC)



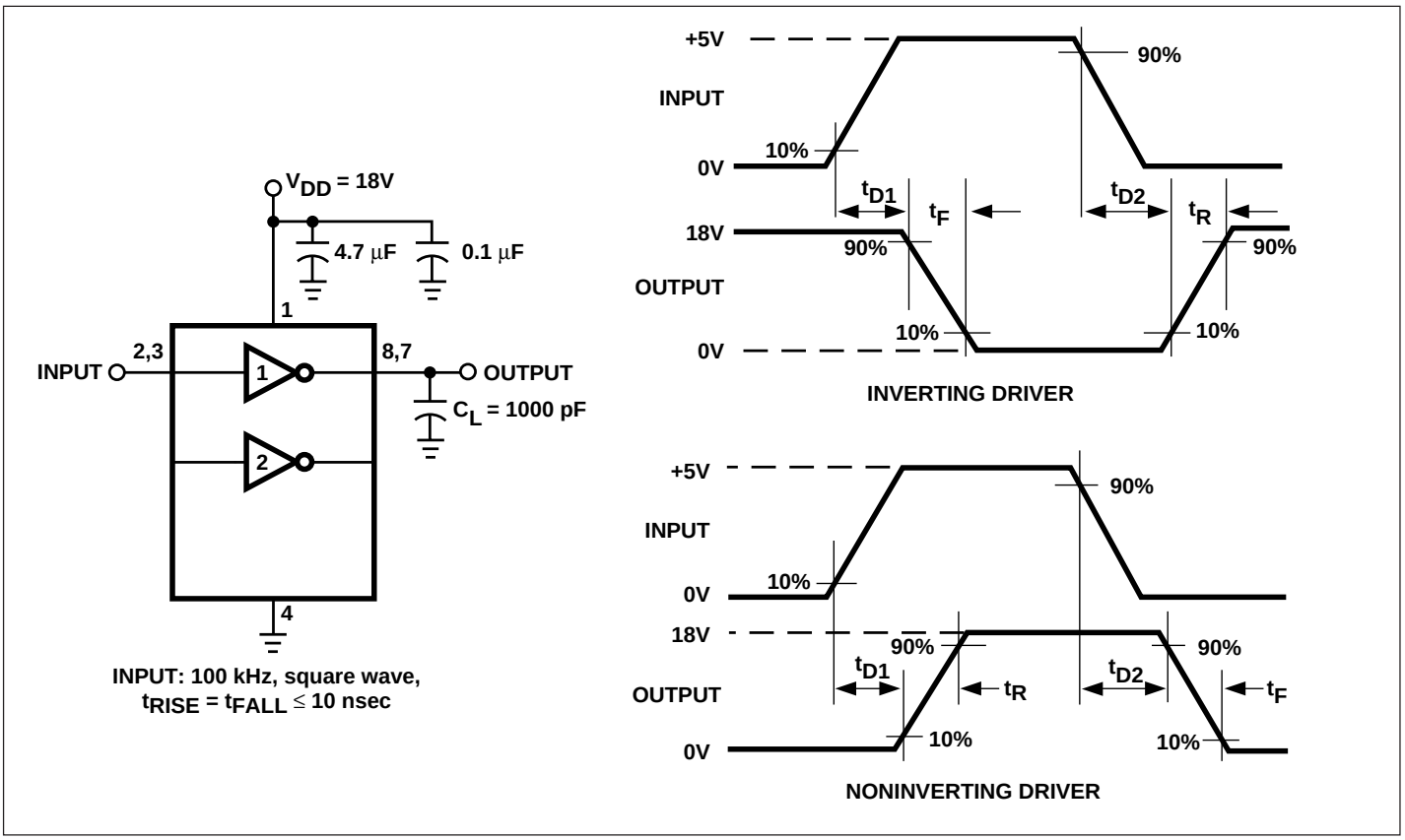
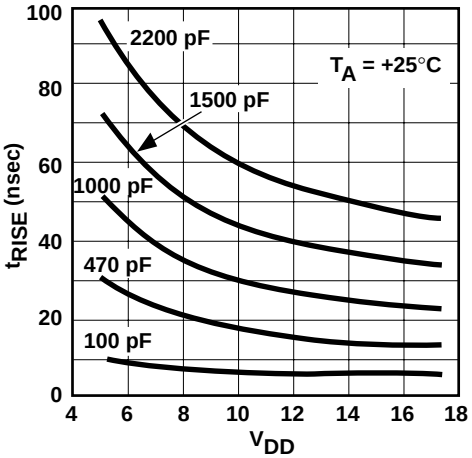


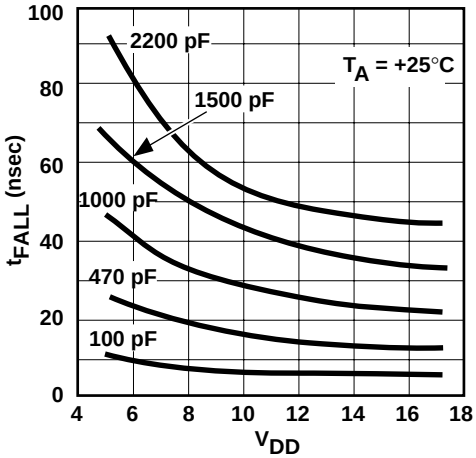
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS

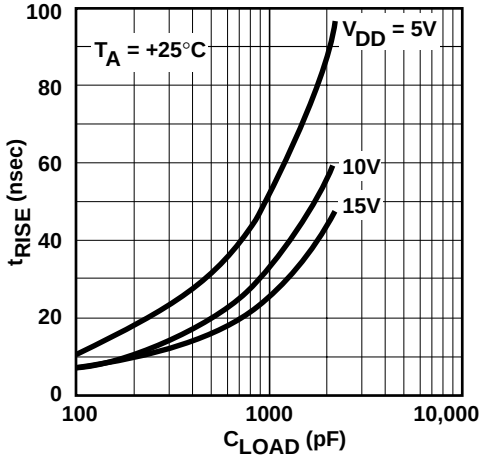
Rise Time vs. Supply Voltage



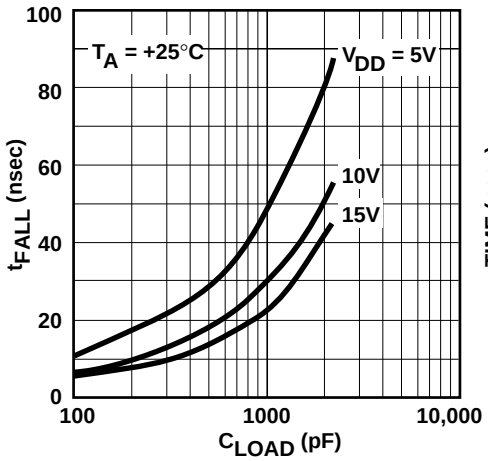
Fall Time vs. Supply Voltage



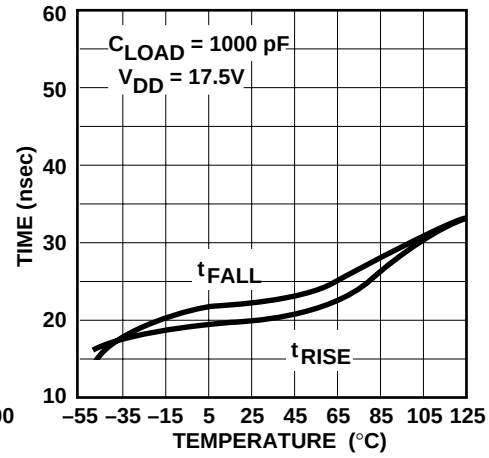
Rise TIme vs. Capacitive Load



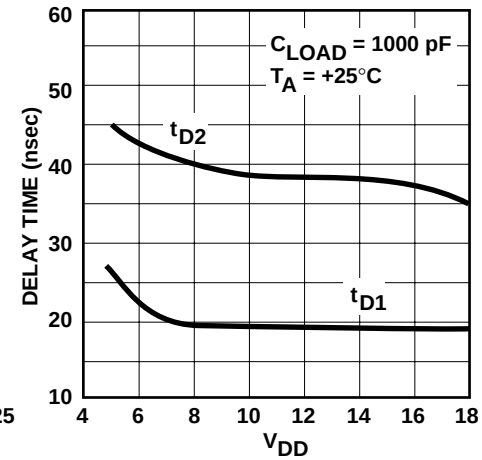
Fall Time vs. Capacitive Load



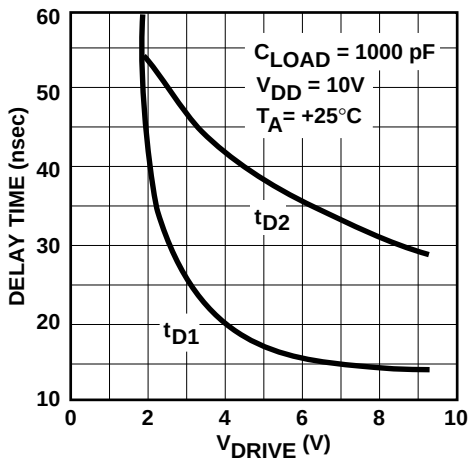
Rise and Fall Times vs. Temperature



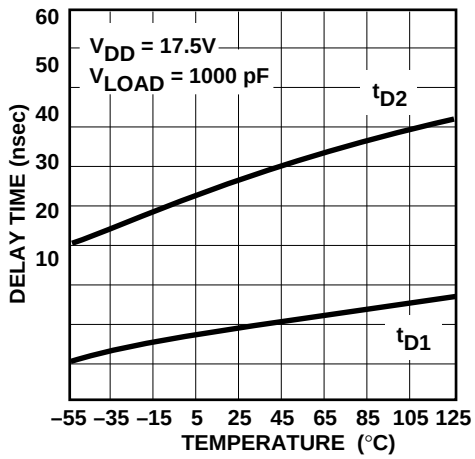
Propagation Delay vs. Supply Voltage



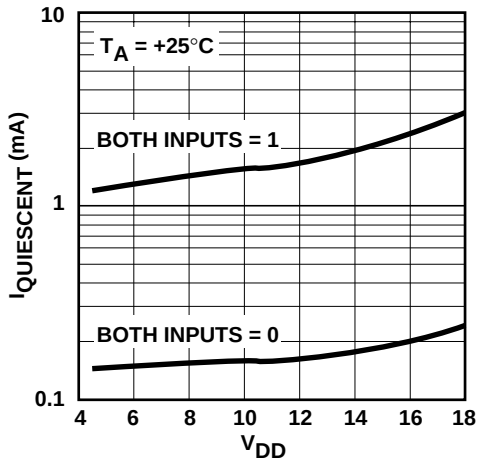
Effect of Input Amplitude on Delay Time



Propagation Delay Time vs. Temperature



Quiescent Supply Current vs. Voltage



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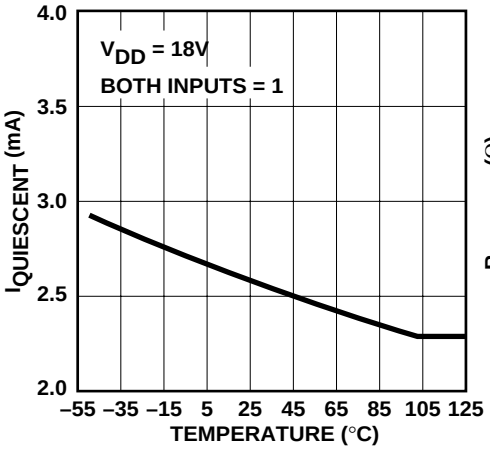
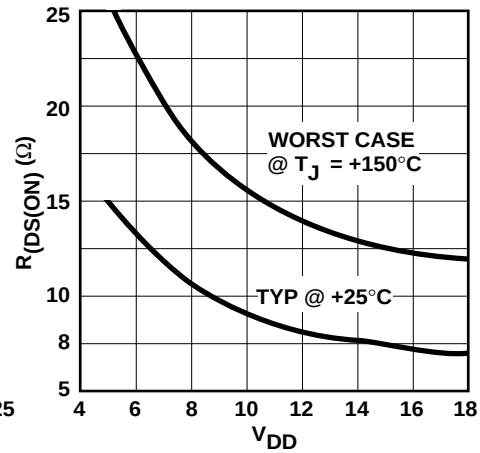
TYPICAL CHARACTERISTICS (Cont.)

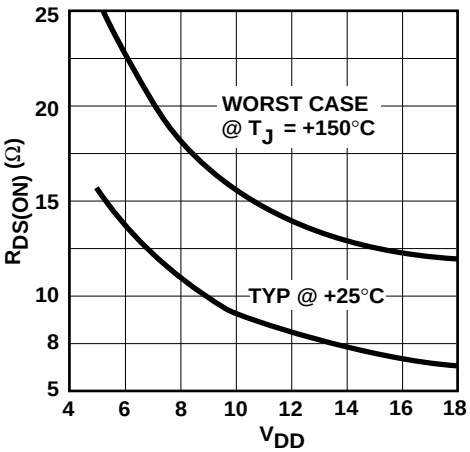
Quiescent Supply Current vs. Temperature



Pull-Up Output Resistance

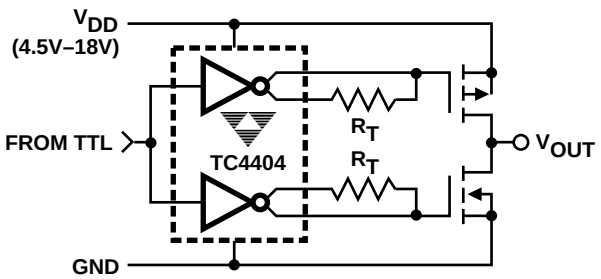


Pull-Down Output Resistance

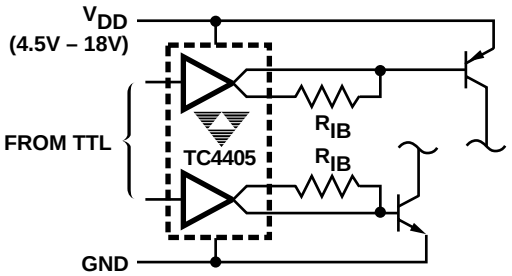


TYPICAL APPLICATIONS

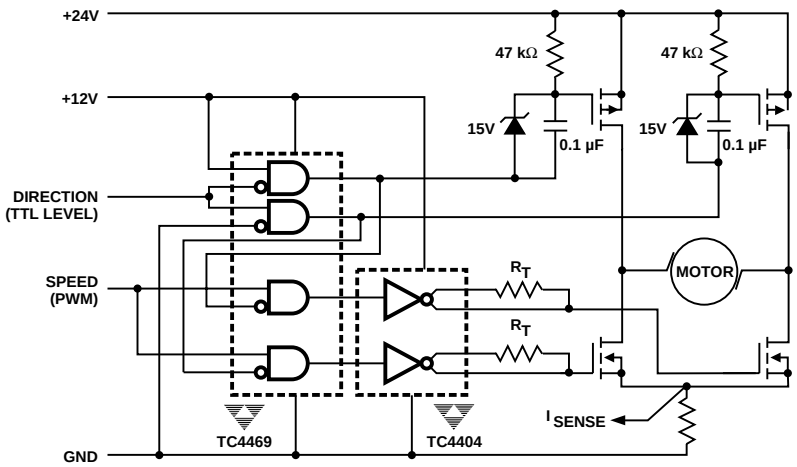
Zero Crossover Current Totem-Pole Switch



Driving Bipolar Transistors



Servo Motor Control



REACH-UP AND REACH-DOWN DRIVING