74VHCT174A

HEX D-TYPE FLIP FLOP WITH CLEAR

PRELIMINARY DATA

- HIGH SPEED:
  f_{MAX} =150 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS:
  V_{IH} = 2V (MIN), V_{IL} = 0.8V (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.8V (Max.)

ORDER CODES		
PACKAGE	**TUBE**	**T & R**
SOP	74VHCT174AM	74VHCT174AMTR
TSSOP		74VHCT174ATTR

DESCRIPTION

The 74VHCT174A is an advanced high-speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

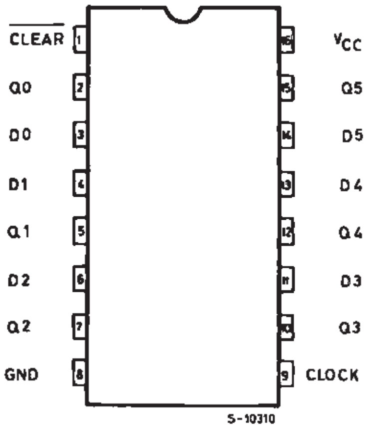
Information signals applied to D inputs are transfered to the Q outputs on the positive going edge of the clock pulse.

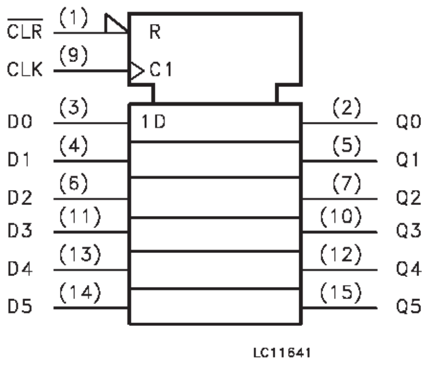
When the $\overline{\text{CLEAR}}$ input is held low, the Q outputs are held low independently of the other inputs.

Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

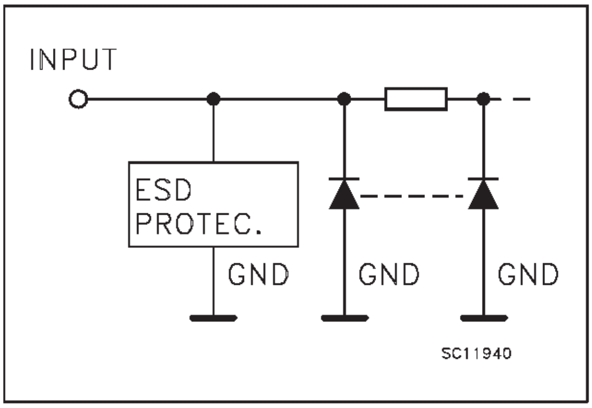
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

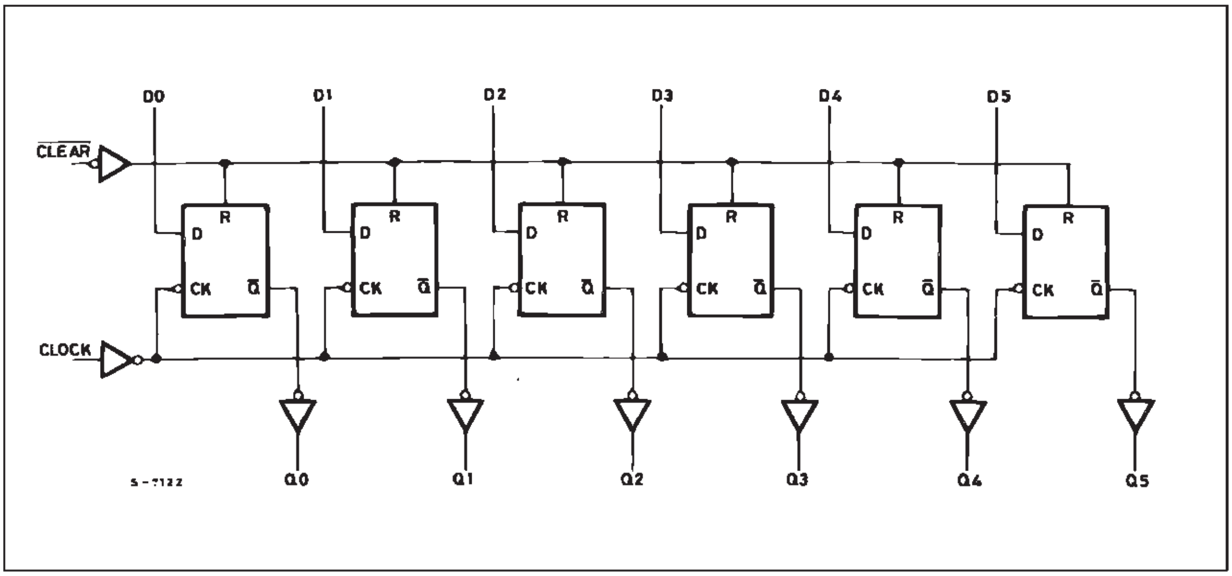
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asyncronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-Flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW-to-HIGH, Edge-Triggered)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLEAR}}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L	↑	L	
H	H	↑	H	
H	X	↓	Q_n	NO CHANGE

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 2)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) V_{CC}=0

2) High or Low State

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (see note 1)	0 to 5.5	V
V_O	Output Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 3) (V_{CC} = 5.0 ± 0.5V)	0 to 20	ns/V

1) V_{CC}=0

2) High or Low State

3) V_{IN} from 0.8V to 2 V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5		2			2		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	I_O=-50 µA	4.4	4.5		4.4		V
		4.5	I_O=-8 mA	3.94			3.8		
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.0	0.1		0.1	V
		4.5	I_O=8 mA			0.36		0.44	
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			4		40	µA
ΔI_{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V_{CC} or GND			1.35		1.5	mA
I_{OPD}	Output Leakage Current	0	V_{OUT} = 5.5V			0.5		5.0	µA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f =3 ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q	5.0(*)	15			7.2	11.0	1.0	13.0	ns
		5.0(*)	50			9.7	14.5	1.0	16.5	
t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Q	5.0(*)	15			7.4	11.4	1.0	13.5	ns
		5.0(*)	50			9.9	14.9	1.0	17.0	
t_W	$\overline{CLR}$ pulse Width LOW	5.0(*)					5.0		5.0	ns
t_W	CK pulse Width HIGH or LOW	5.0(*)					5.0		5.0	ns
t_s	Setup Time D to CK HIGH or LOW	5.0(*)					5.0		6.0	ns
t_h	Hold Time D to CK HIGH or LOW	5.0(*)					0.0		0.0	ns
t_{REM}	Removal Time $\overline{CLR}$ to CK	5.0(*)					3.0		3.0	ns
f_{MAX}	Maximum Clock Frequency	5.0(*)	15		95	150		80		MHz
		5.0(*)	50		55	85		50		

(*) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T_A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			4	10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)			29				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/6$ (per Flip-Flop)

DYNAMIC SWITCHING CHARACTERISTICS

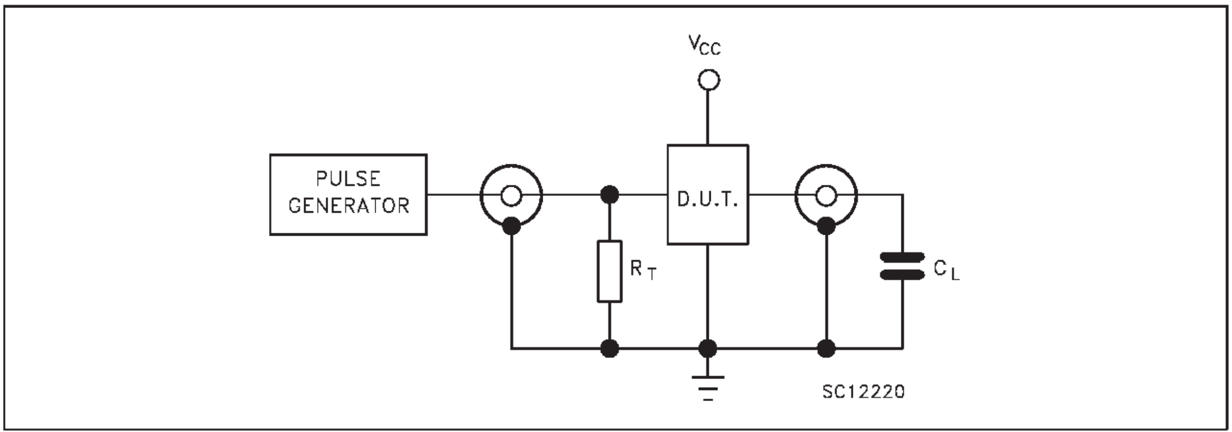
Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C_L = 50 pF		0.3	0.8			V
V_{OLV}				-0.8	-0.3				
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		2.0					
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				0.8			

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n -1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

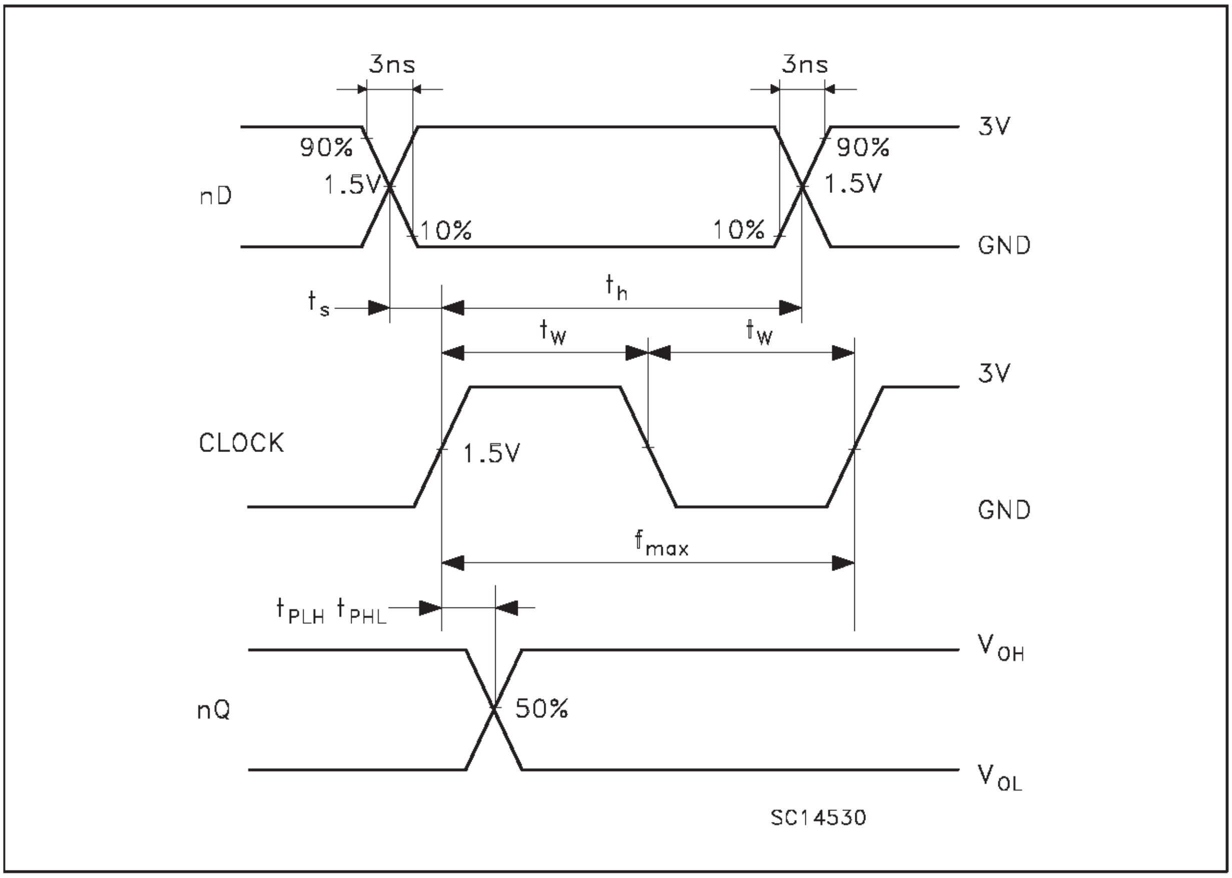
TEST CIRCUIT



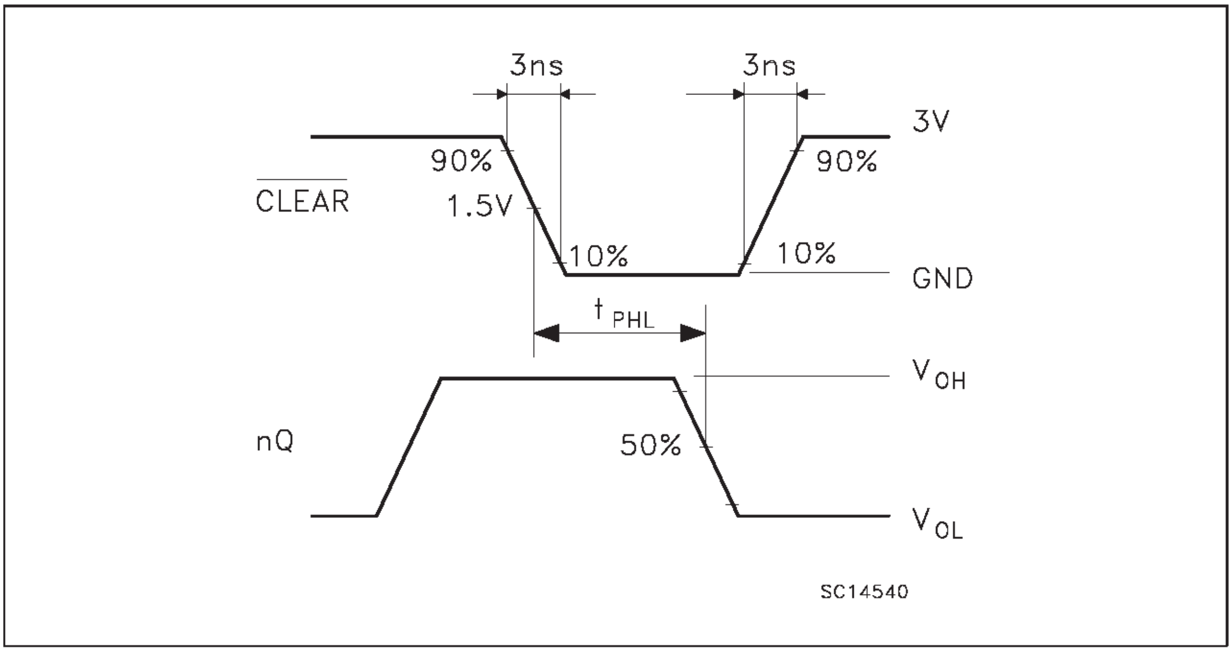
C_L = 15/50 pF or equivalent (includes jig and probe capacitance)

R_T = Z_{OUT} of pulse generator (typically 50Ω)

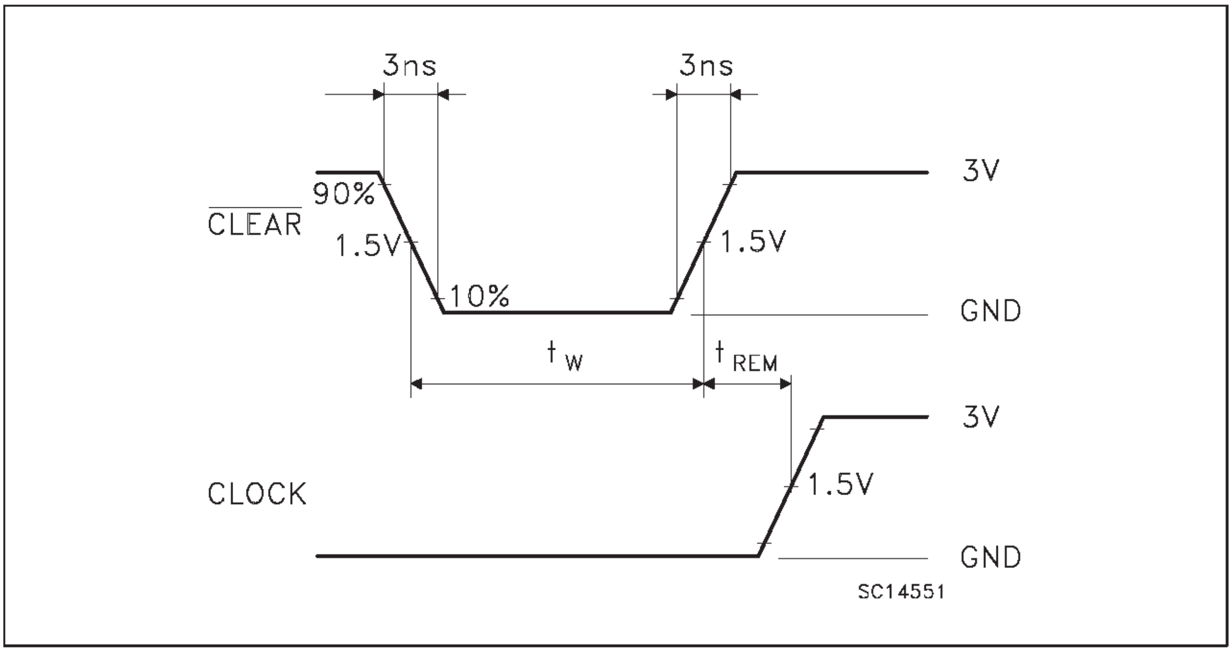
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

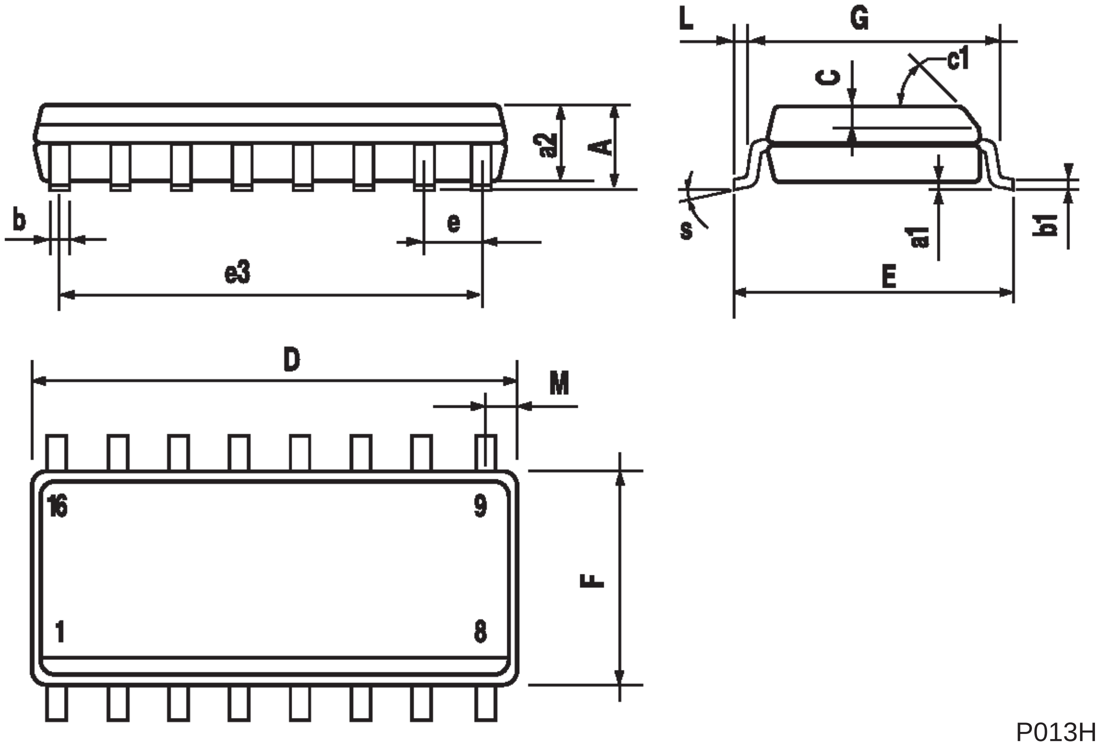


WAVEFORM 3: REMOVAL TIME (f=1MHz; 50% duty cycle)



SO-16 MECHANICAL DATA

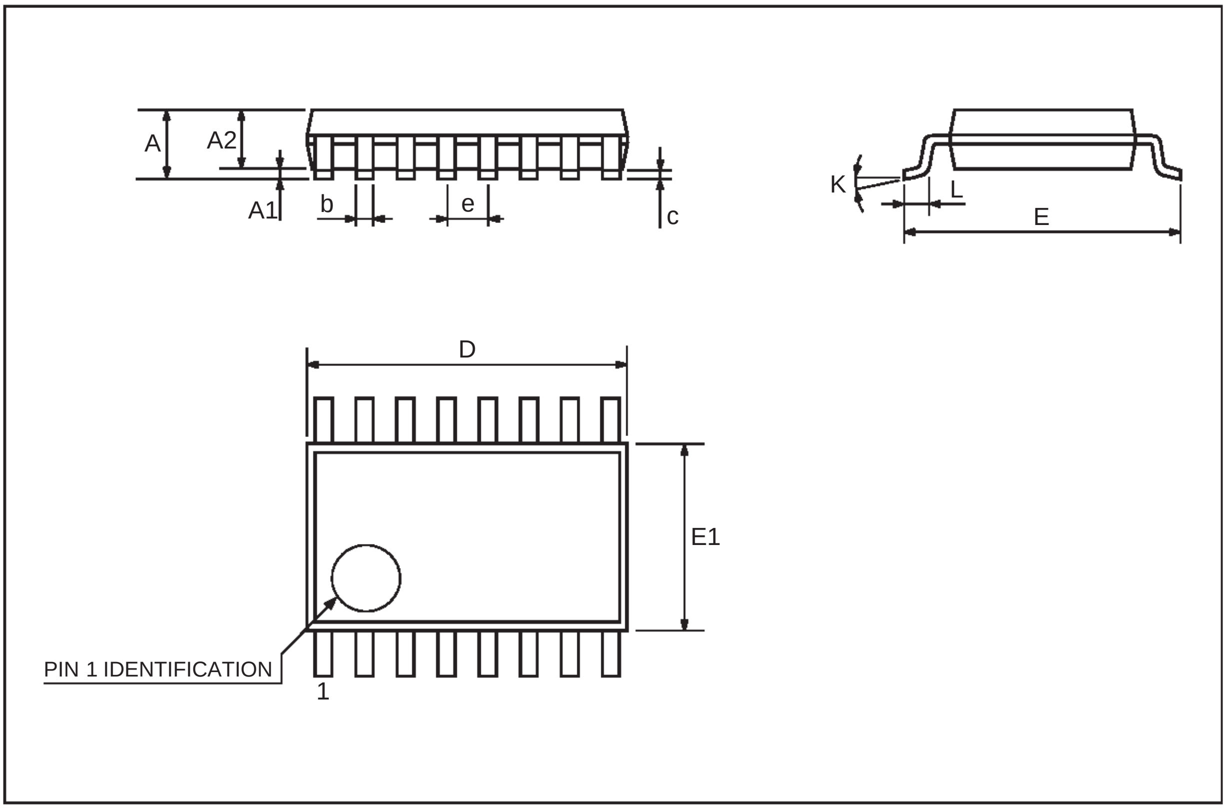
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



P013H

TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^{o}	4^{o}	8^{o}	0^{o}	4^{o}	8^{o}
L	0.50	0.60	0.70	0.020	0.024	0.028



STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com