SiI 201C Intelligent Panel Controller
PanelLink® Digital

March 1999

General Description

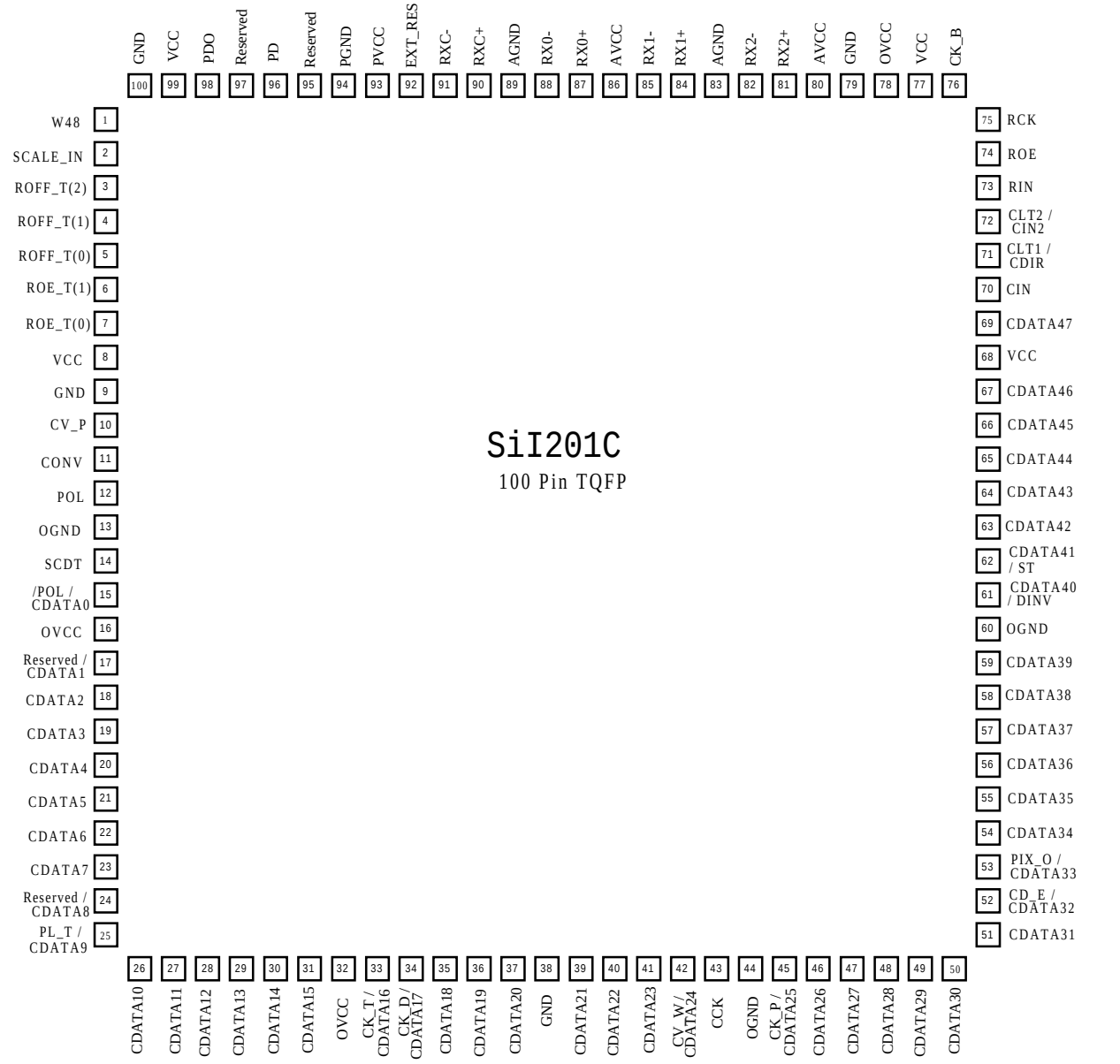
The SiI 201C Intelligent Panel Controller (IPC) uses PanelLink Digital technology to support displays ranging from VGA to XGA (25-68 MHz), which is ideal for LCD notebook and desktop monitor applications. With a flexible single or dual pixel out interface and selectable output drive, the SiI 201C IPC supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode. The SiI 201C is highly programmable to support multiple column and row drivers and to optimize display quality. PanelLink also features an inter-pair skew tolerance up to 1 full input clock cycle and a highly jitter tolerant PLL design.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

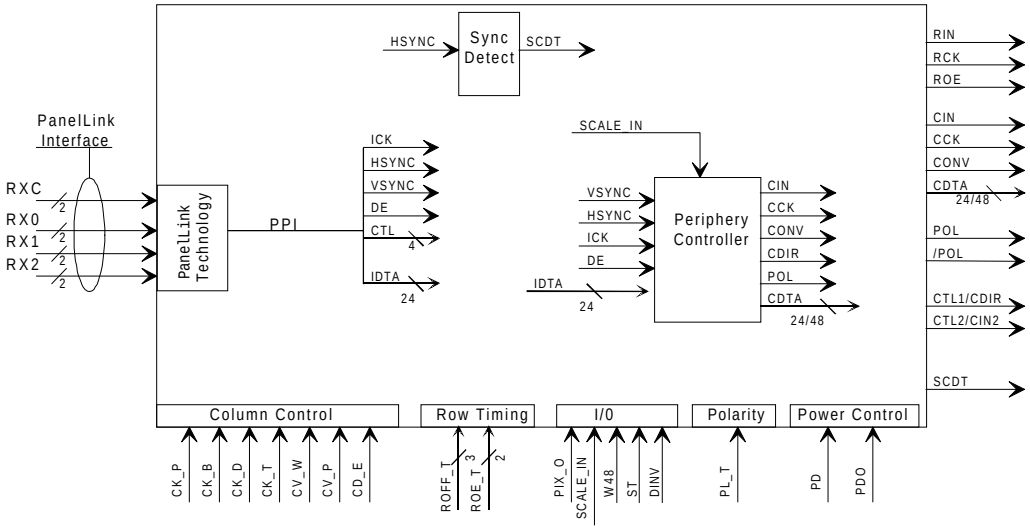
Features

- Scaleable Bandwidth: 25-68 MHz (VGA to XGA)
- Low Power: 3.3V core operation & power-down mode
- High Skew Tolerance: 1 full input clock cycle (15ns at 65 MHz)
- Highly programmable: supports multiple column drivers
- Sync Detect: for Plug & Display "Hot Plugging"
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI 201C Pin Diagram



Functional Block Diagram



The SiI 201C consists of four major blocks: the Functional PanelLink Interface, Sync Detection and the Row and Column Interface.

PanelLink ***Interface:*** The SiI 201C accepts the PanelLink interface of 4 low swing, differential input signals. One pair contains the pixel clock, the other three pairs are the serialized and encoded red, green and blue channels. Each of the color channels also contain two encoded control signals. The PanelLink technology de-serializes and decodes the input data to recover the original panel interface, labeled PPI in the block diagram. This interface is a one color pixel per clock interface at 24 bits per pixel, the recovered input clock is ICK.

Column Interface(CIN, CCK, CONV, CDTA): The column interface block is programmed so that the column drive outputs are set to match the desired column drivers. By programming the pins CK_P, CK_B, CK_D, CK_T, CV_W, CV_P, PL_T and DINV a wide variety of column drivers can be addressed.

Row Interface(RIN, RCK, ROE): The row driving signals are output from this block. While the row signals require no programmability, their timing with respect to the column drive signals is critical, and varies with panel size and processing parameters. Sufficient time must be allowed for the row select signals to be fully switched off before the column driver's analog outputs are allowed to change. This time T_{OFF}, can be set over a wide range of values through the ROFF_T[2:0] programming input bits. If the row driver chosen has an output enable, the width of the output enable pulse can be set using ROE_T[1:0].

Sync Detect: This block monitors the state of HSYNC. If HSYNC becomes inactive the output signal SCDT will be set low. This signal can be used to control driver and backlight supplies enabling panel protection and power savings.

Absolute Maximum Conditions

Note: Permanent device damage may occur if absolute maximum conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	-0.3	-	6.0	V
V_I	Input Voltage	-0.3	-	V_{CC} + 0.3	V
V_O	Output Voltage	-0.3	-	V_{CC} + 0.3	V
T_A	Ambient Temperature (with power applied)	-25	-	85	°C
T_{STG}	Storage Temperature	-40	-	125	°C
P_{PD}	Package Power Dissipation	-	-	1	W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

Note: [1] Guaranteed by design.

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA

Note: [1] Guaranteed by design.

DC Specifications

Under normal operating conditions unless otherwise specified. Low drive strength values, when ST=0, are shown in brackets.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OH}	(ST=0) Output High Drive (**CCK**) (ST=1)	$V_{OUT} = V_{OH}$	6 15	8 16.5	10.5 35	mA
I_{OL}	(ST=0) Output Low Drive (**CCK**) (ST=1)	$V_{OUT} = V_{OL}$	-8.5 -19	-12 -24	-15.4 -27	mA
I_{OH}	(ST=0) Output High Drive (**All Others**) (ST=1)	$V_{OUT} = V_{OH}$	4 9	5.5 11	7 22	mA
I_{OL}	(ST=0) Output Low Drive (**All Others**) (ST=1)	$V_{OUT} = V_{OL}$	-5.6 -9	-8 -16	-10 -11	mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		250		1000	mV
I_{PD}	Power-down Current[1]		-	50 uA	1 mA	
I_{PDL}	Output leakage current to ground in high impedance mode (PD, PDO = LOW)				10	uA
I_{CCR}	Supply Current @ 3.3V V_{CC} Output is one pixel per clock mode.[2]	DLCK = 65 MHz C_{LOAD} = 10pF R_{EXT_SWING} = 680 Ω Typical Pattern[3]	-	137	157	mA
		DCLK = 65 MHz C_{LOAD} = 10pF R_{EXT_SWING} = 680 Ω Worst Case Pattern[4]	-	153	185	mA

Notes:
[1] The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.
[2] For worst case I/O power consumption.
[3] The Typical Pattern contains a gray scale area, checkerboard area, and text.
[4] Black and white checkerboard pattern, each checker is one pixel wide.

AC Specifications

Under normal operating conditions unless otherwise specified. Low drive strength values, when ST=0, are shown in brackets.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew				200	ps
T_{CCS}	Channel to Channel Differential Input Skew				T_{CIP}	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[1,2]				2	ns
D_{LHT}	Low-to-High Transition Time: Data and Controls	ST=1 [ST=0] C_L = 10pF [5pF]			1.9 [1.9]	ns
	CCK				1.6 [1.4]	
D_{HLT}	High-to-Low Transition Time: Data and Controls	ST=1 [ST=0] C_L = 10pF [5pF]			1.6 [1.6]	ns
	CCK				1.4 [1.2]	
T_{SOF}	Data/Control Setup Time to CCK: [4] 65 MHz, One Pixel / Clock, PIXS = 0	ST=1 [ST=0] C_L = 10pF [5pF] CK_T = 0	6.0 [5.8]			ns
		ST=1 [ST=0] C_L = 10pF [5pF] CK_T = 1	1.8 [2.1]			ns
T_{HOF}	Data/Control Hold Time to CCK : [4] 65 MHz, One Pixel / Clock, PIXS = 0	ST=1 [ST=0] C_L = 10pF [5pF] CK_T = 0	4.9 [4.5]			ns
		ST=1 [ST=0] C_L = 10pF [5pF] CK_T = 1	8.9 [9.0]			ns
R_{CIP}	CCK Cycle Time (1 pixel/clock)		14.7		50	ns
F_{CIP}	CCK Frequency (1 pixel/clock)		20		68	MHz
R_{CIP}	CCK Cycle Time (2 pixels/clock)		29.4		100	ns
F_{CIP}	CCK Frequency (2 pixels/clock)		10		34	MHz
R_{CIH}	CCK High Time 65 MHz, One Pixel / Clock, PIXS = 0 [3]	ST=1 [ST=0] C_L = 10pF [5pF]	5.3 [4.9]			ns
R_{CIL}	CCK Low Time 65 MHz, One Pixel / Clock, PIXS = 0 [3]	ST=1 [ST=0] C_L = 10pF [5pF]	6.9 [6.7]			ns
T_{HSC}	Link disabled (HSYNC inactive) to SCDT low				50	ms
T_{FSC}	Link enabled (HSYNC active) to SCDT high				2	ms
T_{PDL}	Delay from PD/ PDO Low to high impedance outputs				8	ns

Notes:
1. Jitter can be estimated by: 1) triggering a digital scope at the rising of input clock, and 2) measuring the peak to peak time spread of the rising edge of the input clock 1µs after the trigger.
2. Actual jitter tolerance may be higher depending on the frequency of the jitter.
3. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
4. The setup and hold timing for the data and controls is measured relative to CCK rising edge.

1.1 Data Bus Mapping

Pin #	Name	18-bpp 1-pixel/clock	24-bpp 1-pixel/clock	36-bit 2-pixel/clock	48-bit 2-pixel/clock
15	CDATA0				B0/E
17	CDATA1				B1/E
18	CDATA2	B0	B2	B0/E	B2/E
19	CDATA3	B1	B3	B1/E	B3/E
20	CDATA4	B2	B4	B2/E	B4/E
21	CDATA5	B3	B5	B3/E	B5/E
22	CDATA6	B4	B6	B4/E	B6/E
23	CDATA7	B5	B7	B5/E	B7/E
24	CDATA8				G0/E
25	CDATA9				G1/E
26	CDATA10	G0	G2	G0/E	G2/E
27	CDATA11	G1	G3	G1/E	G3/E
28	CDATA12	G2	G4	G2/E	G4/E
29	CDATA13	G3	G5	G3/E	G5/E
30	CDATA14	G4	G6	G4/E	G6/E
31	CDATA15	G5	G7	G5/E	G7/E
33	CDATA16				R0/E
34	CDATA17				R1/E
35	CDATA18	R0	R2	R0/E	R2/E
36	CDATA19	R1	R3	R1/E	R5/E
37	CDATA20	R2	R4	R2/E	R4/E
39	CDATA21	R3	R5	R5/E	R5/E
40	CDATA22	R4	R6	R4/E	R6/E
41	CDATA23	R5	R7	R5/E	R7/E
42	CDATA24				B0/O
45	CDATA25				B1/O
46	CDATA26		B0	B0/O	B2/O
47	CDATA27		B1	B1/O	B3/O
48	CDATA28		G0	B2/O	B4/O
49	CDATA29		G1	B3/O	B5/O
50	CDATA30		R0	B4/O	B6/O
51	CDATA31		R1	B5/O	B7/O
52	CDATA32				G0/O
53	CDATA33				G1/O
54	CDATA34			G0/O	G2/O
55	CDATA35			G1/O	G3/O
56	CDATA36			G2/O	G4/O
57	CDATA37			G3/O	G5/O
58	CDATA38			G4/O	G6/O
59	CDATA39			G5/O	G7/O
61	CDATA40				R0/O
62	CDATA41				R1/O
63	CDATA42			R0/O	R2/O
64	CDATA43			R1/O	R3/O
65	CDATA44			R2/O	R4/O
66	CDATA45			R3/O	R5/O
67	CDATA46			R4/O	R6/O
69	CDATA47			R5/O	R7/O

Legend :

1. R = RED Channel, G = GREEN Channel, B = BLUE Channel.
2. /E = EVEN (first) pixel data (P0, P2, P4, etc.)
3. /O = ODD (second) pixel data (P1, P3, P5, etc.)

Assumptions on how `PanelLink` is connected :

1. Bits 7:0 mapped MSB:LSB.
2. Tx0/Rx0 transmits BLUE (B) data.
3. Tx1/Rx1 transmits GREEN (G) data.
4. Tx2/Rx2 transmits RED (R) data

2. Input Timing

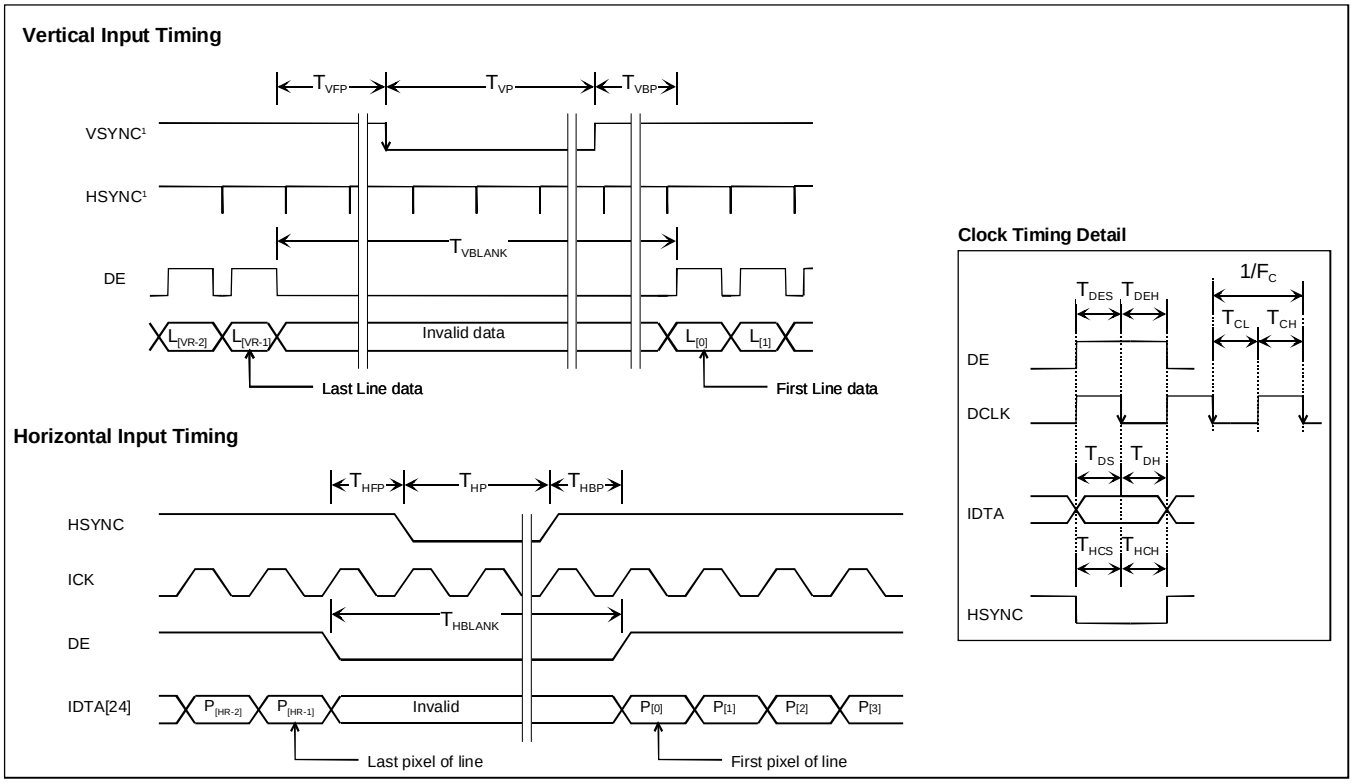


Figure 1: Input Timing Diagram

Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
DCLK	Pixel clock frequency	$F_C = 1/T_C$	30	65		MHz	
	Low time	T_{CL}	5			ns	
	High Time	T_{CH}	5			ns	
VSYNC	Pulse width	T_{VP}	1	2		HSYNC	
	Vertical front porch	T_{VFP}	0	4		HSYNC	
	Vertical back porch	T_{VBP}	0	1		HSYNC	
HSYNC	Pulse width	T_{HP}	2	32		DCLK	
	Horizontal front porch	T_{HFP}	0	144		DCLK	
	Horizontal back porch	T_{HBP}	0	1		DCLK	
IDATA	IDATA to ICK↓ setup time	T_{DS}					1
	IDATA to ICK↓ hold time	T_{DH}					1
	HSYNC to ICK↓ setup time	T_{HCS}					2
	HSYNC to ICK↓ hold time	T_{HCH}					2
DE	DE↑ to ICK↓ setup time	T_{DES}					2
	DE↓ to ICK↓ hold time	T_{DEH}					2

Table 1: Input Timing Table

Notes:

1. HSYNC and VSYNC can be of either polarity, and their polarities are independent of each other.
2. Actual times will be set by the decoding logic. It is assumed that input data is latched on the falling edge of ICK.
3. Actual times will be set by the decoding logic. It is assumed that HSYNC and DE are latched by the falling edge of ICK.

3. Output Timing

3.1 Timing Overview

Frame Start/End Timing Overview

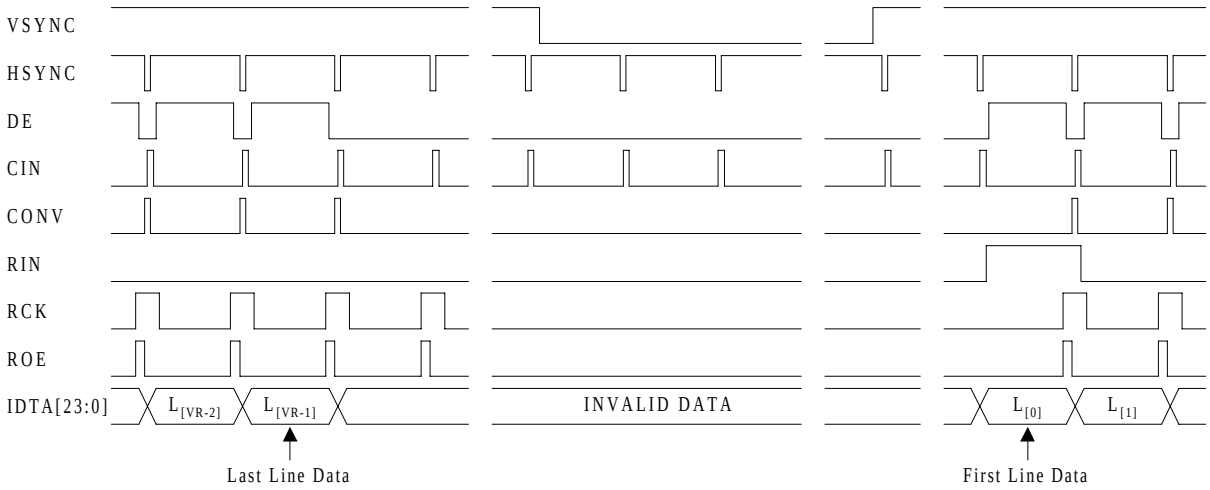


Figure 2: General timing diagram for frame start and end

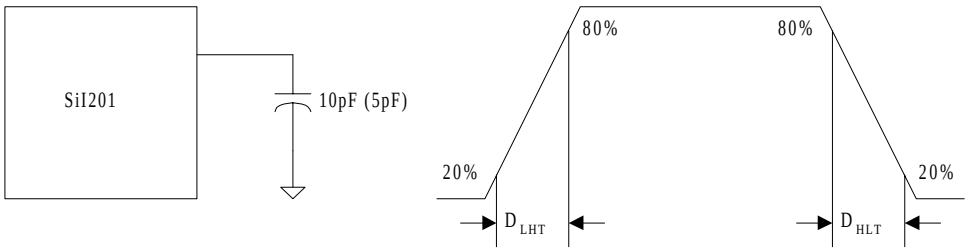


Figure 3: Digital output transition time

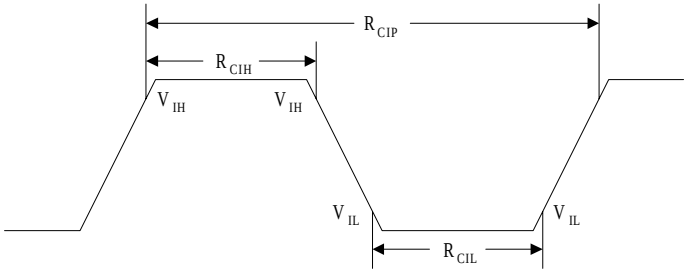


Figure 4:Receiver Clock Cycle/High/Low Times

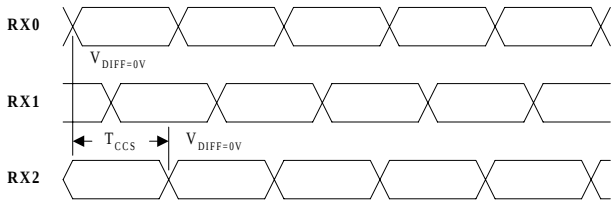


Figure 5:Channel-to-Channel Skew Timing

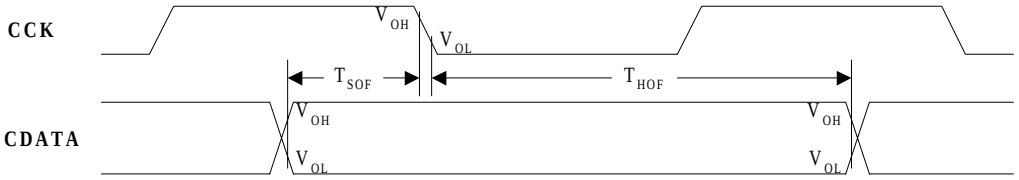


Figure 6: Output Data Setup/Hold Times to ODCK

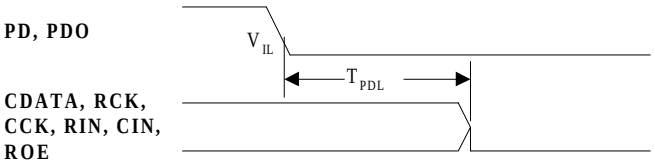


Figure 7: Output Signals Disabled Timing from PD Active

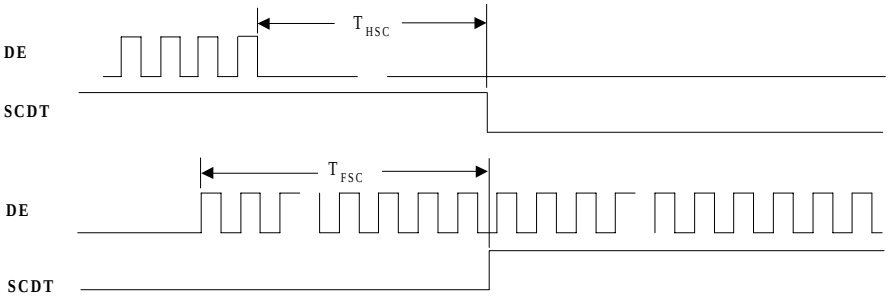


Figure 8: SCDT Timing from DE Inactive/Active

3.2 CCK/CIN/CDTA Timing

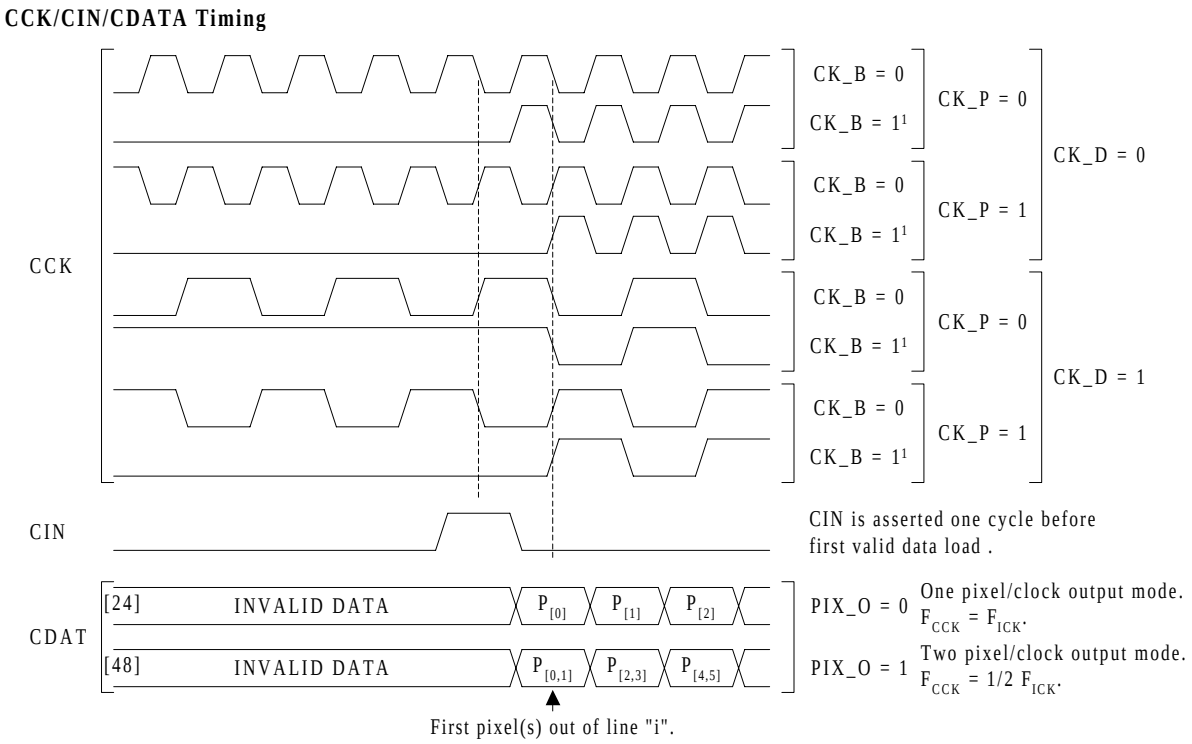


Figure 9: CCK/CIN/CDTA Timing Diagram

Notes:

1. In blanked (controlled) clock mode, there are **four extra load clock** cycles at the end of a data load period. These provide “dummy” load cycles for column drivers that require internal pipelines to be emptied for proper operation.

3.3 CONV/POL Timing

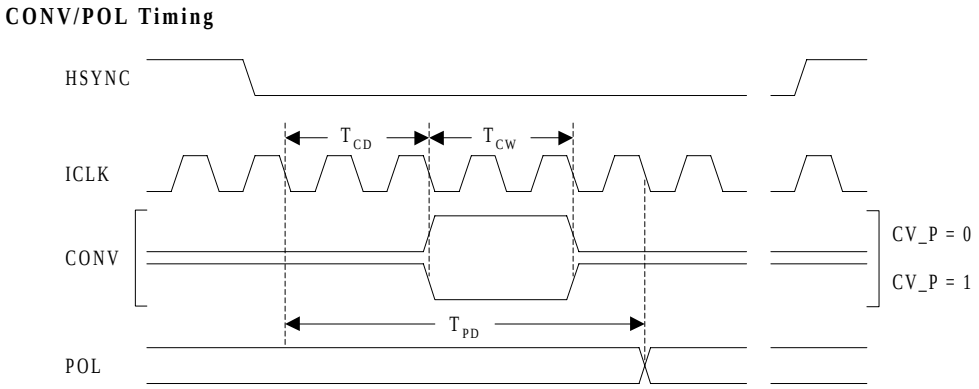


Figure 10: CONV/POL Timing Diagram

Signal	Parameter	Symbol	Value	Program Pin	Note
CONV	CONV start time	T_{CD}	$4*T_{SYNC}$	-	1
	CONV pulse width	T_{CW}	$6* T_{SYNC}$ $48* T_{SYNC}$	CV_W = 0 CV_W = 1	1, 2
POL	POL start time	T_{PD}	0 $T_{CD}+T_{CW}+4*T_{SYNC}$	PL_T = 0 PL_T = 1	1, 3

Table 2: CONV/POL Timing Table

Notes:

1. The time T_{SYNC} varies according to the setting of the SCALE_IN input.

   For SCALE_IN=0, $T_{SYNC} = T_C$ For SCALE_IN=1, $T_{SYNC} = 2*T_C$

2. Some column drivers that support on-chip inversion schemes require a wide conversion pulse. By setting input CV_W to the HIGH state, conversion pulses greater than 1µs in width can be obtained.

3. The POL output signal can be used to control the LC polarity switching. Programming input pin PL_T sets the polarity signal to switch before or after the conversion pulse, as shown above.

3.4 Polarity Inversion Timing

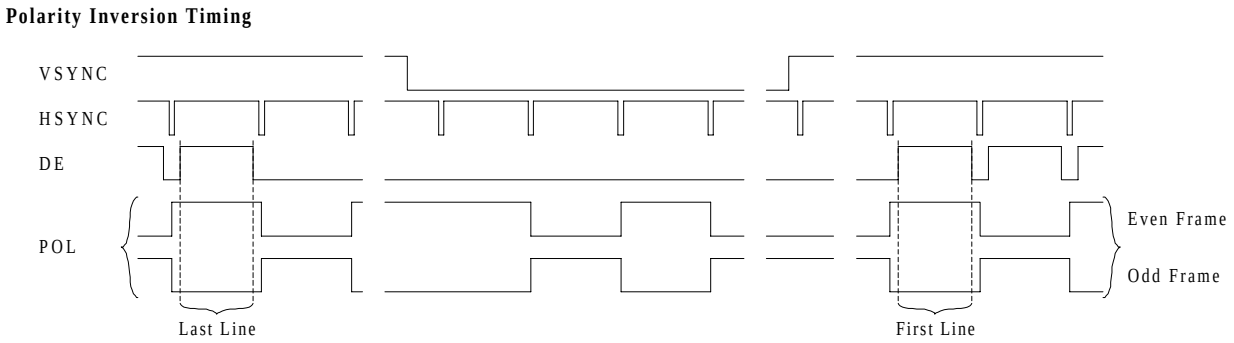


Figure 11: Polarity Inversion Timing Diagram

3.5 RCK to CONV Timing

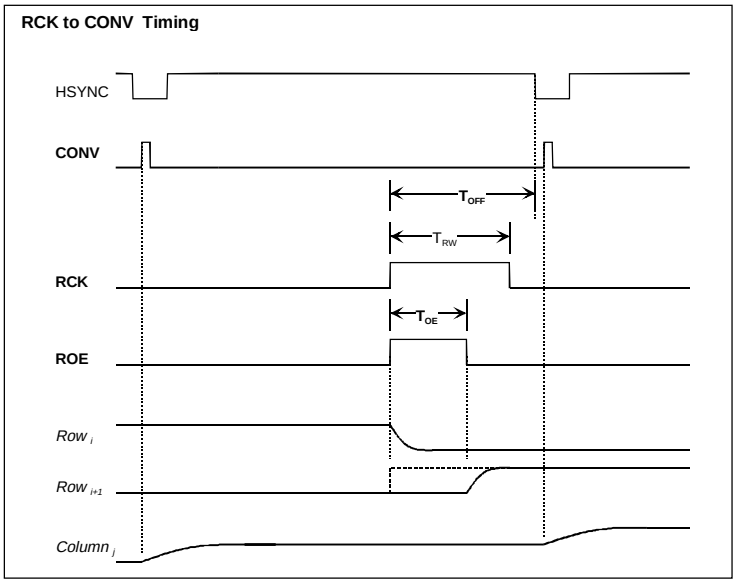


Figure 12: RCK to CONV Timing Diagram

Signal	Parameter	Symbol	Value	Program Pin	Note
RCK	Row clock pulse width.	T_{RW}	255* T_{SYNC}	-	1
	Row off time. TOFF is approximately the time between when the next row is selected to when the column data is allowed to change.	T_{OFF}	 64*T_{SYNC} 80*T_{SYNC} 96*T_{SYNC} 112*T_{SYNC} 128*T_{SYNC} 176*T_{SYNC} 240*T_{SYNC} Reserved	ROFF_T = 000 001 010 011 100 101 110 111	1, 2
ROE	Row blank time.	T_{OE}	 64* T_{SYNC} 96* T_{SYNC} 112* T_{SYNC} 128* T_{SYNC}	ROE_T = 00 01 10 11	1, 3

Table 3: RCK to CONV Table

Notes:

1. The time T_{SYNC} varies according to the setting of the SCALE_IN input.

   For SCALE_IN=0, $T_{SYNC} = T_C$ For SCALE_IN=1, $T_{SYNC} = 2*T_C$

2. T_{OFF} is the time from when the next row is selected (RCK), to when the column out changes (CONV). Input signal ROFF_T[2:0] is used to program the delay.

T_{OE} is the pulse width of ROE. For most row drivers when ROE is HIGH all of the row output select signals are LOW. The width of this blank period is controlled with ROE_T[1:0].

3.6 W48 Mode

When pin 1 (W48) is set HIGH, W48 mode is asserted and the data path is set to 48 bit output. With W48 is asserted, the SiI 201C outputs two 24 bit pixels per clock cycle. In this mode, some of the programming pins (CK_P, DINV, ST, PIX_O, CK_D, CK_T, CV_W, CD_E) are no longer accessible because they are used to output the extra 12 bits of data (also see Configuration Pin Description table on page 16). The internal state of these programming pins in W48 mode is shown in the table below.

Pin Name	Pin #	Description	Pin State During W48 Mode	Description of State
CIN	70	Column Shift Register Start Bit	-	CIN pulse is **always** one output clock cycle before the first data load, even when W48 is low.
ST	62	Output Drive Strength	ST = 1	Output drive strength is high
PIX_0	53	Output Pixel Select	PIX_0 = 1	Two 24 bit pixels are output per clock
CK_D	34	Dual Edge Clocking	CK_D = 0	Dual edge clocking is off
CK_T	33	Column Clock Timing	CK_T = 0	Clock to data setup and hold timings are symmetrical
CV_W	42	Conversion Pulse Width	CV_W = 0	Conversion pulse width is narrow

Table 4: Programming Pin Values During W48 Mode

In W48 mode, the programming pin CV_P (CONV Pulse Polarity) selects the Clock Inversion mode (to latch data on the rising or falling clock edge) and Data Inversion mode. The table below describes how CV_P configures these modes.

CONV Pulse Polarity Setting Pin 10	**Data Latching Edge**	**Data Inversion Mode**
CV_P = 0 • CONV set to positive polarity • NEC/TI mode	• Output data latched on rising clock edge	• Output data is not inverted
CV_P = 1 • CONV set to negative polarity • Vivid mode	• Output data latched on falling clock edge	• Output data is inverted

Note: In W48 mode, CV_P = 0 selects NEC/TI mode. CV_P = 1 selects Vivid mode.

Table 5: CONV Pulse Polarity Configuration for Clock & Data Inversion

Output Pin Description

Pin #	Pin Name	Type	Description
69	CDTA47	Out	Output Data/Programming pins 47-0.
67	CDTA46		Output data is synchronized with output data clock (CCK).
66	CDTA45		
65	CDTA44		**See the "Data Bus Mapping" table to see how pixel data is mapped in**
64	CDTA43		**24/36/48 bit mode.**
63	CDTA42		
62	CDTA41[1,2]		**Pin Notes:**
61	CDTA40[1,2]		[1.] Only available for data output if W48 is HIGH.
59	CDTA39		[2.] This data pin is shared with a programming pin, the programming pin is
58	CDTA38		accessible when W48 is LOW.
57	CDTA37		
56	CDTA36		
55	CDTA35		
54	CDTA34		
53	CDTA33[1,2]		
52	CDTA32[1,2]		
51	CDTA31		
50	CDTA30		
49	CDTA29		
48	CDTA28		
47	CDTA27		
46	CDTA26		
45	CDTA25[1,2]		
42	CDTA24[1,2]		
41	CDTA23		
40	CDTA22		
39	CDTA21		
37	CDTA20		
36	CDTA19		
35	CDTA18		
34	CDTA17[1,2]		
33	CDTA16[1,2]		
31	CDTA15		
30	CDTA14		
29	CDTA13		
28	CDTA12		
27	CDTA11		
26	CDTA10		
25	CDTA9[1,2]		
24	CDTA8[1]		
23	CDTA7		
22	CDTA6		
21	CDTA5		
20	CDTA4		
19	CDTA3		
18	CDTA2		
17	CDTA1[1]		
15	CDTA0[1,2]		

Output Pin Description (continued)

Pin #	Pin Name	Type	Description
43	CCK	Out	Column driver load clock. Valid column driver data (CDTA) is loaded by this clock into the column drivers. This clock is programmable.
70	CIN	Out	Column shift register start bit. If CD_E is low, this signal starts the loading of the column shift registers. If mirroring is enabled (CD_E=1), CIN will output the column shift register start bit when CTL1=0, and will be tri-stated when CTL1 = 1. See pin CTL1/CIN2.
11	CONV	Out	Column transfer signal. This signal is used to transfer data in the column driver storage registers to the driver's analog outputs.
75	RCK	Out	The row clock. Each rising edge shifts the row shift register one bit.
73	RIN	Out	Row shift register start bit. Provides an input bit to the row shift register to start a vertical scan.
74	ROE	Out	Output enable for the row drivers. For most row drivers, when ROE is low row outputs are enabled, when ROE is high all row outputs are held low.
12	POL	Out	The polarity control signal. This signal controls the polarity switching circuits that minimize the DC bias across the liquid crystal.
15	/POL	Out	Inverted POL control signal. **This pin is only accessible when W48 is LOW.**
71	CTL1/CDIR	Out	General output control signal 1. If mirroring is enabled (CD_E=1), CTL1 dynamically selects the direction of the column driver shift register by alternately sending the shift register output bit between outputs CIN and CIN2. The CTL1 output is then used for the direction input to the column drivers. In W48=1 mode, the VSYNC signal comes out of this pin.
72	CTL2/CIN2	Out	General output control signal 2. If mirroring is enabled (CD_E=1) CIN2 will output the column driver start bit when CTL1=1, and will be tri-stated when CTL1=0.

Configuration Pin Description

Pin #	Pin Name	Type	Description
3 4 5	ROFF_T[2] ROFF_T[1] ROFF_T[0]	In	Row Off Timing. Selects the time interval between row clock and column output transitions.
6 7	ROE_T[1] ROE_T[0]	In	Row Output Enable Pulse. Selects the time that the row output is blanked.
25	PL_T	In	Polarity Timing. If low the polarity bit is toggled before the CONV signal is asserted. If high the polarity bit is toggled after the CONV pulse. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set LOW.**
61	DINV	In	Output data inversion. When this pin is tied LOW the output data (CDTA) bits are not inverted. When it is tied HIGH the output data is inverted. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set HIGH.**
62	ST	In	Output drive strength. When this pin is tied LOW it sets the data and clock outputs of the SiI 201C for low drive strength. When it is tied high, the outputs are at maximum drive strength. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set HIGH.**
53	PIX_O	In	Output Pixel Select option. A low level indicates that output data is one pixel (24-bits) per clock and a high level indicates two pixels (36/48-bits) per clock. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set HIGH.**
1	W48	In	Select 48 bit output mode. When this pin is set LOW the data output is set for 36 bit mode. In this mode many of the programming pins are accessible. When this pin is set HIGH the data path is set to 48 bit output. In this mode the programming pins that were previously accessible are set to their default state. See "*Section 3.6: W48 Mode*."
45	CK_P	In	Output Clock Polarity. If CK_P = 0 the output clock latches data on the negative edge, if CK_P = 1, the output data is latched on the positive edge. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set LOW.**
76	CK_B		Output Clock Blank enable. If high the output clock is blanked between valid data loads.
34	CK_D		Dual Edge Clocking. When this signal is HIGH the column clock latches column data on both clock edges, halving the frequency of the column clock. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set LOW.**
33	CK_T		Column Clock Timing. When this signal is LOW the output setup and hold time is nearly symmetric. When HIGH, the minimum hold time is long. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set LOW.**
42	CV_W	In	Conversion Pulse Width. If low the CONV pulse is set to minimum width, if high the conversion pulse is set to the maximum width. **This pin is only accessible when W48 is LOW. When W48 is HIGH, this pin is internally set LOW.**
10	CV_P		Conversion Pulse Polarity. If low the conversion pulse is active high, if high the conversion pulse is active low.
52	CD_E	In	Enable Software Mirroring. If low, software switching is disabled. If high the direction of the column driver loading is set according to the state of CTL1 of SiI100 transmitter. **This pin is only accessible when W48 is LOW. When W48 is HIGH this pin is internally set LOW.**
2	SCALE_IN	In	Timing Scale. If SCALE_IN is low, preset timing registers are not scaled. If SCALE_IN is high timing registers are scaled by a factor of two.

Power Management Pin Description

Pin #	Pin Name	Type	Description
14	SCDT	Out	Sync Detect. Output is high if HSYNC is active. If the HSYNC signal is not detected then SCDT is driven low. SCDT can be externally connected to PD/O pin. In this configuration, all data (CDTA[47:0]), general output control signals, and row and column outputs are driven low when SCDT is low.
96	PD	In	Power Down mode (active low). A high level indicates normal operation and a low level indicates power down mode. During power down mode, all data (CDTA[47:0]), general output control signals, and row and column outputs are driven low. The internal clock is also stopped and all analog logic is powered down. This pin is effective during both normal operation and test modes.
98	PDO	In	Output driver Power Down mode (active low). A high level indicates normal operation and a low level indicates output driver power down mode. During power down mode, all data (CDTA[47:0]), general output control signals, and row and column outputs are driven low. If the operation of SCDT signal is verified, PD/O can be externally connected to SCDT. In this configuration, all data (CDATA[47:0]), general output control signals, and row and column outputs are driven low when SCDT is low.

Differential Signal Data Pin Description

Pin #	Pin Name	Type	Description
87 88 84 85 81 82	RX0+ RX0- RX1+ RX1- RX2+ RX2-	Analog	Low voltage swing differential input data pairs.
90 91	RXC+ RXC-	Analog	Low voltage swing differential input clock pair.
92	EXT_RES	Analog	Impedance Matching Control. Resistor value should be ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 500Ω resistor must be connected between AVCC and this pin.

Reserved Pin Description

Pin #	Pin Name	Type	Description
17	RESERVED	In	This pin should be left unconnected. If connected, it must be connect HIGH.
24	RESERVED	In	This pin should be left unconnected when W48 is LOW. If connected, it must be connect LOW.
95	RESERVED	In	This signal must be tied high (3.3V) for normal operation.
97	RESERVED	Out	This pin should be left unconnected.

Power and Ground Pin Description

Pin #	Pin Name	Type	Description
86 80	AVCC AVCC	Power	Receiver Analog VCC.
83 89	AGND AGND	Ground	Receiver Analog GND.
93	PVCC	Power	PLL Analog VCC.
94	PGND	Ground	PLL Analog GND.
8 68 99 77	VCC VCC VCC VCC	Power	Core VCC. This pin supplies power for input buffers and the core digital logic and must be set to 3.3 V.
9 38 79 100	GND GND GND GND	Ground	Digital GND
16 32 78	OVCC OVCC OVCC	Power	Output VCC. This OVCC pin supplies power for output buffers and for input pin protection devices. This pin must be set to 5 V if output signals are at 5 V and can be set to 3.3 V if output signals are at 3.3 V.
13 44 60	OGND OGND OGND	Ground	Output GND. This OGND is for output buffers and for input pin protection devices. This OGND pin is separated from the digital GND pin for isolating the noisy output GND from the clean core digital GND.

Application Information

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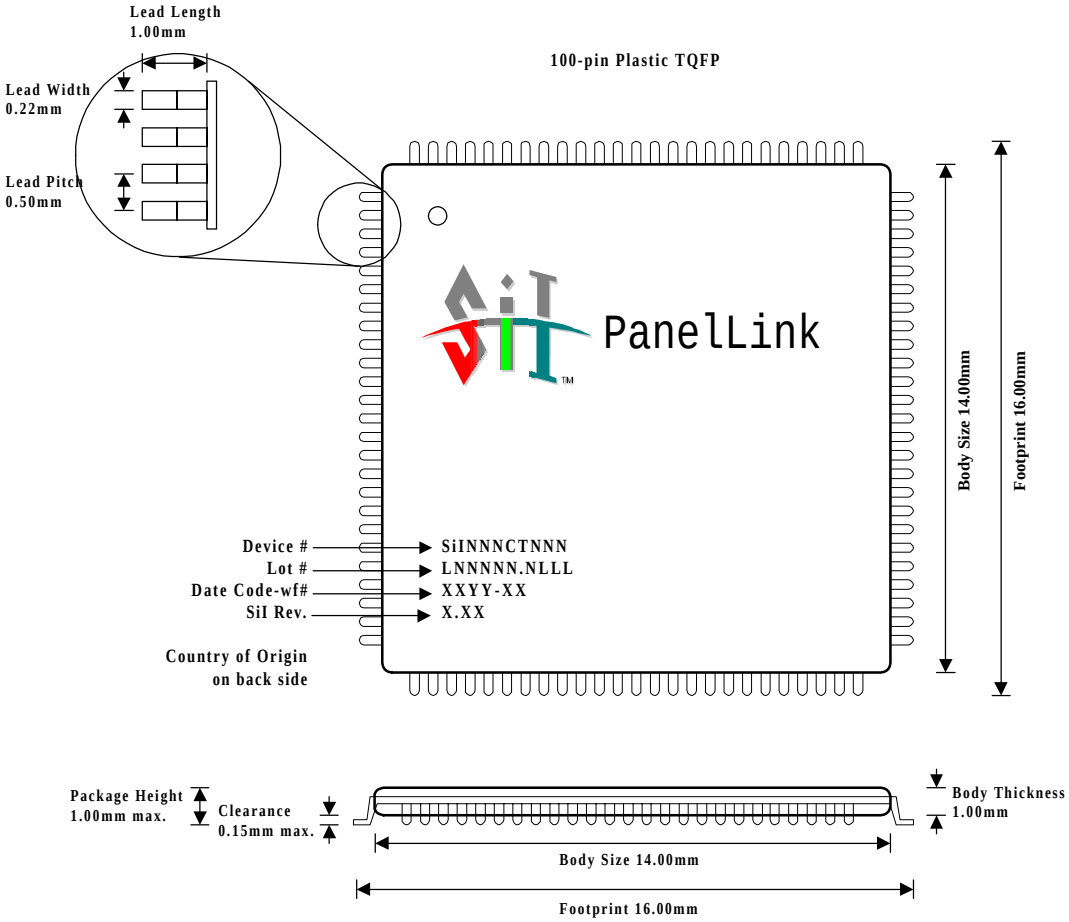
Package Dimensions

100-pin TQFP Package Dimensions



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