General Description

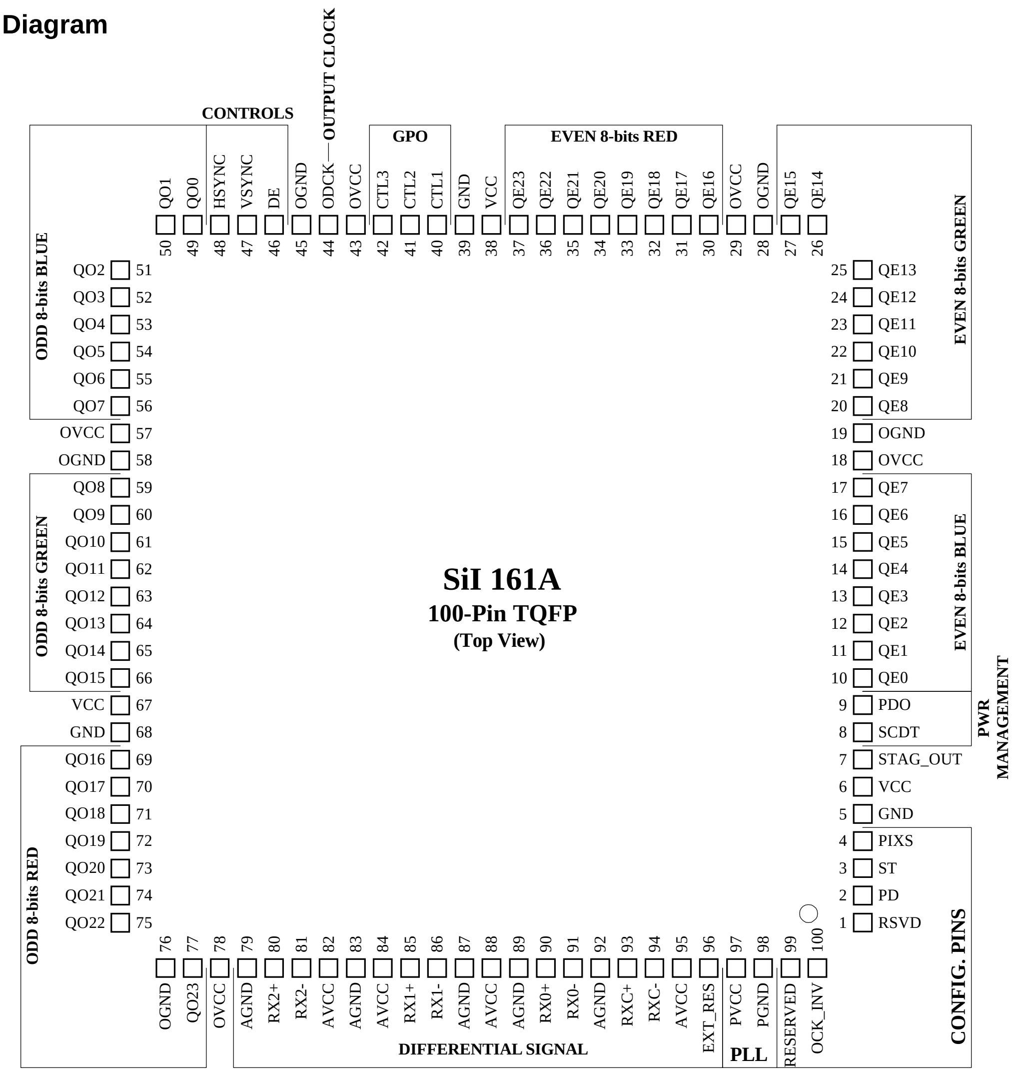
The SiI 161A receiver uses PanelLink Digital technology to support high resolution displays up to UXGA. The SiI 161A receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode. In addition, the receiver data output is time staggered to reduce ground bounce that affects EMI. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

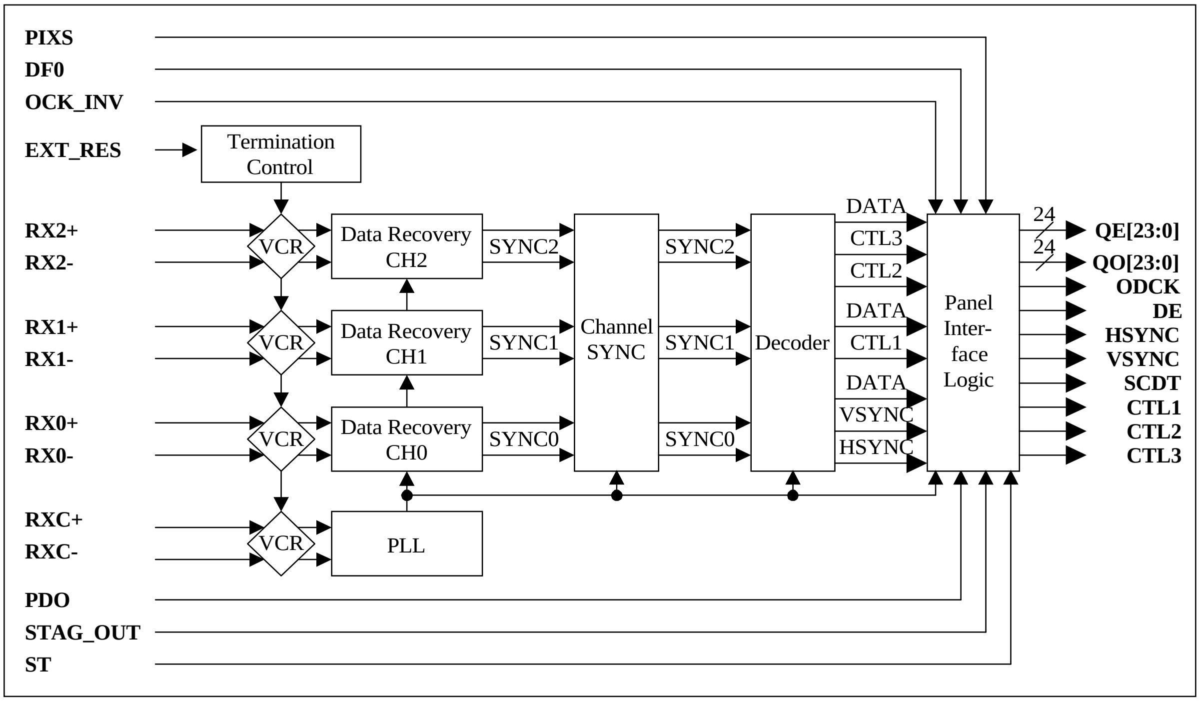
Features

- Low Power: 3.3V core operation
- Time staggered data output for reduced ground bounce
- Sync Detect: for Plug & Display "Hot Plugging"
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI 161A Pin Diagram



Functional Block Diagram



Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-40		125	°C
P_{PD}	Package Power Dissipation			1.8	W

Notes: [1] Permanent device damage may occur if absolute maximum conditions are exceeded.
[2] Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.00	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	μA

Note: [1] Guaranteed by design.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive Data and Controls	$V_{OUT} = V_{OH}$; ST = 1 ST = 0	4.2 2.1	8 4	18 9	mA
I_{OLD}	Output Low Drive Data and Controls	$V_{OUT} = V_{OL}$; ST = 1 ST = 0	-5.2 -2.6	-5.5 -2.75	-11 -5.5	mA
I_{OHC}	ODCK High Drive	$V_{OUT} = V_{OH}$; ST = 1 ST = 0	8.5 4.2	17 9	37 18	mA
I_{OLC}	ODCK Low Drive	$V_{OUT} = V_{OL}$; ST = 1 ST = 0	-10.4 -5.2	-16 -8	-23 -11	mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		75		1000	mV
I_{PD}	Power-down Current[2]				10	mA
I_{CCR}	Receiver Supply Current	DCLK=82.5MHz, 2-pixel/clock mode C_{LOAD}= 10pF R_{EXT_SWING} = 560Ω Typical Pattern[3]		240	270	mA
		DCLK=82.5MHz, 2-pixel/clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 560Ω Worse Case Pattern[4]		270	330	mA

Notes: [1] Guaranteed by design.
[2] The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.
[3] The Typical Pattern contains a gray scale area, checkerboard area, and text.
[4] Black and white checkerboard pattern, each checker is two pixel wide.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]	165MHz 1 pixel/clock			245	ps
T_{CCS}	Channel to Channel Differential Input Skew[1]	165MHz 1 pixel/clock			4	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[2,3]	65 MHz 1 pixel/clock			465	ps
		112 MHz 1 pixel/clock			270	ps
		165 MHz 1 pixel/clock			182	ps
D_{LHT}	Low-to-High Transition Time Data and Controls (measured at 70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			2.2	ns
		C_L = 5pF; ST = 0			2.5	ns
	ODCK (measured at 70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			2.0	ns
		C_L = 5pF; ST = 0			1.5	ns
D_{HLT}	High-to-Low Transition Time Data and Controls (measured at 70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			2.2	ns
		C_L = 5pF; ST = 0			2.2	ns
	ODCK (measured at 70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			1.5	ns
		C_L = 5pF; ST = 0			1.0	ns
T_{SOF}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV = 0, 165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	0.5			ns
		C_L = 5pF; ST = 0	0.5			ns
	(OCK_INV = 1, 165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	3.0			ns
		C_L = 5pF; ST = 0	2.0			ns
T_{HOF}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time to ODCK falling edge (OCK_INV = 0, 165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	3.0			ns
		C_L = 5pF; ST = 0	3.0			ns
	(OCK_INV = 1, 165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	1.2			ns
		C_L = 5pF; ST = 0	1.2			ns

Notes:
1 Guaranteed by design.
2 Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3 Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
4 Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5 Measured when transmitter was powered down (see SiI /AN-0005 "PanelLink Basic Design/Application Guide," Section 2.4).

AC Specifications *(continued)*

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{CIP}	ODCK Cycle Time[1] (1-pixel/clock)		6.06		40	ns
F_{CIP}	ODCK Frequency[1] (1-pixel/clock)		25		165	MHz
R_{CIP}	ODCK Cycle Time[1] (2-pixels/clock)		12.1		80	ns
F_{CIP}	ODCK Frequency[1] (2-pixels/clock)		12.5		82.5	MHz
R_{CIH}	ODCK High Time[4] (165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	1.1			ns
		C_L = 5pF; ST = 0	1.5			ns
R_{CIL}	ODCK Low Time[4] (165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	2.0			ns
		C_L = 5pF; ST = 0	2.3			ns
T_{PDL}	Delay from PD Low to high impedance outputs[1]				10	ns
T_{HSC}	Link disabled (DE inactive) to SCDT low[1]			100		ms
	Link disabled (Tx power down) to SCDT low[5]				250	ms
T_{FSC}	Link enabled (DE active) to SCDT high[1]			25		DE edges
T_{ST}	ODCK high to even data output[1]			0.25		R_{CIP}

Notes:
1. Guaranteed by design.
2. Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down (see SiI/AN-0005 "*PanelLink Basic Design/Application Guide*," Section 2.4).

Timing Diagrams

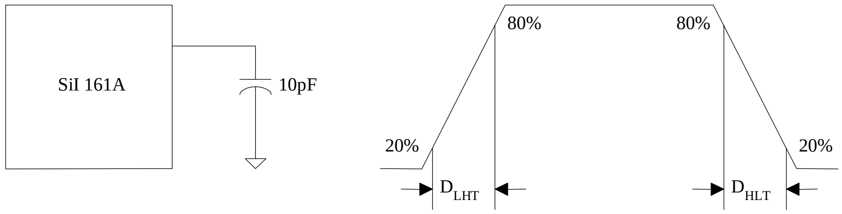


Figure 1. Digital Output Transition Times

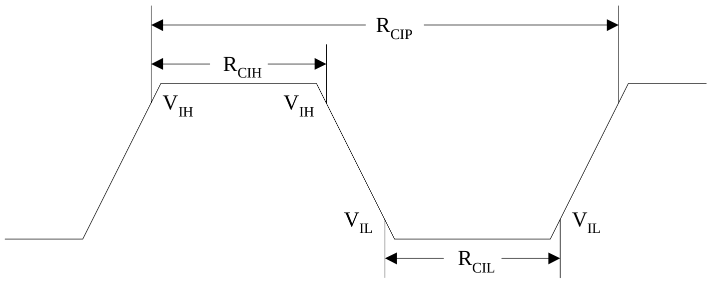


Figure 2. Receiver Clock Cycle/High/Low Times

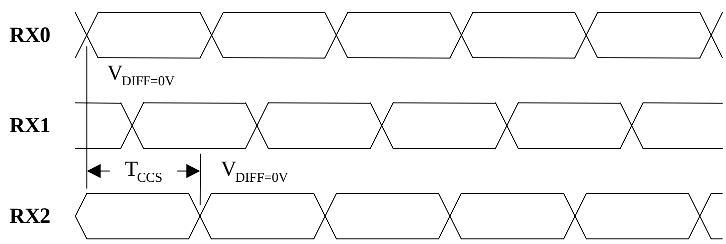


Figure 3. Channel-to-Channel Skew Timing

Output Timing

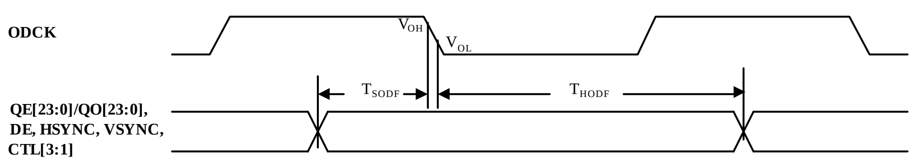


Figure 4. Output Data, DE, and Control Signals Setup/Hold Times to ODCK Falling Edge

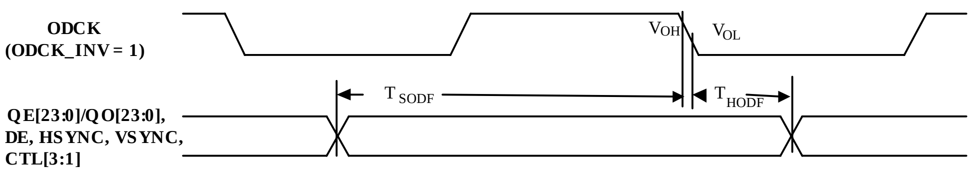


Figure 5. Output Data, DE, and Control Signals Setup/Hold Times to ODCK Falling Edge with Inverted Output Clock (ODCK_INV = 1)

Output Timing *(continued)*

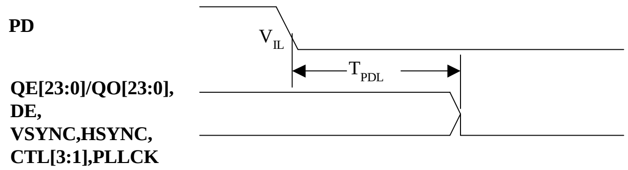


Figure 6. Output Signals Disabled Timing from PD Active

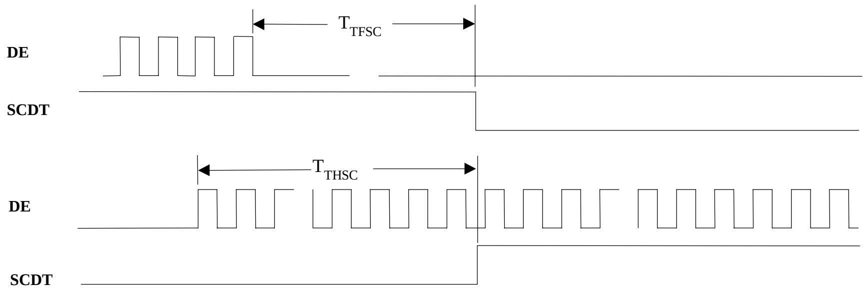


Figure 7. SCDT Timing from DE Inactive/Active

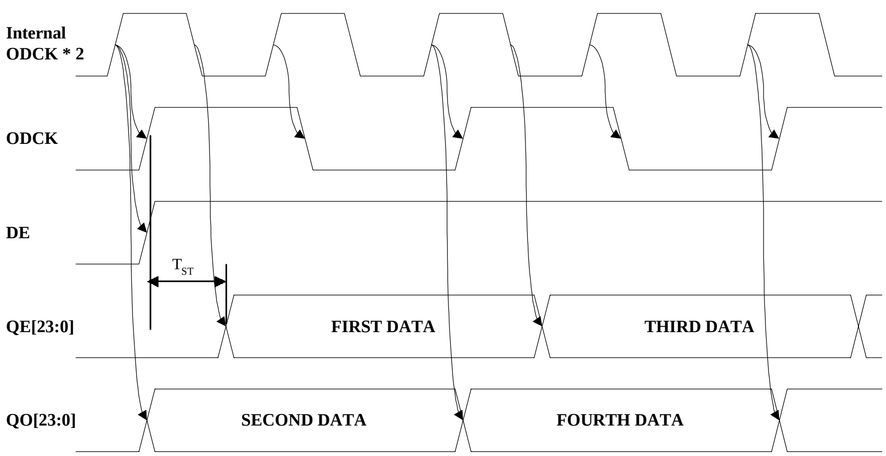


Figure 8. TFT 2-Pixels/Clock Staggered Output Timing Diagram

Output Pins Description

Pin Name	Pin #	Type	Description
QE23-QE0	See SiI 161A Pin Diagram	Out	Output Even Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode and to the first 24-bit pixel data for 2-pixels/clock mode. Output data is synchronized with output data clock (ODCK). Refer to the TFT Signal Mapping application note (SiI/AN-0007) which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
QO23-QO0	See SiI 161A Pin Diagram	Out	Output Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. During 1-pixel/clock mode, these outputs are driven low. Output data is synchronized with output data clock (ODCK). Refer to the TFT Signal Mapping application note (SiI/AN-0007) which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
ODCK	44	Out	Output Data Clock. This output can be inverted using the OCK_INV pin. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
DE	46	Out	Output Data Enable. This signal qualifies the active data area. A HIGH level signifies active display time and a LOW level signifies blanking time. This output signal is synchronized with the output data. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
HSYNC VSYNC CTL1 CTL2 CTL3	48 47 40 41 42	Out Out Out Out Out	Horizontal Sync input control signal. Vertical Sync input control signal. General output control signal 1. This output is **not** powered down by PDO. General output control signal 2. General output control signal 3. A low level on PD or PDO will put the output drivers (except CTL1 by PDO) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.

Configuration Pins Description

Pin Name	Pin #	Type	Description
OCK_INV	100	In	ODCK Polarity. A LOW level selects normal ODCK output. A HIGH level selects inverted ODCK output. All other output signals are not affected by this pin. They will maintain the same timing no matter the setting of OCK_INV pin.
PIXS	4	In	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel.
STAG_OUT	7	In	Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive. This function is only available in 2-pixels per clock mode.
ST	3	In	Output Drive. A HIGH level selects HIGH output drive strength. A LOW level selects LOW output drive strength.

Power Management Pins Description

Pin Name	Pin #	Type	Description
SCDT	8	Out	Sync Detect. A HIGH level is outputted when DE is actively toggling indicating that the link is alive. A LOW level is outputted when DE is inactive, indicating the link is down. Can be connected to PDO to power down the outputs when DE is not detected. The SCDT output itself, however, remains in the active mode at all times.
PDO	9	In	Output Driver Power Down (active LOW). A HIGH level indicates normal operation. A LOW level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. PDO is a sub-set of the PD description. The chip is not in power-down mode with this pin. SCDT and CTL1 are not tri-stated by this pin.
PD	2	In	Power Down (active LOW). A HIGH level indicates normal operation and a LOW level indicates power down mode. During power down mode, all output buffers are disabled and brought low, all analog logic is powered down, and all inputs are disabled.

Differential Signal Data Pins Description

Pin Name	Pin #	Type	Description
RX0+ RX0- RX1+ RX1- RX2+ RX2-	90 91 85 86 80 81	Analog Analog Analog Analog Analog Analog	TMDS Low Voltage Differential Signal input data pairs.
RXC+ RXC-	93 94	Analog Analog	TMDS Low Voltage Differential Signal input data pairs.
EXT_RES	96	Analog	Impedance Matching Control. Resistor value should be approximately ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 560Ω resistor must be connected between AVCC and this pin.

Reserved Pin Description

Pin Name	Pin #	Type	Description
RESERVED	1	In	Must be tied LOW for normal operation.
RESERVED	99	In	Must be tied HIGH for normal operation.

Power and Ground Pins Description

Pin Name	Pin #	Type	Description
VCC	6,38,67	Power	Digital Core VCC, must be set to 3.3V.
GND	5,39,68	Ground	Digital Core GND.
OVCC	18,29,43,57,78	Power	Output VCC, must be set to 3.3V.
OGND	19,28,45,58,76	Ground	Output GND.
AVCC	82,84,88,95	Power	Analog VCC must be set to 3.3V.
AGND	79,83,87,89,92	Ground	Analog GND.
PVCC	97	Power	PLL Analog VCC must be set to 3.3V.
PGND	98	Ground	PLL Analog GND.

TFT Panel Data Mapping

The following table shows the output data mapping in one pixel per clock mode for the SiI 161A. This output data mapping is dependent upon the SiI PanelLink transmitters having the exact same type of input data mappings. Please refer to the SiI PanelLink transmitter for the specific input data mappings and to the TFT Signal Mapping application note (SiI AN-0007).

	SiI 161A	
	1-Pixel/Clock Output	
	18bpp	24bpp
BLUE[7:0]	QE[7:2]	QE[7:0]
GREEN[7:0]	QE[15:10]	QE[15:8]
RED[7:0]	QE[23:18]	QE[23:16]

Table 1. One Pixel/Clock Mode Data Mapping

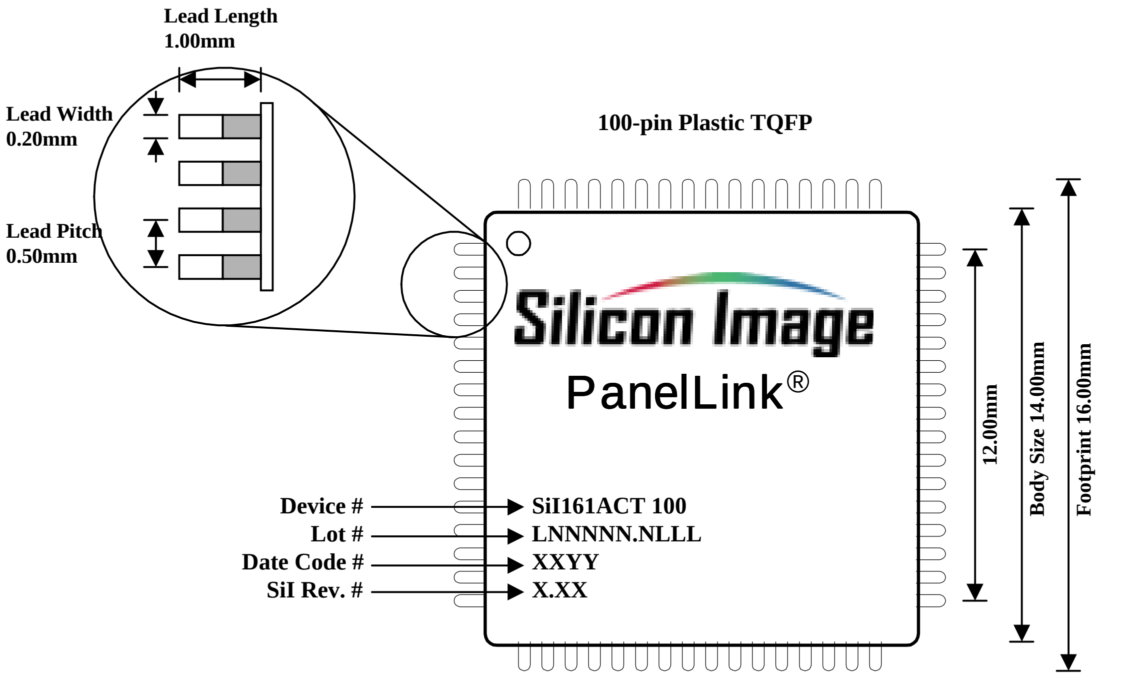
	SiI 161A	
	2-Pixel/Clock Output	
	18bpp	24bpp
BLUE[7:0] - 0	QE[7:2]	QE[7:0]
GREEN[7:0] – 0	QE[15:10]	QE[15:8]
RED[7:0] – 0	QE[23:18]	QE[23:16]
BLUE[7:0] – 1	QO[7:2]	QO[7:0]
GREEN[7:0] – 1	QO[15:10]	QO[15:8]
RED[7:0] – 1	QO[23:18]	QO[23:16]

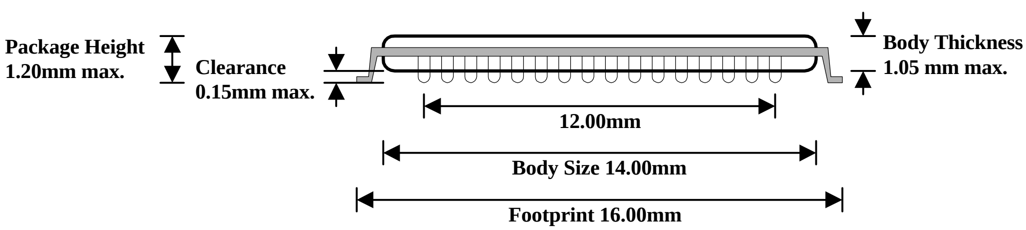
Table 2. Two Pixel/Clock Mode Data Mapping

Note: For 18-bit mode, the Flat Panel Timing Controller interfaces to the SiI 161A exactly the same as in the 24-bit mode; however, only 6-bits per channel (color) are interfaced instead of the full 8. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified.

Package Dimensions

PanelLink®





100-pin TQFP Package Dimensions

PCB Design Requirements

In order to remove the heat from the package, it is required that a thermal land be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package, as shown in *Figure 10: TQFP Thermal Land Design on PCB.* Although the size of this thermal land can be larger than the exposed pad on the package, the solderable area, as defined by the solder mask, should be at least the same as the exposed pad area on the package. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the thermal land and the inner edges of pad pattern for the leads to avoid any shorts.

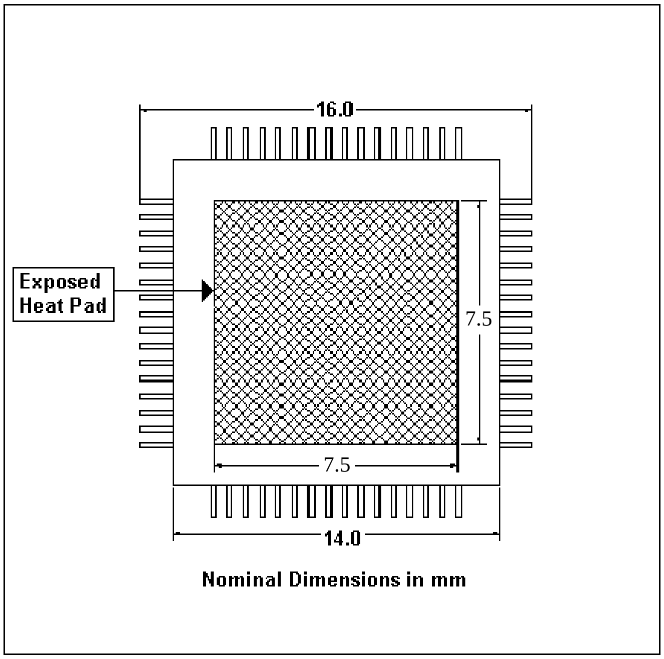


Figure 9. Bottom View of Thermally Enhanced 100-pin TQFP Package

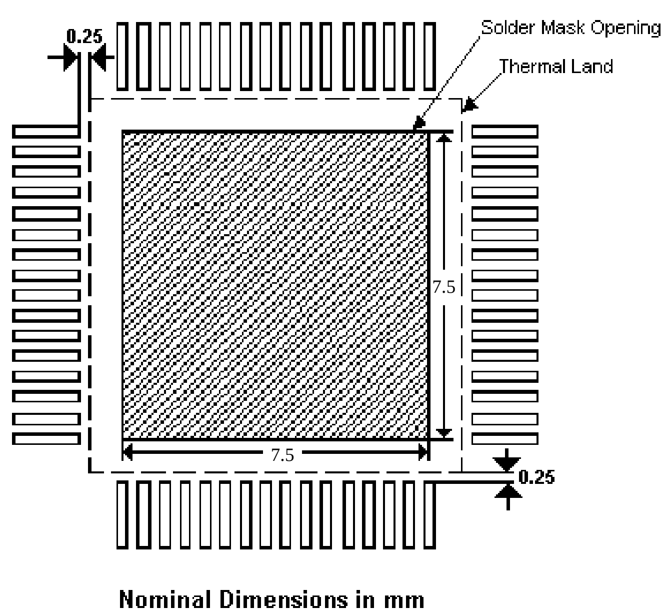


Figure 10. TQFP Thermal Land Design on PCB

While the thermal land on the PCB provides a means of heat transfer from the package to the board through a solder joint, thermal vias are required to remove the heat from the PCB. It is recommended that these vias connect to the ground plane of the PCB. These vias provide a heat transfer path from the top surface of the PCB to the inner layers and the bottom surface of the package. An array of vias should be incorporated in the thermal pad at 1.2 mm pitch grid, as shown in *Figure 11. Thermal Pad Via Grid*. It is also recommended that the via diameter should be around 12 to 13 mils (0.30 to 0.33 mm) and the via barrel should be plated with 1 oz copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

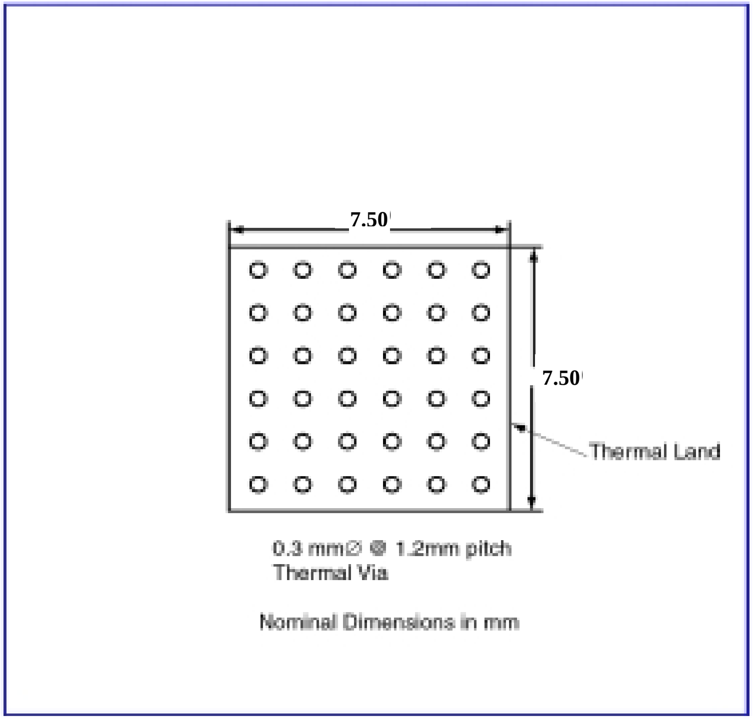


Figure 11. Thermal Pad Via Grid

Board Mounting Guidelines

The following are general recommendations for mounting exposed pad leadframe devices on the motherboard. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally enhanced packages.

Stencil Design:

For proper heat transfer, it is required that the exposed pad on the package be soldered to the thermal land on the PCB. This requires solder paste application not only on the pad pattern for lead attachment but also on the thermal land using the stencil. While for standard (non-thermally enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package coplanarity only, the package standoff also needs to be considered for the thermally enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 5 to 8 mils (depending upon the pitch) should still provide good solder joint between the exposed pad and the thermal land. The aperture openings should be the same as the solder mask opening on the thermal land. Since a large stencil opening may result in poor release, the aperture opening can be subdivided into an array of smaller openings, similar to the thermal land pattern shown in *Figure 12. Recommended Stencil Design*. The above guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

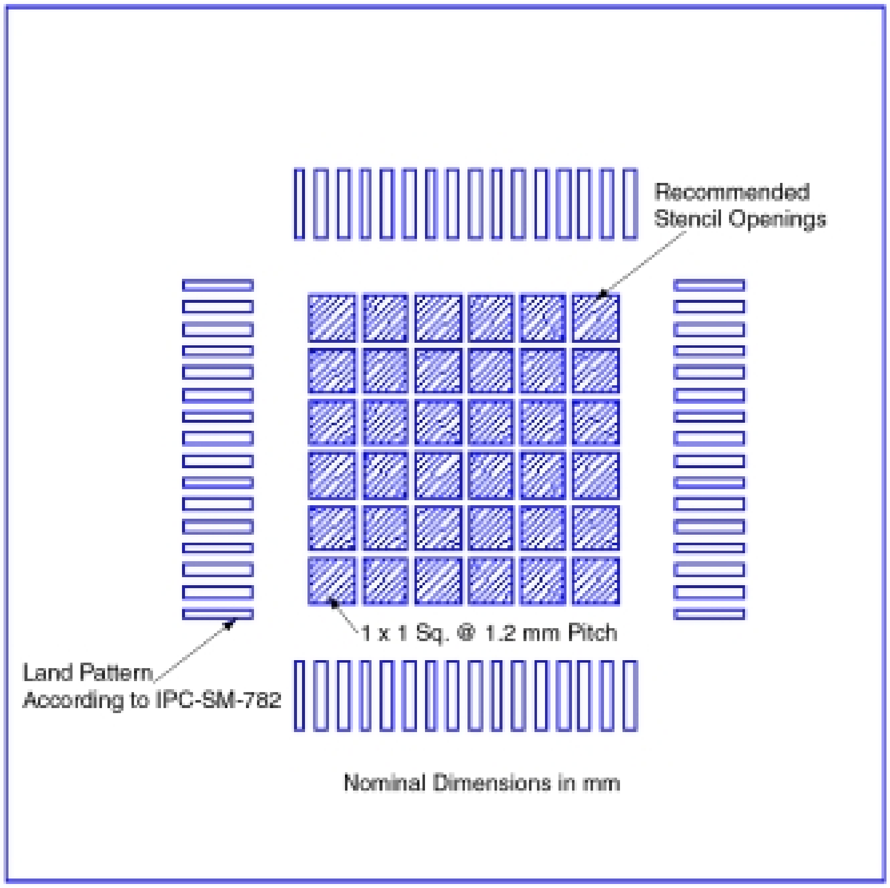


Figure 12. Recommended Stencil Design

Application Information

To obtain the most updated Application Notes and other useful information for your design application, please visit the Silicon Image web site at ***www.siimage.com***, or contact your local Silicon Image sales office.

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Ordering Information

Part Number: SiI161ACT100

Revision History

Revision	Date	Comment
0.86	11/99	Preliminary release
A	3/00	Full release

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