QL5022 QuickPCI Data Sheet

33 MHz/32-bit PCI Host Capable Master Target with Embedded Programmable Logic

Device Highlights

High Performance PCI Controller

- 32-bit / 33 MHz PCI Master/Target with Embedded Programmable Logic
- Zero-wait state PCI Master provides 132 MBps transfer rates
- Programmable back-end interface to optional local processor
- Independent PCI bus (33 MHz) and local bus (up to 160 MHz) clocks
- Fully Customizable PCI Configuration Space
- Reference design with driver code (Win 95/98/Win 2000/NT4.0) available
- PCI v2.2 compliant
- Supports Type 0 Configuration Cycles in Target mode
- 3.3 V, 5 V tolerant PCI signaling supports Universal PCI Adapter designs
- High performance PCI controller 3.3 V CMOS in 208-pin PQFP and 144-pin TQFP packages
- Supports unlimited/continuous burst transfers

Extendable PCI Functionality

- Support for Configuration Space from 0 × 40 to 0 × 3FF
- Multi-Function, Expanded Capabilities, and Expansion ROM capable
- Power Management, Compact PCI, Hot-Swap/Hot-Plug compatible
- PCI v2.2 Power Management Specification compatible
- PCI v2.2 Vital Product Data (VPD) configuration support
- Programmable Interrupt Generator
- I_2O Support with local processor
- Mailbox Register support

Programmable Logic

- 387 Logic Cells
- 250 MHz 16-bit counters and 275 MHz datapaths
- All back-end interface and glue-logic can be implemented on chip
- Three 32-bit bus interfaces between the PCI Controller and the Programmable Logic

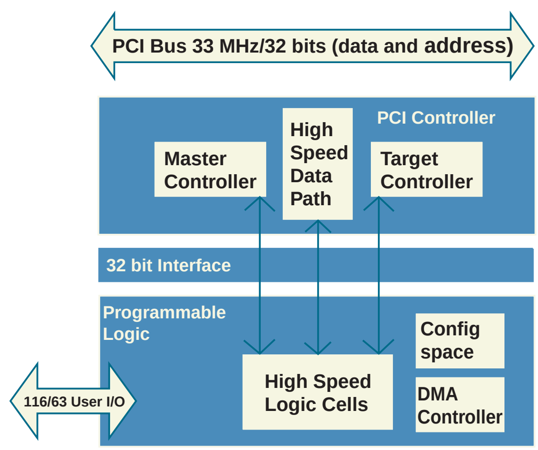


Figure 1: QL5022 Block Diagram

Architecture Overview

The QL5022 device in the QuickLogic® QuickPCI™ ESP (Embedded Standard Product) family provides a complete and customizable PCI interface solution combined with 25,000 system gates of programmable logic. This device eliminates any need for the designer to worry about PCI bus compliance, yet allows for the maximum 32-bit PCI bus bandwidth (132 MBps).

The programmable logic portion of the device contains 387 QuickLogic logic cells.

The QL5022 device meets PCI 2.2 electrical and timing specifications and has been fully hardware-tested.

The QL5022 device features 3.3 V operation with multi-volt compatible I/Os. Thus, it can easily operate in 3 V systems and is fully compatible with 3.3 V, 5 V, or Universal PCI card development.

PCI Controller

The PCI Controller is a 32-bit/33 MHz PCI 2.2 Compliant Master/Target Controller. It is capable of infinite length Master Write and Read transactions at zero wait state (132 MBps). The Master will never insert wait states during transfers, so data should be supplied or received by the logic in the programmable region of the device. The Master Controller will most often be operated by a DMA Controller in the programmable region of the device. A DMA Controller reference design is available. The Target interface offers full PCI Configuration Space and flexible target addressing. Any number of 32-bit BARs may be configured, as either memory or I/O space. All required and optional PCI 2.2 Configuration Space registers can be implemented within the programmable region of the device. A reference design of a Target Configuration and Addressing module is provided.

The interface ports are divided into a set of ports for master transactions and a set for target transactions. The Master DMA controller and Target Configuration Space and Address Decoding are done in the programmable logic region of the device. Since these functions are not timing critical, leaving these elements in the programmable region allows the greatest degree of flexibility to the designer. References to DMA controller, Configuration Space, and Address Decoding blocks are included so that the design cycle can be minimized.

Configuration Space and Address Decode

The configuration space is completely customizable in the programmable region of the device.

PCI address and command decoding is performed by logic in the programmable section of the device. This allows support for any size of memory or I/O space for back-end logic. It also allows the user to implement any subset of PCI commands supported by the QL5022. QuickLogic provides a reference Address Register/Counter and Command Decode block.

DMA Master/Target Control

The customizable DMA controller included with the QuickWorks® design software contains the following features:

- Supports DMA transfer from PCI to external
- Configurable DMA burst size for PCI
- DMA Registers may be mapped to any area of Target Memory Space
  - Read Address (32-bit register)
  - Read Length (16-bit register)
  - Control and Status (32-bit register, includes 2 bit Burst Length)
- DMA Registers are available to the local design or the PCI bus
- Programmable Interrupt Control to signal end of transfer or other event

Internal PCI Interface

Figure 2 shows the interface symbol you will use in your schematic design to attach the local interface programmable logic design to the PCI core. If you were designing with a top-level Verilog® or VHDL file, then you would use a structural instantiation of this PCI32 block, instead of a graphical symbol.

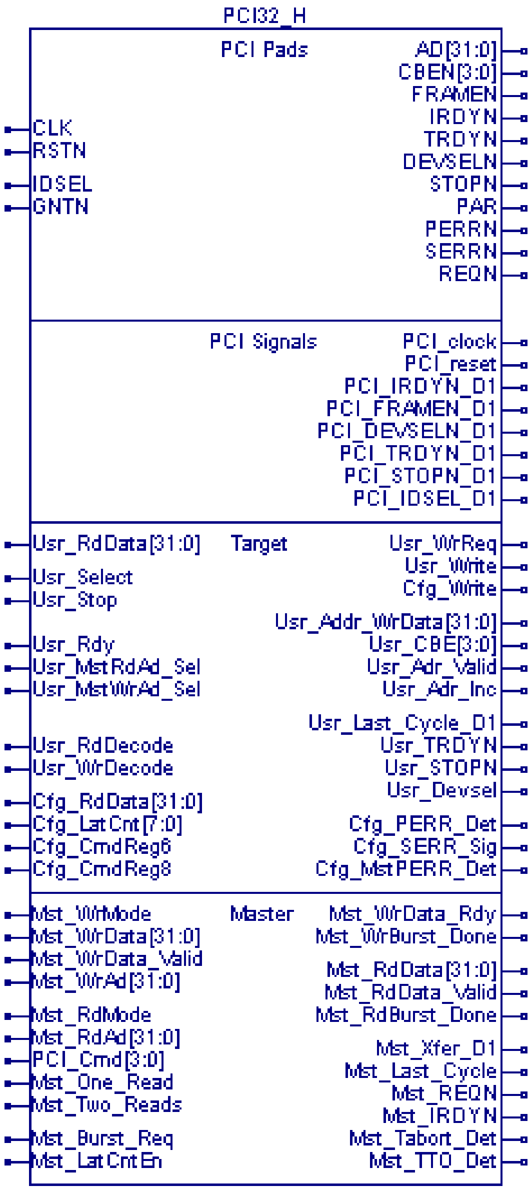


Figure 2: PCI Interface Symbol

PCI Master Interface

Table 1 lists the internal signals used to interface with the PCI controller in the QL5022 along with a description of each signal. The direction of the signal indicates if it is an input provided by the local interface (I) or an output provided by the PCI controller (O). Signals that end with the character 'N' should be considered active-low (for example, Mst_IRDYN).

Table 1: PCI Controller Signals

Signal	I/O	Description
Mst_WrAd[31:0]	I	**Address for master DMA Writes**. This address must be treated as valid from the beginning of a DMA burst write until the DMA write operation is complete. It must be incremented by four each time data is transferred on the PCI bus, since only DWORD (4 byte) transfers are supported.
Mst_RdAd[31:0]	I	**Address for master DMA Reads**. This address must be treated as valid from the beginning of a DMA burst read until the DMA read operation is complete. It must be incremented by four each time data is transferred on the PCI bus, since only DWORD (4 byte) transfers are supported.
Mst_WrMode	I	**DMA state machine in Write mode**. This must be asserted at the beginning of a Master Transfer, and must be held until the Master Transfer completed (Mst_WrBurst_Done).
Mst_RdMode	I	**DMA state machine in Read mode**. This must be asserted at the beginning of a Master Transfer, and must be held until the Master Transfer completed (Mst_RdBurst_Done).
Mst_Burst_Req	I	**Request use of the PCI bus**. This signal should be held from when the DMA controller is ready to provide the first data, until the transfer is complete (Mst_WrBurst Done or Mst_RdBurst_Done).
Mst_One_Read	I	This signals to the PCI core that one data transfer remains in the burst. This signal must be asserted when only one DWORD remains to be transferred on the PCI bus.
Mst_Two_Reads	I	Two or less data transfers remain in the burst. This signal must be asserted when two or less DWORDs remain to be transferred on the PCI bus.
Mst_WrData[31:0]	I	Data for master DMA writes (to PCI bus).
Mst_WrData_Valid	I	Data valid on Mst_WrData[31:0].
Mst_WrData_Rdy	O	Data receive acknowledge for Mst_WrData[31:0]. This serves as a POP control for a FIFO which provides data to the PCI core.
Mst_WrBurst_Done	O	Master Write pipeline is empty, which indicates that the Write burst transaction is completed.
Mst_RdData[31:0]	O	Data for master DMA reads (from PCI bus).
Mst_RdData_Valid	O	Data valid on Mst_RdData[31:0]. This serves as a PUSH control for a FIFO that receives data from the PCI core.
Mst_RdBurst_Done	O	Master read pipeline is empty, which indicates that Read burst transaction is completed.

Table 1: PCI Controller Signals (Continued)

PCI_Cmd[3:0]	I	**PCI command to be used for the master transaction.** This signal must remain unchanged throughout the period when Mst_Burst_Req is active. PCI commands considered as Reads include Interrupt Acknowledge, I/O Read, Memory Read, Configuration Read, Memory Read Multiple, Memory Read Line. PCI commands considered as Writes include Special Cycle, I/O Write, Memory Write, Configuration Write, Memory Write and Invalidate. Users should make sure that only valid PCI commands are supplied.
Mst_LatCntEn	I	**Enable Latency Counter.** Set to 0 to ignore the Latency Timer in the PCI configuration space (offset 0Ch). For full PCI compliance, this port should be always set to 1.
Mst_Xfer_D1	O	Data was transferred on the previous PCI clock. Useful for updating DMA transfer counts on DMA Read operations.
Mst_Last_Cycle	O	Active during the last data transfer of a PCI master transaction.
Mst_REQN	O	The PCI REQN signal generated by this device as PCI master. Not usually used in the back-end design.
Mst_IRDYN	O	The PCI IRDYN signal generated by this device as PCI master. Not usually used in the back-end design.
Mst_Tabort_Det	O	Target abort detected during master transaction. This is normally an error condition to be handled in the DMA controller.
Mst_TTO_Det	O	Target timeout detected (no response from target). This is normally an error condition to be handled in the DMA controller.

PCI Target Interface

Table 2: PCI Target Interface Signals

Signal	I/O	Description
Usr_Addr_WrData [31:0]	O	**Target address and data from target Writes**. During all target accesses, the address will be presented on Usr_Addr_WrData[31:0] and simultaneously, Usr_Adr_Valid will be active. During target Write transactions, this port will present write data to the PCI configuration space or user logic.
Usr_CBE[3:0]	O	**PCI command and byte enables**. During target accesses, the PCI command will be presented on Usr_CBE[3:0] and simultaneously, Usr_Adr_Valid will be active. During target Read or Write transactions, this port will present active-low byte-enables to the PCI configuration space or user logic.
Usr_Adr_Valid	O	Indicates the beginning of a PCI transaction, and that a target address is valid on Usr_Addr_WrData[31:0] and the PCI command is valid on Usr_CBE[3:0]. When this signal is active, the target address must be latched and decoded to determine if this address belongs to the device's memory space. Also, the PCI command must be decoded to determine the type of PCI transaction. On subsequent clocks of a target access, this signal will be low, indicating that data (not an address) is present on Usr_Addr_WrData[31:0].
Usr_Adr_Inc	O	Indicates that the target address should be incremented, because the previous data transfer was completed. During burst target accesses, the target address is only presented to the back-end logic at the beginning of the transaction (when Usr_Adr_Valid is active), and must therefore be latched and incremented by four for subsequent data transfers.
Usr_WrReq	O	This signal will be active for the duration of a target Write transaction, and may be used by back-end logic to turn on output-enables for transmitting the data off-chip.
Usr_RdDecode	I	Active when a user Read command has been decoded from the Usr_CBE[3:0] bus. This command may be mapped from any of the PCI Read commands, such as Memory Read, Memory Read Line, Memory Read Multiple, I/O Read, etc.
Usr_WrDecode	I	Active when a user Write command has been decoded from the Usr_CBE[3:0] bus. This command may be mapped from any of the PCI Write commands, such as Memory Write or I/O Write.
Usr_Select	I	The address on Usr_Addr_WrData[31:0] has been decoded and determined to be within the address space of the device. Usr_Addr_WrData[31:0] must be compared to each of the valid Base Address Registers in the PCI configuration space. Also, this signal must be gated by the Memory Access Enable or I/O Access Enable registers in the PCI configuration space (Command Register bits 1 or 0 at offset 04h).
Usr_Write	O	Write enable for data on Usr_Addr_WrData[31:0] during PCI writes.
Cfg_Write	O	Write enable for data on Usr_Addr_WrData[31:0] during PCI configuration Write transactions.
Cfg_RdData[31:0]	I	Data from the PCI configuration registers, required to be presented during PCI configuration reads.

Table 2: PCI Target Interface Signals (Continued)

Usr_RdData[31:0]	I	Data from the back-end user logic (and/or DMA configuration registers), required to be presented during PCI reads.
Cfg_CmdReg8 Cfg_CmdReg6	I	Bits 6 and 8 from the Command Register in the PCI configuration space (offset 04h).
Cfg_LatCnt[7:0]	I	8-bit value of the Latency Timer in the PCI configuration space (offset 0Ch).
Usr_MstRdAd_Sel	I	Used when a target Read operation should return the value set on the Mst_RdAd[31:0] pins. This select pin saves on logic which would otherwise need to be used to multiplex Mst_RdAd[31:0] into the Usr_RdData[31:0] bus. When this signal is asserted, the data on Usr_RdData[31:0] is ignored.
Usr_MstWrAd_Sel	I	Used when a target Read operation should return the value set on the Mst_WrAd[31:0] pins. This select pin saves on logic which would otherwise need to be used to multiplex Mst_WrAd[31:0] into the Usr_RdData[31:0] bus. When this signal is asserted, the data on Usr_RdData[31:0] is ignored.
Cfg_PERR_Det	O	**Parity error detected on the PCI bus**. When this signal is active, bit 15 of the Status Register must be set in the PCI configuration space (offset 04h).
Cfg_SERR_Sig	O	**System error asserted on the PCI bus**. When this signal is active, the Signalled System Error bit, bit 14 of the Status Register, must be set in the PCI configuration space (offset 04h).
Cfg_MstPERR_Det	O	**Data parity error detected on the PCI bus by the master**. When this signal is active, bit 8 of the Status Register must be set in the PCI configuration space (offset 04h).
Usr_TRDYN	O	Copy of the TRDYN signal as driven by the PCI target interface.
Usr_STOPN	O	Copy of the STOPN signal as driven by the PCI target interface.
Usr_Devsel	O	Inverted copy of the DEVSELN signal as driven by the PCI target interface.
Usr_Last_Cycle_D1	O	Last transfer in a PCI transaction is occurring.
Usr_Rdy	I	Used to delay (add wait states to) a PCI transaction when the back end needs additional time. Subject to PCI latency restrictions.
Usr_Stop	I	Used to prematurely stop a PCI target access on the next PCI clock.

PCI Internal Signals

Table 3: PCI Internal Signals

Signal	I/O	Description
PCI_clock	O	PCI clock.
PCI_reset	O	PCI reset signal.
PCI_IRDYN_D1	O	Copy of the IRDYN signal from the PCI bus, delayed by one clock.
PCI_FRAMEN_D1	O	Copy of the FRAMEN signal from the PCI bus, delayed by one clock.
PCI_DEVSELN_D1	O	Copy of the DEVSELN signal from the PCI bus, delayed by one clock.
PCI_TRDYN_D1	O	Copy of the TRDYN signal from the PCI bus, delayed by one clock.
PCI_STOPN_D1	O	Copy of the STOPN signal from the PCI bus, delayed by one clock.
PCI_IDSEL_D1	O	Copy of the IDSEL signal from the PCI bus, delayed by one clock.

JTAG Support

JTAG pins support IEEE standard 1149.1a to provide boundary scan capability for the QL5022 device. Six pins are dedicated to JTAG and programming functions on each QL5022 device, and are unavailable for general design input and output signals. TDI, TDO, TCK, TMS, and TRSTB are JTAG pins. A sixth pin, STM, is used only for programming.

Development Tool Support

Software support for the QL5022 device is available through the Quick*Works*® development package. This turnkey PC-based Quick*Works* package, shown in **Figure 3**, provides a complete ESP software solution with design entry, logic synthesis, place and route, and simulation. Quick*Works* includes VHDL, Verilog®, schematic, and mixed-mode entry with fast and efficient logic synthesis provided by the integrated Synplicity Synplify Lite™ tool, specially tuned to take advantage of the QL5022 architecture. Quick*Works* also provides functional and timing simulation for guaranteed timing and source-level debugging.

The UNIX-based Quick*Tools*™ and PC-based Quick*Works-Lite* packages are a subset of Quick*Works* and provide a solution for designers who use schematic-only design flow third-party tools for design entry, synthesis, or simulation. Quick*Tools* and Quick*Works-Lite* read EDIF netlists and provide support for all QuickLogic devices. Quick*Tools* and Quick*Works-Lite* also support a wide range of third-party modeling and simulation tools. In addition, the PC-based package combines all the features of Quick*Works-Lite* with the SCS schematic capture environment, providing a low-cost design entry and compilation solution.

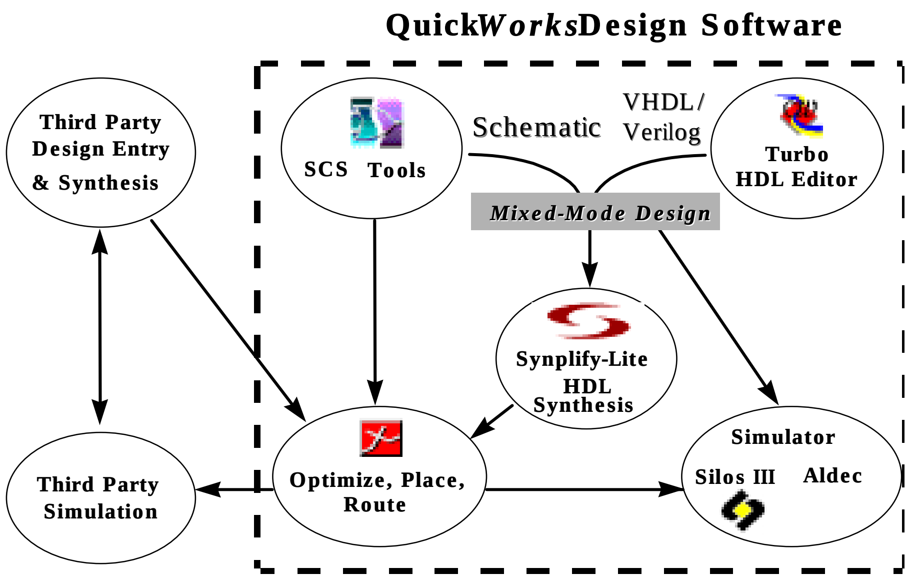


Figure 3: QuickWorks Tool Suite

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 10** by the numbers provided in **Table 4** through **Table 8**.

Table 4: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay [b]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time [b]	1.7	1.7	1.7	1.7	1.7
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 10**.

b. These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 5: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 10**.

Table 6: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 11 loads per half column.

Table 7: Input-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 10**.

Table 8: Output-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State [a]	2.0	-	-	-	-
t_{PLZ}	Output Delay Low to Tri-State	1.2	-	-	-	-

a. The following loads presented in **Figure 4** are used for t_{PXZ}:

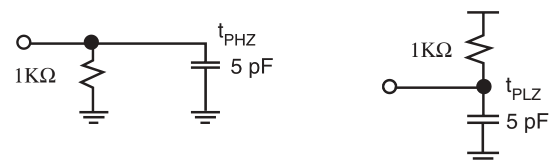


Figure 4: Loads used for t_{PXZ}

DC Characteristics

The DC specifications are provided in **Table 9** through **Table 11**.

Table 9: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 10: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55	-	-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a

Table 11: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage		0.5 V_{CC}	V_{CCIO} + 0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{CC}	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12 mA	2.4		V
		I_{OH} = -500 µA	0.9 V_{CC}		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA[a]		0.45	V
		I_{OL} = 1.5 mA		0.1 V_{CC}	V
I_I	I or I/O Input Leakage Current	V_I = V_{CCIO} or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	V_I = V_{CCIO} or GND	-10	10	µA
C_I	Input Capacitance[b]			10	pF
I_{OS}	Output Short Circuit Current[c]	V_O = GND	-15	-180	mA
		V_O = V_{CC}	40	210	mA
I_{CC}	D.C. Supply Current[d]	V_I, V_{IO} = V_{CCIO} or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. For -1/-2/-3/-4 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group. (See **Contact Information**).

Kv and Kt Graphs

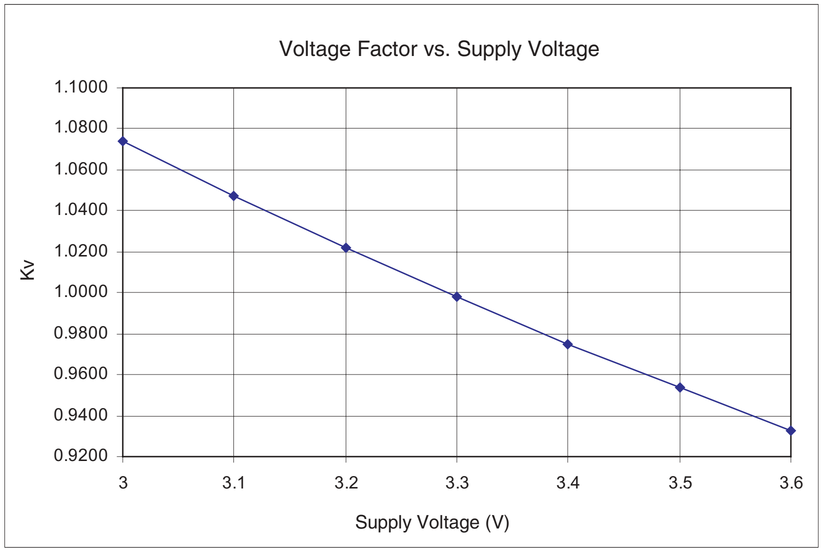


Figure 5: Voltage Factor vs. Supply Voltage

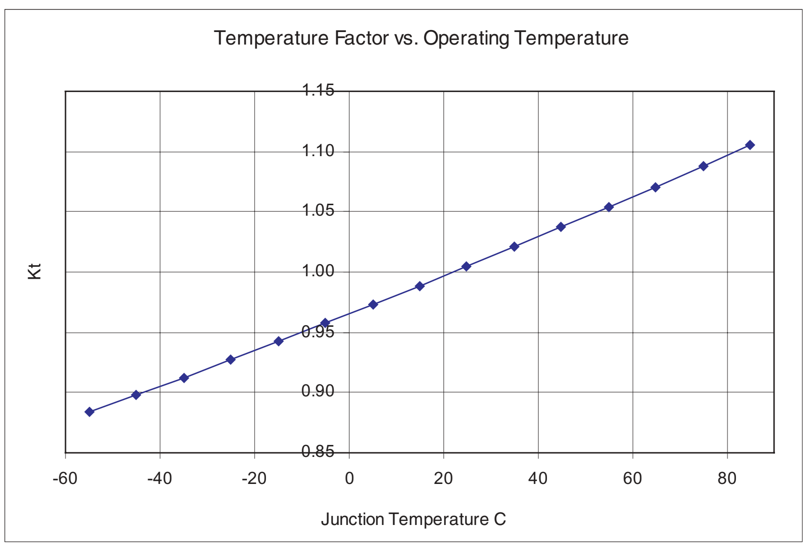


Figure 6: Temperature Factor vs. Operating Temperature

QL5022 External Device Pins

The definitions for the QL5022 pin types are listed in **Table 12**.The names of all QL5022 device pins are indicated in **Table 13** and **Table 14**. These are pins on the device, some of which connect to the PCI bus, and others that are programmable as user I/O.

Table 12: QL5022 External Device Pins

Type	Description
IN	Input. A standard input-only signal
OUT	Totem pole output. A standard active output driver
T/S	Tri-state. A bi-directional, tri-state input/output pin
S/T/S	Sustained Tri-state. An active low tri-state signal driven by one PCI agent at a time. It must be driven high for at least one clock before being disabled (set to Hi-Z). A pull-up needs to be provided by the PCI system central resource to sustain the inactive state once the active driver has released the signal.
O/D	Open Drain. Allows multiple devices to share this pin as a wired-or.

Table 13: QL5022 External Device Pins

Pin/Bus Name	Type	Function
VCC	IN	Supply pin. Tie to 3.3 V supply.
VCCIO	IN	Supply pin for I/O. Set to 3.3 V for 3.3 V I/O, 5 V for 5.0 V compliant I/O
GND	IN	Ground pin. Tie to GND on the PCB.
I/O	T/S	Programmable Input/Output/Tri-State/Bi-directional Pin.
GLCK/I	IN	Programmable Global Network or Input-only pin. Tie to V_{CC} or GND if unused.
ACLK/I	IN	Programmable Array Network or Input-only pin. Tie to V_{CC} or GND if unused.
TDI/RSI*	IN	JTAG Data In/Ram Init. Serial Data In. Tie to V_{CC} if unused. Connect to Serial EPROM data for RAM init.
TDO/RCO*	OUT	JTAG Data Out/Ram Init Clock. Leave unconnected if unused. Connect to Serial EPROM clock for RAM init.
TCK	IN	JTAG Clock. Tie to GND if unused.
TMS	IN	JTAG Test Mode Select. Tie to V_{CC} if unused.
TRSTB/RRO*	IN	JTAG Reset/RAM Init. Reset Out. Tie to GND if unused. Connect to Serial EPROM reset for RAM init.
STM	IN	QuickLogic Reserved pin. Tie to GND on the PCB.

Table 14: QL5022 External Device Pins

Pin/Bus Name	Type	Function
AD[31:0]	T/S	**PCI Address and Data** 32 bit multiplexed address/data bus.
CBEN[3:0]	T/S	**PCI Bus Command and Byte Enables** Multiplexed bus which contains byte enables for AD[31:0] or the Bus Command during the address phase of a PCI transaction.
PAR	T/S	**PCI Parity** Even Parity across AD[31:0] and C/BEN[3:0] busses. Driven one clock after address or data phases. Master drives PAR on address cycles and PCI writes. The Target drives PAR on PCI reads.
FRAMEN	S/T/S	**PCI Cycle Frame** Driven active by current PCI Master during a PCI transaction. Driven low to indicate the address cycle, driven high at the end of the transaction.
DEVSELN	S/T/S	**PCI Device Select** Driven by a Target that has decoded a valid base address.
CLK	IN	**PCI System Clock Input**
RSTN	IN	**PCI System Reset Input**
REQN	T/S	**PCI Request** Indicates to the Arbiter that this PCI Agent (Initiator) wants to use the bus. A point-to-point signal between the PCI device and the system Arbiter.
GNTN	IN	**PCI Grant** Indicates to a PCI Agent (Initiator) that it has been granted access to the PCI bus by the Arbiter. A point-to-point signal between the PCI device and the system Arbiter.
PERRN	S/T/S	**PCI Data Parity Error** Driven active by the initiator or target two clock cycles after a data parity error is detected on the AD and C/BEN busses.
SERRN	O/D	**PCI System Error** Driven active when an address cycle parity error, data parity error during a special cycle, or other catastrophic error is detected.
IDSEL	IN	**PCI Initialization Device Select** Use to select a specific PCI Agent during System Initialization.
IRDYN	S/T/S	**PCI Initiator Ready** Indicates the Initiator’s ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
TRDYN	S/T/S	**PCI Target Ready** Indicates the Target’s ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
STOPN	S/T/S	**PCI Stop** Used by a PCI Target to end a burst transaction.

144 TQFP Pinout Diagram

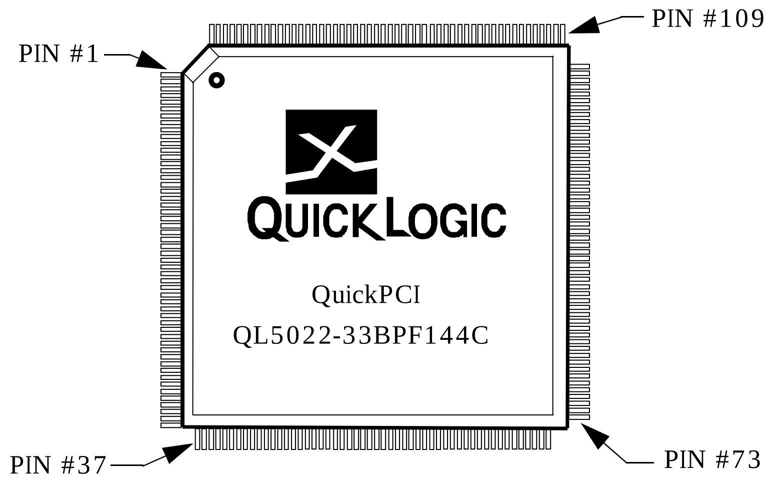


Figure 7: 144 TQFP Pinout Diagram

144 TQFP Pinout Table

Table 15: 144 TQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	37	AD[21]	73	AD[4]	109	TCK
2	I/O	38	TDI/RSI	74	AD[3]	110	STM
3	I/O	39	AD[20]	75	AD[2]	111	I/O
4	I/O	40	AD[19]	76	AD[1]	112	I/O
5	I/O	41	AD[18]	77	AD[0]	113	I/O
6	I/O	42	VCC	78	I/O	114	VCC
7	VCC	43	AD[17]	79	VCC	115	I/O
8	I/O	44	AD[16]	80	I/O	116	I/O
9	I/O	45	CBEN[2]	81	I/O	117	I/O
10	I/O	46	FRAMEN	82	I/O	118	I/O
11	I/O	47	IRDYN	83	I/O	119	I/O
12	I/O	48	TRDYN	84	I/O	120	I/O
13	I/O	49	DEVSELN	85	I/O	121	I/O
14	I/O	50	GND	86	I/O	122	GND
15	GND	51	STOPN	87	GND	123	I/O
16	GNTN	52	PERRN	88	I/O	124	I/O
17	I	53	SERRN	89	I	125	I/O
18	ACLK/I	54	GND	90	ACLK/I	126	GND
19	VCC	55	PAR	91	VCC	127	I/O
20	RSTN	56	CBEN[1]	92	I	128	I/O
21	CLK	57	AD[15]	93	GCLK/I	129	I/O
22	VCC	58	VCCIO	94	VCC	130	VCCIO
23	REQN	59	AD[14]	95	I/O	131	I/O
24	AD[31]	60	AD[13]	96	I/O	132	I/O
25	AD[30]	61	AD[12]	97	I/O	133	I/O
26	AD[29]	62	AD[11]	98	I/O	134	I/O
27	AD[28]	63	AD[10]	99	I/O	135	I/O
28	AD[27]	64	AD[9]	100	I/O	136	I/O
29	AD[26]	65	AD[8]	101	I/O	137	I/O
30	GND	66	GND	102	GND	138	GND
31	AD[25]	67	CBEN[0]	103	I/O	139	I/O
32	AD[24]	68	AD[7]	104	I/O	140	I/O
33	CBEN[3]	69	AD[6]	105	I/O	141	I/O
34	IDSEL	70	AD[5]	106	I/O	142	I/O
35	AD[23]	71	TRSTB/RRO	107	I/O	143	TDO/RCO
36	AD[22]	72	TMS	108	I/O	144	I/O

208 PQFP Pinout Diagram

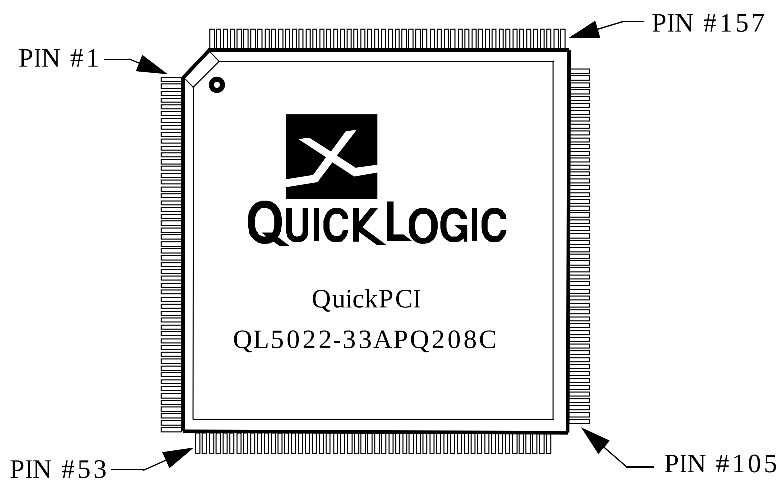


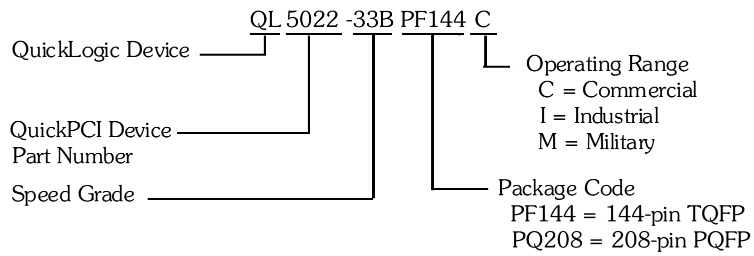
Figure 8: 208 PQFP Pinout Diagram

208 PQFP Pinout Diagram

Table 16: 208 PQFP Pin Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	37	AD[27]	73	GND	109	I/O	145	VCC	181	I/O
2	I/O	38	AD[26]	74	AD[11]	110	I/O	146	I/O	182	GND
3	I/O	39	AD[25]	75	AD[10]	111	I/O	147	GND	183	I/O
4	I/O	40	AD[24]	76	AD[9]	112	I/O	148	I/O	184	I/O
5	I/O	41	VCC	77	AD[8]	113	I/O	149	I/O	185	I/O
6	I/O	42	CBEN[3]	78	GND	114	VCC	150	I/O	186	I/O
7	I/O	43	GND	79	CBEN[0]	115	I/O	151	I/O	187	VCCIO
8	I/O	44	IDSEL	80	AD[7]	116	GND	152	I/O	188	I/O
9	I/O	45	AD[23]	81	AD[6]	117	I/O	153	I/O	189	I/O
10	VCC	46	AD[22]	82	AD[5]	118	I/O	154	I/O	190	I/O
11	I/O	47	AD[21]	83	VCCIO	119	I/O	155	I/O	191	I/O
12	GND	48	AD[20]	84	AD[4]	120	I/O	156	I/O	192	I/O
13	I/O	49	AD[19]	85	AD[3]	121	I/O	157	TCK	193	I/O
14	I/O	50	AD[18]	86	AD[2]	122	I/O	158	STM	194	I/O
15	I/O	51	AD[17]	87	AD[1]	123	I/O	159	I/O	195	I/O
16	I/O	52	AD[16]	88	AD[0]	124	I/O	160	I/O	196	I/O
17	I/O	53	CBEN[2]	89	I/O	125	I/O	161	I/O	197	I/O
18	I/O	54	TDI	90	I/O	126	I/O	162	I/O	198	I/O
19	I/O	55	FRAMEN	91	I/O	127	GND	163	GND	199	GND
20	I/O	56	IRDYN	92	I/O	128	I/O	164	I/O	200	I/O
21	I/O	57	TRDYN	93	I/O	129	I	165	VCC	201	VCC
22	I/O	58	DEVSELN	94	I/O	130	ACLK/I	166	I/O	202	I/O
23	GND	59	GND	95	GND	131	VCC	167	I/O	203	I/O
24	I/O	60	STOPN	96	I/O	132	I	168	I/O	204	I/O
25	RSTN	61	VCC	97	VCC	133	GCLK/I	169	I/O	205	I/O
26	ACLK/I	62	I/O	98	I/O	134	VCC	170	I/O	206	I/O
27	VCC	63	I/O	99	I/O	135	I/O	171	I/O	207	TDO
28	I	64	PERRN	100	I/O	136	I/O	172	I/O	208	I/O
29	CLK	65	I/O	101	I/O	137	I/O	173	I/O		
30	VCC	66	SERRN	102	I/O	138	I/O	174	I/O		
31	GNTN	67	PAR	103	TRSTB	139	I/O	175	I/O		
32	REQN	68	CBEN[1]	104	TMS	140	I/O	176	I/O		
33	AD[31]	69	AD[15]	105	I/O	141	I/O	177	GND		
34	AD[30]	70	AD[14]	106	I/O	142	I/O	178	I/O		
35	AD[29]	71	AD[13]	107	I/O	143	I/O	179	I/O		
36	AD[28]	72	AD[12]	108	I/O	144	I/O	180	I/O		

Ordering Information



Revision History

Table 17: Revision History

Revision	Date	Comments
A	November 2002	Preliminary release
B	March 2003	Bernhard Andretzky, Claire Tu, Kathleen Murchek

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