DATA SHEET

OKI

ML54053

NAND Flash Memory Controller

PRELIMINARY

SECOND EDITION

ISSUE DATE : JAN. 1999

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Preliminary

OKI Semiconductor

This version: Jan. 1999
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ML54053

NAND Flash Memory Controller

The ML54053 is a controller that integrates into a single chip a host interface that conforms to PCMCIA, the necessary functions to control NAND memory, and a microcontroller.

Internal 256 byte RAM is provided for storage of the card information structure (CIS).

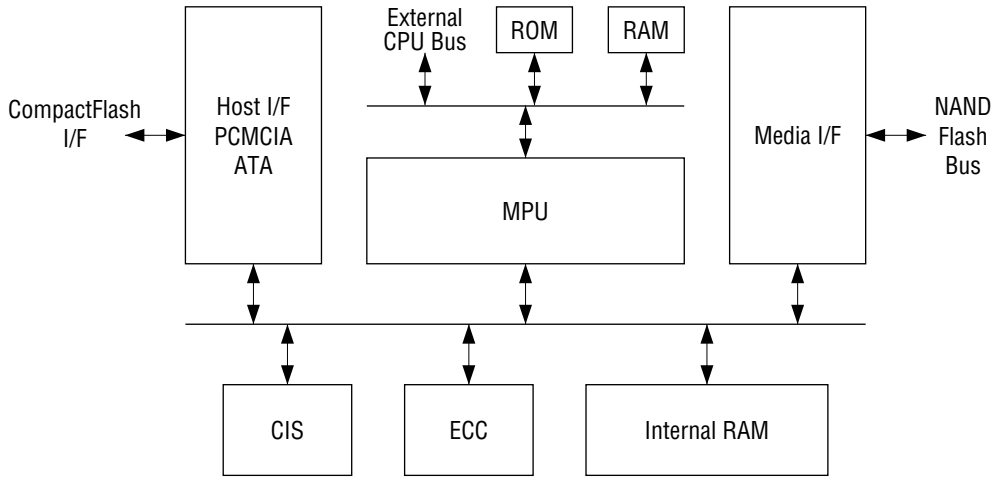
A maximum of 4 chips of 64 Mbit or larger NAND flash memory can be controlled.

CompactFlash™ is a trademark of SanDisk Corporation.

1. FEATURES

- Single chip controller with internal microcontroller (min. 4 cycles/instruction execution)
- Operating voltage: 3.3 V, Interface voltage: 3.3 V/5 V
- Internal 256B RAM for card information structure (CIS) storage
- Conforms to CompactFlash specification
- Auto-sleep mode support
- True IDE Mode support
- ECC system by BCH code (3-bit random error correction is possible for user data and ECC data)
- Substitute control function (defect management function)
- Debug mode support
- High-speed operation via dual port bus control
- Low power consumption due to single chip controller
- Control of four NAND flash memories (64MB to 512MB) is possible
- 120-pin TQFP package (TQFP120-P-1414-0.40-K)

2. BLOCK DIAGRAM



3. PIN SPECIFICATIONS

Refer to Section 11, "Application Example" for specific connection examples.

3.1 Host Interface

Signal Name	Type	Pin Count	Description
ha [10:0]	I	11	Address bus (A10 is MSB, A0 is LSB)
hd [15:0]	B	16	Data bus (D15 is MSB, D0 is LSB)
hcen [2:1]	I	2	Card enable signal (hcen1 controls even addresses and hcen2 controls odd addresses. The combination of ha0, hcen1 and hcen2 allows even/odd addresses to be accessed by hd[7:0].)
hiordn	I	1	I/O read signal (control signal to read data from ATA registers)
hiowrn	I	1	I/O write signal (control signal to write data to ATA registers)
hoen	I	1	Output enable signal
hwen	I	1	Write enable signal
hregn	I	1	Register select & I/O Enable signal
hirqn	O	1	Interrupt request signal (when the card is configured as an I/O card)
hstschgn	O	1	Card status change signal (signal to change the status of the configuration status register)
hinpackn	O	1	Input port acknowledge signal (acknowledge signal during I/O read)
hiois16n	O	1	16-bit address enable signal (when the card is configured as an I/O card, this signal indicates that 16-bit addresses are enabled)
hwaitn	O	1	Wait signal
hspkr	B	1	Audio digital waveform signal
hrst	I	1	Reset signal
hcseln	I	1	Cable select signal (used only in True IDE Mode, GND: Master, X: Slave)
		Total 42 pins	

I: Input, O: Output, B: Bidirectional

3.2 NAND Flash Memory Interface

Signal Name	Type	Pin Count	Description
maio [7:0]	B	8	Port A I/O bus
macle	O	1	Port A command latch enable signal (signal to control latching of an operation command into a device)
maale	O	1	Port A address latch enable signal (signal to control latching of an address or input data into a device)
maren	O	1	Port A read enable signal
mawen	O	1	Port A write enable signal (signal to latch data into a device)
marbn	I	1	Port A ready/busy signal (signal to check internal status of device)
mbio [7:0]	B	8	Port B I/O bus
mbcle	O	1	Port B command latch enable signal (signal to control latching of an operation command into a device)
mbale	O	1	Port B address latch enable signal (signal to control latching of an address or input data into a device)
mbren	O	1	Port B read enable signal
mbwen	O	1	Port B write enable signal (signal to latch data into a device)
mbrbn	I	1	Port B ready/busy signal (signal to check internal status of device)
mcen [3:0]	O	4	Chip enable signals
mwpn	O	1	Write protect signal (signal to forcibly prohibit write and erase operations)

Total 31 pins

3.3 Extended Bus Interface

The extended bus interface is a signal line for the ML54053's internal microcontroller. The extended bus interface is used for purposes such as debugging.

Signal Name	Type	Pin Count	Description
xah [15:8]	B	8	Address bus for extended bus
xad [7:0]	B	8	Address/data bus for extended bus
xrd	B	1	Read signal for extended bus
xwr	B	1	Write signal for extended bus
xale	B	1	Address latch enable signal for extended bus
xpsen	I	1	Program store enable signal for extended bus
xint	O	1	Interrupt signal for extended bus
xrst	O	1	Reset signal for extended bus
xclk	O	1	Clock signal for extended bus

Total 23 pins

* In an external ROM connection mode, xah, xad, xrd, xwr, and xale are used to connect to external ROM.

3.4 Other Interfaces

Signal Name	Type	Pin Count	Description
txd/pcfg [0]	B	1	Serial data I/O and chip mode setting
rxd/pcfg [1]	I	1	
porn	I	1	Power-on-reset signal (connect to power monitor circuit)
xin	I	1	Clock I/O (connect a crystal oscillator between xin and xout)
xout	O	1	

Total 5 pins

* The chip mode is determined depending upon the status of pcfg[1:0] when the porn signal rises.
pcfg[1:0] = 11 : Normal mode
pcfg[1:0] = 01 : External CPU connection mode
pcfg[1:0] = 10 : External ROM connection mode
pcfg[1:0] = 00 : Test mode (normally not used)

3.5 Power Supply

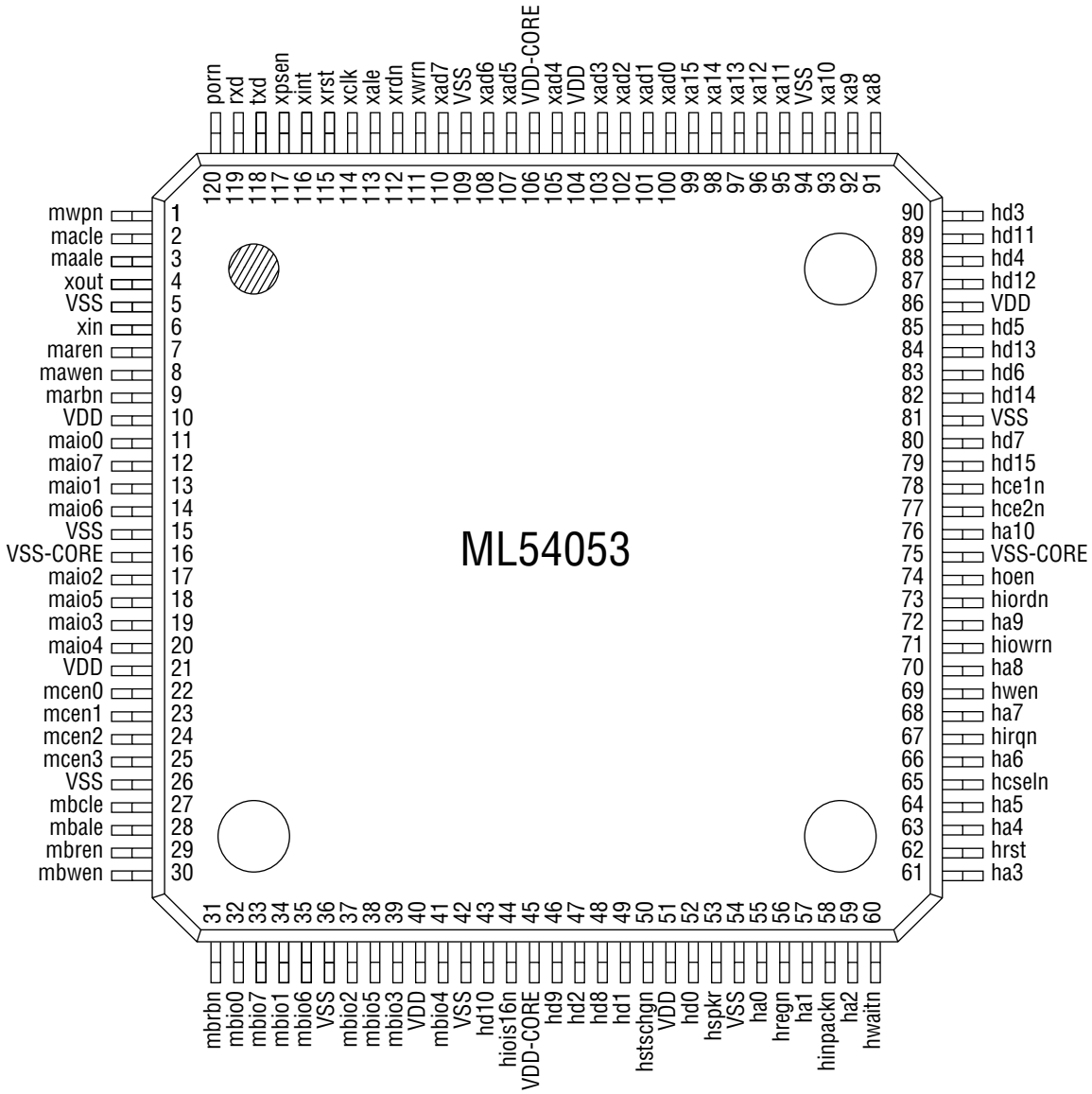
Signal Name	Type	Pin Count	Description
VDD-CORE	DC	2	Power supply for core
VSS-CORE	DC	2	
VDD	DC	6	Power supply for I/O pad
VSS	DC	9	

Total 19 pins

3.6 Pin Totals

Host Interface	42
NAND Flash Memory Interface	31
Extended Bus Interface	23
Other Interfaces	5
Power Supply	19
Total	120

3.7 Pin Configuration



120-Pin Plastic TQFP

4. FUNCTIONS

(1) Sector Formatter and Sequencer
The sector formatter and sequencer control the logical format of the NAND flash memory and efficiently perform defect management (substitute processing).

(2) CompactFlash Interface
The PCMCIA interface conforms to CompactFlash specification.

(3) Chip Modes
An external ROM connection mode for the ML54053's internal microcontroller and an external CPU connection mode are supported. With these modes, evaluation can be performed efficiently.

(4) Auto-Sleep Mode
If there is no access from the host over a specific period of time, operation automatically transfers to the sleep mode.

(5) Dual Port Bus Control Mode
When erasing data or writing the same data, two port buses (Port A, Port B) can be utilized simultaneously for high-speed operation.

5. ATA REGISTERS

When a mode such as memory mode or I/O mode is configured, the host must use different addresses for access.

5.1 Memory Mapped Configuration

-CE1	-CE2	-REG	A10	A9-A4	A3-A0	Read (-OE = L)		Write (-WE = L)	
0	0	1	0	*	(000x)	16-bit Data	D15 : D0	16-bit Data	D15 : D0
0	1	1	0	*	0h	8-bit Data	D7 : D0	8-bit Data	D7 : D0
0	1	1	0	*	1h	Error	D7 : D0	Features	D7 : D0
1	0	1	0	*	(000x)	Error	D15 : D8	Features	D15 : D8
0	1	1	0	*	2h	Sector Count	D7 : D0	Sector Count	D7 : D0
0	1	1	0	*	3h	Sector Number	D7 : D0	Sector Number	D7 : D0
1	0	1	0	*	(001x)	Sector Number	D15 : D8	Sector Number	D15 : D8
0	1	1	0	*	4h	Cylinder Low	D7 : D0	Cylinder Low	D7 : D0
0	1	1	0	*	5h	Cylinder High	D7 : D0	Cylinder High	D7 : D0
1	0	1	0	*	(010x)	Cylinder High	D15 : D8	Cylinder High	D15 : D8
0	1	1	0	*	6h	Drive/Head	D7 : D0	Drive/Head	D7 : D0
0	1	1	0	*	7h	Status	D7 : D0	Command	D7 : D0
1	0	1	0	*	(011x)	Status	D15 : D8	Command	D15 : D8
0	0	1	0	*	(100x)	Duplicate Data	D15 : D0	Duplicate Data	D15 : D0
0	1	1	0	*	8h	Duplicate Even	D7 : D0	Duplicate Even	D7 : D0
0	1	1	0	*	9h	Duplicate Odd	D7 : D0	Duplicate Odd	D7 : D0
1	0	1	0	*	(100x)	Duplicate Odd	D15 : D8	Duplicate Odd	D15 : D8
0	1	1	0	*	Dh	Duplicate Error	D7 : D0	Duplicate Features	D7 : D0
1	0	1	0	*	(110x)	Duplicate Error	D15 : D8	Duplicate Features	D15 : D8
0	1	1	0	*	Eh	Alternate Status	D7 : D0	Device Control	D7 : D0
0	1	1	0	*	Fh	Drive Address	D7 : D0	Not Used	
1	0	1	0	*	(111x)	Drive Address	D15 : D8	Not Used	
0	0	1	1	*	*	16-bit Data	D15 : D0	16-bit Data	D15 : D0
0	1	1	1	*	(xxx0)	Even Data	D7 : D0	Even Data	D7 : D0
0	1	1	1	*	(xxx1)	Odd Data	D7 : D0	Odd Data	D7 : D0
1	0	1	1	*	*	Odd Data	D15 : D8	Odd Data	D15 : D8

* Don't care

5.2 I/O Mapped 16 Contiguous Registers Configuration

-CE1	-CE2	-REG	A9-A4	A3-A0	Read (-IORD = L)		Write (-IOWR = L)	
0	0	0	*	0h	16-bit Data	D15 : D0	16-bit Data	D15 : D0
0	1	0	*	0h	8-bit Data	D7 : D0	8-bit Data	D7 : D0
0	1	0	*	1h	Error	D7 : D0	Features	D7 : D0
1	0	0	*	(000x)	Error	D15 : D8	Features	D15 : D8
0	1	0	*	2h	Sector Count	D7 : D0	Sector Count	D7 : D0
0	1	0	*	3h	Sector Number	D7 : D0	Sector Number	D7 : D0
1	0	0	*	(001x)	Sector Number	D15 : D8	Sector Number	D15 : D8
0	1	0	*	4h	Cylinder Low	D7 : D0	Cylinder Low	D7 : D0
0	1	0	*	5h	Cylinder High	D7 : D0	Cylinder High	D7 : D0
1	0	0	*	(010x)	Cylinder High	D15 : D8	Cylinder High	D15 : D8
0	1	0	*	6h	Drive/Head	D7 : D0	Drive/Head	D7 : D0
0	1	0	*	7h	Status	D7 : D0	Command	D7 : D0
1	0	0	*	(011x)	Status	D15 : D8	Command	D15 : D8
0	0	0	*	8h	Duplicate Data	D15 : D0	Duplicate Data	D15 : D0
0	1	0	*	8h	Duplicate Even	D7 : D0	Duplicate Even	D7 : D0
0	1	0	*	9h	Duplicate Odd	D7 : D0	Duplicate Odd	D7 : D0
1	0	0	*	(100x)	Duplicate Odd	D15 : D8	Duplicate Odd	D15 : D8
0	1	0	*	Dh	Duplicate Error	D7 : D0	Duplicate Features	D7 : D0
1	0	0	*	(110x)	Duplicate Error	D15 : D8	Duplicate Features	D15 : D8
0	1	0	*	Eh	Alternate Status	D7 : D0	Device Control	D7 : D0
0	1	0	*	Fh	Drive Address	D7 : D0	Not Used	
1	0	0	*	(111x)	Drive Address	D15 : D8	Not Used	

* Don't care

5.3 Primary I/O Mapped Configuration

-CE1	-CE2	-REG	A9-A0	Read (-IORD = L)		Write (-IOWR = L)	
0	0	0	1F0h	16-bit Data	D15 : D0	16-bit Data	D15 : D0
0	1	0	1F0h	8-bit Data	D7 : D0	8-bit Data	D7 : D0
0	1	0	1F1h	Error	D7 : D0	Features	D7 : D0
1	0	0	1F0h/1F1h	Error	D15 : D8	Features	D15 : D8
0	1	0	1F2h	Sector Count	D7 : D0	Sector Count	D7 : D0
0	1	0	1F3h	Sector Number	D7 : D0	Sector Number	D7 : D0
1	0	0	1F2h/1F3h	Sector Number	D15 : D8	Sector Number	D15 : D8
0	1	0	1F4h	Cylinder Low	D7 : D0	Cylinder Low	D7 : D0
0	1	0	1F5h	Cylinder High	D7 : D0	Cylinder High	D7 : D0
1	0	0	1F4h/1F5h	Cylinder High	D15 : D8	Cylinder High	D15 : D8
0	1	0	1F6h	Drive/Head	D7 : D0	Drive/Head	D7 : D0
0	1	0	1F7h	Status	D7 : D0	Command	D7 : D0
1	0	0	1F6h/1F7h	Status	D15 : D8	Command	D15 : D8
0	1	0	3F6h	Alternate Status	D7 : D0	Device Control	D7 : D0
0	1	0	3F7h	Drive Address	D7 : D0	Not Used	
1	0	0	3F6h/3F7h	Drive Address	D15 : D8	Not Used	

5.4 Secondary I/O Mapped Configuration

-CE1	-CE2	-REG	A9-A0	Read (-IORD = L)		Write (-IOWR = L)	
0	0	0	170h	16-bit Data	D15 : D0	16-bit Data	D15 : D0
0	1	0	170h	8-bit Data	D7 : D0	8-bit Data	D7 : D0
0	1	0	171h	Error	D7 : D0	Features	D7 : D0
1	0	0	170h/171h	Error	D15 : D8	Features	D15 : D8
0	1	0	172h	Sector Count	D7 : D0	Sector Count	D7 : D0
0	1	0	173h	Sector Number	D7 : D0	Sector Number	D7 : D0
1	0	0	172h/173h	Sector Number	D15 : D8	Sector Number	D15 : D8
0	1	0	174h	Cylinder Low	D7 : D0	Cylinder Low	D7 : D0
0	1	0	175h	Cylinder High	D7 : D0	Cylinder High	D7 : D0
1	0	0	174h/175h	Cylinder High	D15 : D8	Cylinder High	D15 : D8
0	1	0	176h	Drive/Head	D7 : D0	Drive/Head	D7 : D0
0	1	0	177h	Status	D7 : D0	Command	D7 : D0
1	0	0	176h/177h	Status	D15 : D8	Command	D15 : D8
0	1	0	376h	Alternate Status	D7 : D0	Device Control	D7 : D0
0	1	0	377h	Drive Address	D7 : D0	Not Used	
1	0	0	376h/377h	Drive Address	D15 : D8	Not Used	

5.5 True IDE Mapped Configuration

• Command Block Register

-CE1	-CE2	-REG	A9-A3	A2-A0	Read (-IORD = L)		Write (-IOWR = L)	
0	1	0	*	0h	16-bit Data	D15 : D0	16-bit Data	D15 : D0
0	1	0	*	1h	Error	D7 : D0	Features	D7 : D0
0	1	0	*	2h	Sector Count	D7 : D0	Sector Count	D7 : D0
0	1	0	*	3h	Sector Number	D7 : D0	Sector Number	D7 : D0
0	1	0	*	4h	Cylinder Low	D7 : D0	Cylinder Low	D7 : D0
0	1	0	*	5h	Cylinder High	D7 : D0	Cylinder High	D7 : D0
0	1	0	*	6h	Drive/Head	D7 : D0	Drive/Head	D7 : D0
0	1	0	*	7h	Status	D7 : D0	Command	D7 : D0
0	0	0	*	(xxx)	Not Used		Not Used	

* Don't care

• Control Block Register

-CE1	-CE2	-REG	A9-A3	A2-A0	Read (-IORD = L)		Write (-IOWR = L)	
1	1	0	*	(xxx)	High Impedance		Not Used	
1	0	0	*	(0xx)	High Impedance		Not Used	
1	0	0	*	(10x)	High Impedance		Not Used	
1	0	0	*	6h	Alternate Status	D17 : D0	Device Control	D7 : D0
1	0	0	*	7h	Drive Address	D7 : D0	Not Used	

* Don't care

5.6 ATA Registers

ATA registers realize functions of the PC Card ATA Specifications.

5.6.1 Data Register (Write/Read)

This 16-bit or 8-bit register is used in the transfer of data blocks between the internal data buffer and the host. Data can be transferred via consecutive 16-bit or 8-bit accesses to the data register.

5.6.2 Error Register (Read Only)

Additional information regarding the cause of a processing error in the previously executed command is indicated. If the error bit of the status register has been set, the host must examine this register.

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

BBK : This bit is set when a Bad Block is detected.
UNC : This bit is set when an Uncorrectable Error is encountered.
IDNF : The requested sector ID is in error or cannot be found.
ABRT : This bit is set if the command has been aborted or when an invalid command has been issued.
AMNF : This bit is set in case of a general error.

5.6.3 Feature Register (Write Only)

This register is used to write information related to commands.

D7	D6	D5	D4	D3	D2	D1	D0
Feature Bytes							

5.6.4 Sector Count Register (Write/Read)

This register is used to specify the number of sectors or address of logical blocks to be processed by a command. By reading this register after a command has been completed, the host can check the number of sectors not processed by the command.

D7	D6	D5	D4	D3	D2	D1	D0
Sector Count							

5.6.5 Sector Number Register (Write/Read)

This register is used to specify the sector number or logical block address where processing by the command will begin. By reading this register after a command has been completed, the host can check the sector number or logical block address processed by the command.

D7	D6	D5	D4	D3	D2	D1	D0
Sector Number/LBA7-LBA0							

5.6.6 Cylinder Low Register (Write/Read)

This register is used to specify the lower cylinder number or the logical block address where processing by the command will begin. By reading this register after a command has been completed, the host can check the last lower cylinder number or logical block address that was processed by the command.

D7	D6	D5	D4	D3	D2	D1	D0
Cylinder Low/LBA15-LBA8							

5.6.7 Cylinder High Register (Write/Read)

This register is used to specify the upper cylinder number or the logical block address where processing by the command will begin. By reading this register after a command has been completed, the host can check the last upper cylinder number or logical block address that was processed by the command.

D7	D6	D5	D4	D3	D2	D1	D0
Cylinder High/LBA23-LBA16							

5.6.8 Drive Head Register (Write/Read)

This register is used to specify the head number or the logical block address where processing by the command will begin. By reading this register after a command has been completed, the host can check the last upper head number or logical block address that was processed by the command.

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV#	HS3/LBA27	HS2/LBA26	HS1/LBA25	HSO/LBA24

LBA: 1: LBA (logical block address) mode
0: CHS address mode

DRV#: card number 0: drive 0 is selected
1: drive 1 is selected

If the value of the Drive# bit of the socket copy register matches the value of this bit, this controller will execute the command.

5.6.9 Status Register & Alternate Status Register (Read Only)

This register indicates the internal status of the controller. When the host reads this register, the controller clears pending interrupt requests. However, even if the alternate status register is read, interrupts requests will not be cleared.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	IDX	ERR

BUSY: This bit is set in the following cases:
- from the time when the host writes a command to the command register until processing of the command is completed
- when hardware and software resets have been executed from the host

RDY: This bit indicates Drive Ready.

DWF: This bit is set when an error related to substitute processing occurs during access to the internal flash memory. If this bit is set, commands that follow may not execute properly.

DSC: This bit is always set to 1.

DRQ: During execution of a command that involves data transfer, this bit is set once the transfer preparations are made.

CORR: This bit indicates that a correctable error has occurred during access to flash memory.

IDX: This bit is always set to 0.

ERR: This bit is set when an error occurs during command execution. Detailed information is set in the error register.

5.6.10 Device Control Register (Write Only)

This register is used to control interrupt requests from the card and to specify software reset.

D7	D6	D5	D4	D3	D2	D1	D0
X				1	SRST	-IEN	0

SRST: While this bit is 1, the controller is in the reset state.

-IEN: 1: Interrupt signal mask, 0: Interrupt signal non-mask

5.6.11 Command Register (Write Only)

This register is used to set the command code.

D7	D6	D5	D4	D3	D2	D1	D0
Command Code							

6. COMPACTFLASH INTERFACE

6.1 ATA Commands (Standard)

Supported ATA commands are listed below.

Command	Code	FR	SC	SN	CY	DH	C/R/W
Check Power Mode	98h, E5h	—	—	—	—	○	C
Execute Drive Diagnostic	90h	—	—	—	—	○	C
Format Track	50h	—	○	—	○	○	W
Identify Drive	ECh	—	—	—	—	○	R
Idle	97h, E3h	—	○	—	—	○	C
Idle Immediate	95h, E1h	—	—	—	—	○	C
Initialize Drive Parameters	91h	—	○	—	—	○	C
Read Buffer	E4h	—	—	—	—	○	R
Read Long Sector	22h, 23h	—	—	○	○	○	R
Read Multiple	C4h	—	○	○	○	○	R
Read Sector (s)	20h, 21h	—	○	○	○	○	R
Read Verify Sector (s)	40h, 41h	—	○	○	○	○	C
Recalibrate	1xh	—	—	—	—	○	C
Seek	7xh	—	—	○	○	○	C
Set Features	EFh	○	—	—	—	○	C
Set Multiple Mode	C6h	—	○	—	—	○	C
Set Sleep Mode	99h, E6h	—	—	—	—	○	C
Standby	96h, E2h	—	—	—	—	○	C
Standby Immediate	94h, E0h	—	—	—	—	○	C
Write Buffer	E8h	—	—	—	—	○	W
Write Long Sector	32h, 33h	—	—	○	○	○	W
Write Multiple	C5h	—	○	○	○	○	W
Write Sector (s)	30h, 31h	—	○	○	○	○	W

FR: Features register SC: Sector count register SN: Sector number register
CY: Cylinder register DH: Drive/head register
C/R/W: C - Control, R - Read, W - Write
○ : modified, valid — : invalid

6.2 Commands for CompactFlash

Supported CompactFlash commands are listed below.

Command	Code	FR	SC	SN	CY	DH	C/R/W
Request Sense	03h	—	—	—	—	○	C
Erase Sector (s)	C0h	—	○	○	○	○	C
Translate Sector	87h	—	○	○	○	○	R
Wear Level	F5h	—	—	—	—	○	C
Write Multiple w/o Erase	CDh	—	○	○	○	○	W
Write Sector (s) w/o Erase	38h	—	○	○	○	○	W

6.3 Vendor-Unique Commands

Vendor-unique commands can be executed by writing "FFh" data to the command register when a value from the below chart has been written to the feature register.

Command	Code	FR	Description	C/R/W
Low Level Format	FFh	Undefined	Initialization of substitute information, all sectors	C
Change Information	FFh	Undefined	Change CIS/Identify information	W
Change Physical Cylinder	FFh	Undefined	Set maximum value of physical cylinder	C
Read All	FFh	Undefined	Read 528 bytes of the specified page	R
Un Lock	FFh	Undefined	Vendor-unique commands that follow are valid	C

Change Physical Cylinder: Sets the maximum value of the user area that is accessible from the host. For details, refer to section 6.6, "Number of Installed Memory Chips and CHS Structure."

6.4 Card Information Structure

The desired card information structure (CIS) can be stored by the change information command.

6.5 Identify Information

The desired identify information can be stored by the change information command.

6.6 Number of Installed Memory Chips and CHS Structure

NAND flash memory is erased in block units. Since block erasing is also performed during a 1-page (sector) write, efficiency is increased during write operations by serially addressing sectors within the same block.

The CHS structure and number of installed memory chips when using 64, 128, 256 and 512 Mbit memory are listed below (where C is the default value). The C value of the CHS address can be set by the change physical cylinder command (a vendor-unique command).

• 64 Mbit Memory

Capacity	No. of Chips	CHS			LBA Max. (Hex)
		C	H	S	
8	1	1000	1	16	16000 (3E80)
16	2	1000	1	32	32000 (7D00)
32	4	1000	2	32	64000 (FA00)

• 128 Mbit Memory

Capacity	No. of Chips	CHS			LBA Max. (Hex)
		C	H	S	
16	1	1000	1	32	32000 (7D00)
32	2	1000	1	64	64000 (FA00)
64	4	1000	2	64	128000 (1F400)

• 256 Mbit Memory

Capacity	No. of Chips	CHS			LBA Max. (Hex)
		C	H	S	
32	1	1000	2	32	64000 (FA00)
64	2	1000	2	64	128000 (1F400)
128	4	1000	4	64	256000 (3E800)

• 512 Mbit Memory

Capacity	No. of Chips	CHS			LBA Max. (Hex)
		C	H	S	
64	1	1000	4	32	128000 (1F400)
128	2	1000	4	64	256000 (3E800)
256	4	1000	8	64	512000 (7D000)

6.7 Modes

6.7.1 Memory Mapped

In the memory mapped mode, ATA registers appear in the 0 to 2K window of common memory space.

6.7.2 I/O Mapped 16 Contiguous Registers

In the I/O mapped 16 contiguous registers mode, contiguous ATA registers appear in I/O space.

6.7.3 Primary I/O Mapped

In the primary I/O mapped mode, ATA registers appear in 1F0h to 1F7h and 3F6h to 3F7h of the standard I/O address space.

6.7.4 Secondary I/O Mapped

In the secondary I/O mapped mode, ATA registers appear in 170h to 177h and 376h to 377h of the standard I/O address space.

6.7.5 True IDE

This mode is compatible with True IDE Mode.

7. CHIP MODES

7.1 Types

There are four types of chip modes. Note that default pin assignments change depending upon the chip mode.

- Normal Mode
  This mode is normally used.

- External ROM Connection Mode
  This mode is used for connection to external ROM.

- External CPU Connection Mode
  This mode is used for debugging. When this mode is activated, the internal microcontroller does not operate.

- Test Mode
  This mode is used for testing. The test mode is not normally used.

7.2 Settings

Chip modes are determined by the status of pcfg[1:0] when the power-on-reset signal (porn signal) rises.

pcfg [1 : 0] = 11	Normal Mode
pcfg [1 : 0] = 01	External CPU Connection Mode
pcfg [1 : 0] = 10	External ROM Connection Mode
pcfg [1 : 0] = 00	Test Mode

7.3 Pin Assignment

Interface	Signal Name	Normal		External ROM Connection		External CPU Connection	
Extended Bus	xah [15 : 8]	(Low-Level)	O	xah [15 : 8]	I/O	xah [15 : 8]	I/O
Extended Bus	xad [7 : 0]	(Low-Level)	O	xad [7 : 0]	I/O	xad [7 : 0]	I/O
Extended Bus	xrd	(Low-Level)	O	xrd	O	xrd	I
Extended Bus	xwr	(Low-Level)	O	xwr	O	xwr	I
Extended Bus	xale	(Low-Level)	O	xale	O	xale	I
Extended Bus	xint	(Low-Level)	O	(Low-Level)	O	xint	O
Extended Bus	xpsenn	(Low-Level)	I	(Low-Level)	I	xpsenn	I
Extended Bus	xrst	(Low-Level)	O	(Low-Level)	O	xrst	O
Extended Bus	xclk	(Low-Level)	O	(Low-Level)	O	xclk	O

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Parameter		Symbol	Condition	Rating	Unit
Power Supply Voltage		V_{DD}	Tj = 25°C The standard is V_{SS} = 0 V	–0.3 to +4.6	V
Input Voltage	Normal Buffer	V_I		–0.3 to V_{DD} + 0.3	
	5 V Tolerant Buffer			–0.3 to +6.0	
Output Voltage	Normal Buffer	V_O		–0.3 to V_{DD} + 0.3	
	5 V Tolerant Buffer			–0.3 to +6.0	
Input Current	Normal Buffer	I_I		–10 to +10	mA
	5 V Tolerant Buffer			–6 to +6	
Storage Temperature		Tstg		–65 to +150	°C

8.2 Recommended Operating Conditions

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{DD}	3.0 to 3.6	V
Operating Temperature	Tj	–40 to +85	°C

8.3 DC Characteristics

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, Tj = –40 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
High Level Input Voltage	V_{IH}	TTL normal input	2.0	—	V_{DD} + 0.3	V
		5 V tolerant input	2.0	—	5.5	
Low Level Input Voltage	V_{IL}	—	–0.3	—	+0.8	
Schmitt Trigger Threshold Voltage	V_{t+}	—	—	1.5	2.0	
	V_{t-}	—	0.7	1.0	—	
	ΔV_t	$V_{t+} - V_{t-}$	0.4	0.5	—	
High Level Output Voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	—	
		I_{OL} = 2, 4, 8 mA	2.4	—	—	
Low Level Output Voltage	V_{OL}	I_{OH} = –100 µA	—	—	0.2	
		I_{OL} = 2, 4, 8 mA	—	—	0.4	
High Level Input Current	I_{IH}	V_{IH} = V_{DD}	—	0.01	1	µA
Low Level Input Current	I_{IL}	V_{IL} = V_{SS}	–1	+0.01	—	
		(50 kΩ pull-up)	–170	–66	–15	
Output Leakage Current	I_{OZH}	V_{OL} = V_{DD}	—	0.01	1	
	I_{OZL}	V_{OL} = V_{SS}	–1	–0.01	—	
		(50 kΩ pull-up)	–170	–66	–15	
Standby Power Supply Current	I_{DDS}	Output open	–10	—	+10	

Note 1 : Listed values are for a normal buffer and a 5 V tolerant buffer unless otherwise specified.

Note 2 : Typical values are indicated for a typical condition at V_{DD} = 3.3 V and Tj = 25°C.

9. BUS SPECIFICATIONS

9.1 I/O Mode

The I/O mode conforms to CompactFlash and IDE specifications.

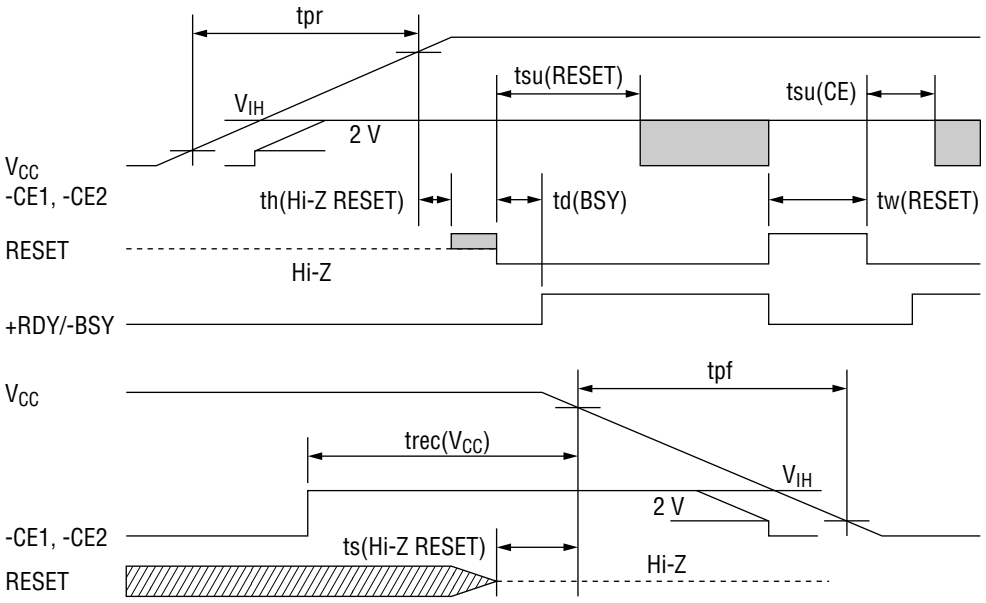
9.2 Bus Timing Specifications

Bus timing conforms to CompactFlash, IDE and NAND flash memory specifications.

9.3 Power ON/OFF, Reset, Busy Timing

Parameter	Symbol	Condition	Specified Value		
			Min.	Max.	Unit
-CE Signal Level	V_I (CE)	0 V ≤ V_{CC} < 2.0 V	0	V_I Max.	V
		2.0 V ≤ V_{CC} < V_{IH}	V_{CC} – 0.1	V_I Max.	
		V_{IH} ≤ V_{CC}	V_{IH}	V_I Max.	
Reset Setup Time	tsu (RESET)	—	TBD		ms
Ready Release Delay Time	td (BSY)	—	TBD		ms
-CE Recovery Time	trec (V_{CC})	—	TBD		ms
V_{CC} Rise Time	tpr	10%→(V_{CC} + 5%) 90% *1	TBD		ms
V_{CC} Fall Time	tpf	(V_{CC} – 5%) 90%→10% *1	TBD		ms
Reset Width	tw (RESET)	—	TBD		ms
	th (Hi-Z RESET)	—	TBD		ms
	ts (Hi-Z RESET)	—	TBD		ms

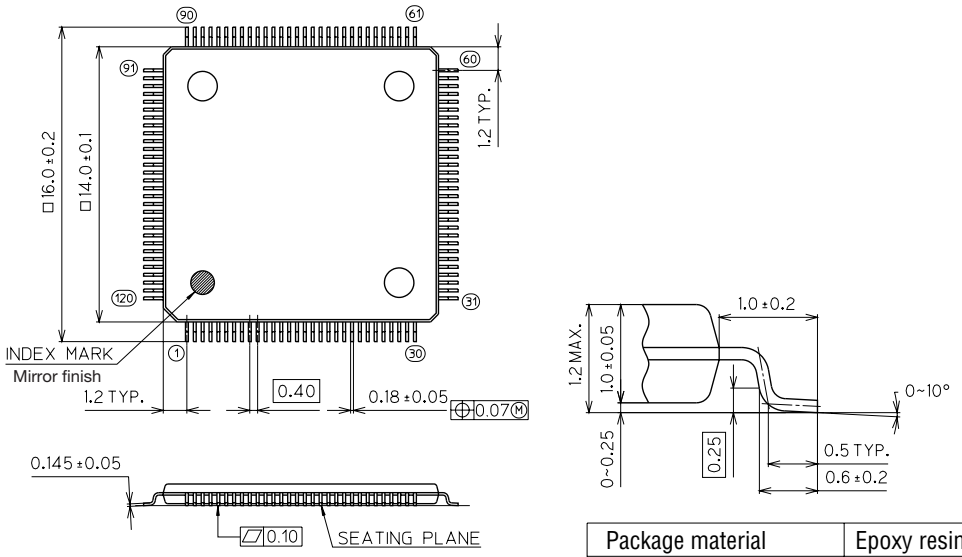
*1: tpr and tpf are defined as the time of the "straight-line change from 10% to 90% of V_{CC}", and vice-versa. Even if the rise and fall waveforms are non-linear, the maximum slope of the waveform must meet these specifications.



10. PACKAGE DIMENSIONS

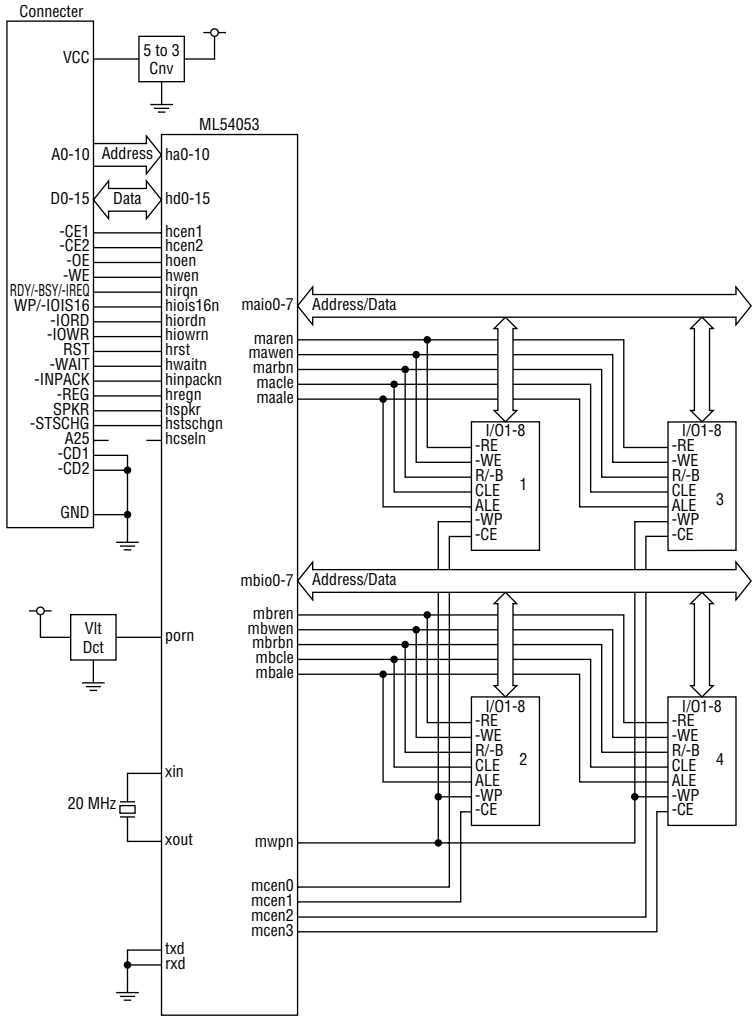
(Unit : mm)

TQFP120-P-1414-0.40-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature, and times).

11. APPLICATION EXAMPLE