DATA SHEET

O K I A S I C P R O D U C T S

MG73/74Q and MSM98Q/99Q 0.35µm Customer Structured Arrays

August 2002

Oki Semiconductor

CONTENTS

Oki Semiconductor

MG73Q/74Q and MSM98Q/99Q

0.35μm Customer Structured Arrays

DESCRIPTION

Oki's 0.35μm Application-Specific Integrated Circuit (ASIC) products are available in Customer Structured Array (CSA) architectures with 0.60-μm or 100-μm I/O pad pitch. Both the MG73Q000 and the MSM98Q000 series use a three-layer metal process on 0.35μm drawn (0.27μm L-effective) CMOS technology. The MG74Q and MSM99Q series uses the same base-array architecture as the MG73Q or MSM99Q series respectively, but offers four metal layers instead of three. The semiconductor process is adapted from Oki's production-proven 64-Mbit DRAM manufacturing process.

The 0.35-μm family provides significant performance, density, and power improvement over previous 0.4 and 0.5μm technologies. The Oki 0.35-μm family operates using 3-V V_{DD} core with optimized 3-V I/O buffers and 3-V I/O buffers that are 5-V tolerant. The MG73Q/74Q series contains 21 array bases, offering up to 868 I/O pads and over 2 M raw gates. The MSM98Q/99Q series contains 18 array bases, offering up to 432 I/O pads and over 1.4M raw gates. These CSA array sizes are designed to fit the most popular quad flat pack (QFP), low profile QFPs (LQFPs), thin QFPs (TQFPs), and plastic ball grid array (PBGA) packages.

The 3-layer-metal MG73Q and MSM98Q and 4-layer-metal MG74Q and MSM99Q CSA series offer a wide span of gate and I/O counts. Oki uses the Artisan Components memory compiler which provides high performance, embedded synchronous single- and dual-port RAM macrocells for CSA designs. As such, the MG73Q/74Q and MSM98Q/99Q series is suited to memory-intensive ASICs and high-volume designs where fine tuning of package size produces significant cost or real-estate savings.

FEATURES

- 0.35μm drawn 3-, and 4-layer metal CMOS
- Optimized 3.3-V core
- Optimized 3-V I/O and 3-V I/O that is 5-V tolerant
- 0.60-μm and 100-μm I/O pitch
- CSA architecture
- 77-ps typical gate propagation delay (for a 4x-drive inverter gate with a fan-out of 2 and 0 mm of wire, operating at 3.3 V)
- Up to 2.0 M raw gates and 868 I/O pads
- User-configurable I/O with V_{SS}, V_{DD}, TTL, 3-state, and 1- to 24-mA options
- Slew-rate-controlled outputs for low-radiated noise
- Clock tree drivers which reduces the maximum skew for clock signals
- User-configurable single- and dual-port memories
- Specialized macrocells including phase-locked loop (PLL), LVDS, pseudo-emitter coupled logic (PECL), and peripheral component interconnect (PCI) cells
- Floorplanning for front-end simulation, back-end layout controls, and link to synthesis
- Joint Test Action Group (JTAG) boundary scan and scan path Automatic Test Pattern Generation (ATPG)
- Support for popular CAE systems including Cadence, Exemplar, Gambit, IKOS, Mentor Graphics, Model Technology, Inc. (MTI), Zycad, Synopsys, and VIEWLogic

MG73Q/74Q and MSM98Q/99Q FAMILY MASTERSLICES

MG73Q/74Q Family Listing

E/A		# of	Usable Gate				
Product Name	Base Array						
MG7XQ	B7XQ	Pads	MG73Q	MG74Q	Raw Gate	Column	Row
B02	017x017	68	6,000	8,000	9,152	176	52
B04	027x027	108	17,000	23,000	25,800	300	86
B06	037x037	148	33,000	47,000	51,240	420	122
B08	047x047	188	55,000	78,000	85,952	544	158
B10	057x057	228	80,000	115,000	129,592	668	194
B12	067x067	268	106,000	154,000	181,240	788	230
B14	077x077	308	135,000	201,000	242,592	912	266
B16	087x087	348	165,000	239,000	311,664	1,032	302
B18	097x097	388	198,000	291,000	388,416	1,156	336
B20	107x107	428	233,000	333,000	476,160	1,280	372
B22	117x117	468	268,000	388,000	571,200	1,400	408
B24	127x127	508	304,000	439,000	676,656	1,524	444
B26	137x137	548	348,000	506,000	791,040	1,648	480
B28	147x147	588	383,000	547,000	912,288	1,768	516
B30	157x157	628	417,000	605,000	1,044,384	1,892	552
B32	167x167	668	448,000	636,000	1,179,032	2,012	586
B34	177x177	708	478,000	690,000	1,328,592	2,136	622
B36	187x187	748	520,000	743,000	1,487,080	2,260	658
B38	197x197	788	561,000	792,000	1,651,720	2,380	694
B40	207x207	828	603,000	840,000	1,827,920	2,504	730
B42	217x217	868	643,000	904,000	2,009,984	2,624	766

MSM98Q/99Q Family Listing

E/A		# of	Usable Gate				
Product Name	Base Array						
MSM9xQ	B9xQ	PAD	M98Q	M99Q	Raw Gate	Column	Row
B06	036x036	144			138,400		
B10	044x044	176	128,000	184,000	214,000	856	250
B11	048x048	192	149,000	216,000	257,560	940	274
B12	050x050	200	159,000	229,000	280,280	980	286
B13	052x052	208	170,000	244,000	305,152	1,024	298
B14	056x056	224	192,000	278,000	356,776	1,108	322
B15	060x060	240	213,000	308,000	411,048	1,188	346
B16	064x064	256	240,000	343,000	470,640	1,272	370
B17	068x068	272	268,000	381,000	536,976	1,356	396
B18	072x072	288	296,000	417,000	604,800	1,440	420
B19	076x076	304	324,000	460,000	676,656	1,524	444
B20	080x080	320	353,000	504,000	752,544	1,608	468
B21	084x084	336	382,000	539,000	830,496	1,688	492
B22	088x088	352	402,000	576,000	914,352	1,772	516
B23	092x092	368	430,000	611,000	1,002,240	1,856	540
B24	096x096	384	461,000	658,000	1,098,040	1,940	566
B25	100x100	400	477,000	680,000	1,194,160	2,024	590
B26	104x104	416	503,000	710,000	1,291,856	2,104	614

ARRAY ARCHITECTURE

The primary components of a 0.35μm MG73Q/74Q and MSM98Q/99Q circuit include:

- I/O base cells: 60-μm staggered I/O pitch (MG73Q/74Q) or 100-μm In-Line I/O pitch (MSM98Q/99Q)
- Configurable I/O pads for V_{DD}, V_{SS}, or I/O (optimized 3-V I/O and 3-V I/O that is 5-V tolerant)
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells containing N-channel and P-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility

Each array has 24 dedicated corner pads for power and ground use during wafer probing, with four pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and output drive transistors (V_{DDO} and V_{SSO}).

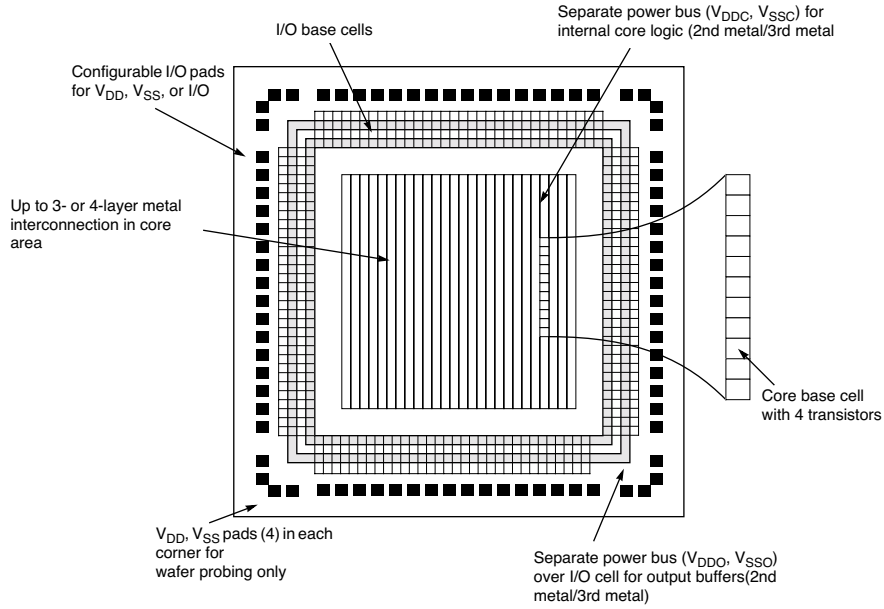


Figure 7. MSM98Q000 Array Architecture

CSA Layout Methodology

The procedure to design, place, and route a CSA follows.

1. Select suitable base array frame from the available predefined sizes. To select an array size:
    - Identify macrocell functions required and minimum array size to hold macrocell functions.
    - Add together all the area occupied by the required random logic and macrocells and select the optimum array.
2. Make a floor plan for the design's megacells.
    - Oki Design Center engineers verify the master slice and review simulation.
    - Oki Design Center or customer engineers floorplan the array using Oki's proprietary floorplanner, Cadence DP3, or Gambit GFP and customer performance specifications.
    - Using Oki CAD software, Design Center engineers remove the SOG transistors and replace them with diffused memory macrocells to the customer's specifications.

Figure 8 shows an array base after placement of the optimized memory macrocells.

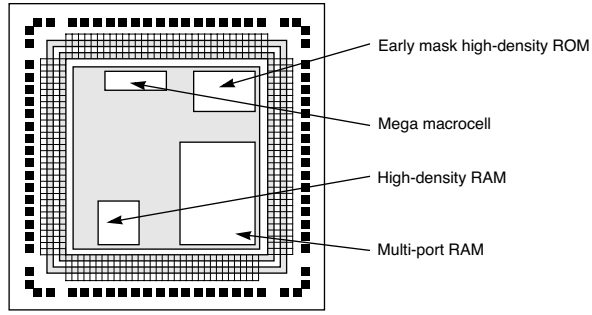


Figure 8. Optimized Memory Macrocell Floor Plan

3. Place and route logic into the array transistors.
    - Oki Design Center engineers use layout software and customer performance specifications to connect the random logic and optimized memory macrocells.

Figure 9 marks the area in which placement and routing is performed with cross hatching.

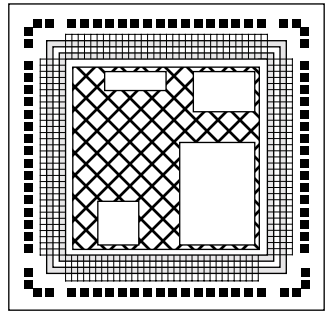


Figure 9. Random Logic Place and Route

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0 V, Tj = 25°C) [1]

Parameter [2]		Symbol	Conditions	Rated Value	Unit
Power supply voltage	Core (2.5 V)	V_{DDCORE}	-	-0.3 ~ +3.6	V
	I/O (3.3 V)	V_{DDIO}	-	-0.3 ~ +4.6	
Input voltage	(Normal Buffer)	V_I	-	-0.3 ~ V_{DDIO}+0.3	
	(5-V Tolerant Buffer)		V_{DDIO} = +0.3 ~ 3.6V	-0.3 ~ 6.0	
			V_{DDIO} < 3.0V	-0.3 ~ V_{DDIO}+0.3	
Output voltage	(Normal Buffer)	V_O	-	-0.3 ~ V_{DDIO}+0.3	
	(5-V Tolerant Buffer)		V_{DDIO} = +0.3 ~ 3.6V	-0.3 ~ 6.0	
			V_{DDIO}< 3.0V	-0.3 ~ V_{DDIO}+0.3	
Input current	(Normal Buffer)	I_I	-	-10 ~ + 10	mA
	(5-V Tolerant Buffer)		-	-9 ~ + 9	
Output current	1 mA buffer	I_O	-	-5 ~ + 5	
	2 mA buffer		-	-9 ~ +9	
	4 mA buffer		-	-9 ~ +9	
	6 mA buffer		-	-12 ~ + 12	
	8 mA buffer		-	-16 ~ + 16	
	12 mA buffer		-	-24 ~ + 24	
	24 mA buffer		-	-48 ~ + 48	
Storage temperature		Tj	-	-65 ~ +150	°C

1. [1] Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions in the other specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 5-V Tolerant IO is available on CSA product only

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter		Symbol	Rated Value			Unit
			Min	Typ	Max	
Power supply voltage	Core	V_{DD}core	+2.25	+2.5	+2.75	V
	I/O	V_{DD}io	+3.0	+3.3	+3.6	
Junction temperature		Tj	-40	-	+85	°C
Input rise time/fall time		tr, tf	-	2	20	ns

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V , Tj = - 40 to + 85°C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ [1]	Max	
High-level input voltage	V_{IH}	TTL normal input	2.0	-	VDD+0.3	V
		TTL 5-V tolerant input	2.0	-	5.5	
Low-level input voltage	V_{IL}	TTL normal input	-0.3	-	0.8	
		TTL 5-V tolerant input	-0.3	-	0.8	
TTL-level Schmitt Trigger threshold voltage (Normal buffer)	Vt+	TTL normal input	-	-	2.0	
	Vt-		0.7	-	-	
	ΔVt	Vt+ - Vt-	0.4	-	-	
TTL-level Schmitt Trigger threshold voltage (5-V tolerant buffer)	Vt+	TTL 5-V tolerant input	-	-	2.0	
	Vt-		0.7	-	-	
	ΔVt	Vt+ - Vt-	0.4	-	-	
High-level output voltage (Normal buffer)	V_{OH}	I_{OH}= -100 μA	V_{DD}-0.2	-	-	
		I_{OH}= -1,-2,-4,-6,-8,-12,-24 mA	2.4	-	-	
High-level output voltage (5-V tolerant buffer)		I_{OH}= -100 μA	V_{DD}-0.2	-	-	
		I_{OH}= -1,-2,-4,-6,-8,-12 mA	2.4	-	-	
Low-level output voltage (Normal buffer)	V_{OL}	IOL= 100 μA	-	-	0.2	
		I_{OL}= 1,2,4,6,8,12,24 mA	-	-	0.4	
Low-level output voltage (5-V tolerant buffer)		I_{OL}= 100 μA	-	-	0.2	
		I_{OL}= 1,2,4,6,8,12 mA	-	-	0.4	
High-level input current (Normal buffer)	I_{IH}	V_{IH}=VDDio	-	-	10	μA
		V_{IH}= V_{DDIO} (50kΩ pull down)	10	66	200	
High-level input current (5-V tolerant buffer)		V_{IH}= V_{DDIO}	-	-	10	
		V_{IH}= V_{DDIO} (50kΩ pull down)	10	66	200	
		V_{IH}= 5.5 V	-	-	10	
		V_{IH}= 5.5 V (3k/50kΩ pull up)	-	-	250	
		V_{IH}= 5.5 V (50kΩ pull down)	-	-	200	
Low-level input current (Normal buffer)	I_{IL}	V_{IL}= V_{SS}	-10	-	-	
		V_{IL}= V_{SS} (50kΩ pull up)	-200	-66	-10	
		V_{IL}= V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA
Low-level input current (5-V tolerant buffer)		V_{IL}= V_{SS}	-10	-	-	μA
		V_{IL}= V_{SS} (50kΩ pull up)	-200	-66	-10	
		V_{IL}= V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA
3-state output leakage current (Normal buffer)	I_{OZH}	V_{OH}= V_{DDIO}	-	-	10	μA
		V_{OH}= V_{DDIO} (50kΩ pull down)	10	66	200	
	I_{OZL}	V_{OL}= V_{SS}	-10	-	-	
		V_{OL}= V_{SS} (50kΩ pull up)	-200	-66	-10	
		V_{OL}= V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA
3-state output leakage current (5-V tolerant buffer)	I_{OZH}	V_{OH}= V_{DDIO}	-	-	10	μA
		V_{OH}= V_{DDIO} (50kΩ pull down)	10	66	200	
		V_{OH}= 5.5 V	-	-	10	
		V_{OH}= 5.5 V (3k/50kΩ pull up)	-	-	150	
		V_{OH}= 5.5 V (50kΩ pull down)	-	-	200	
	I_{OZL}	V_{OL}= V_{SS}	-10	-	-	
		V_{OL}= V_{SS} (50kΩ pull up)	-200	-66	-10	
		V_{OL}= V_{SS} (3kΩ pull up)	-3.3	-1.1	-0.3	mA

1. Typical condition in V_{DD}= 3.3 V and Tj= 25°C

MG73Q/74Q AC Characteristics (V_{DD} = 3.3 V, V_{SS} = 0 V , Tj = 25°C)

Parameter		Driving Type	Conditions [1] [2]	Rated Value [3]	Unit
Internal gate propagation delay	Inverter	1X	F/O=2 , L=0 mm	0.11	ns
		2X		0.091	
		4X		0.077	
	2-input NAND	1X		0.13	
		2X		0.11	
	Inverter	1X	F/O=2 standard wire length	0.23	
		2X		0.17	
		4X		0.12	
	2-input NAND	1X		0.28	
		2X		0.19	
Toggle frequency			F/O=1, L=0 mm	1040	MHz
Input buffer propagation delay	TTL level normal input buffer		F/O=2 , standard wire length	0.35	ns
	TTL level 5-V tolerant input buffer			0.56	
Output buffer propagation delay	Push-pull Normal output buffer	4 mA	CL=20 pF	1.79	
		8 mA	CL=50 pF	2.09	
		12 mA	CL=100 pF	2.66	
	3-state 5-V tolerant output buffer	4 mA	CL=20 pF	2.01	
Output buffer transition times [4]	Push-pull Normal output buffer	12 mA	CL=100 pF	4.08 (r) 3.13 (f)	
	3-state 5-V tolerant output buffer	4 mA	CL=20 pF	3.26 (r) 2.52 (f)	

1. Input transition time in 0.2 ns / 3.3 V
2. Typical condition in VDD= 3.3 V and Tj= 25°C.
3. Rated value is calculated as an average of the L-H and H-L delay times of each macro type on a typical process.
4. Output rising and falling times are both specified over a 10%-90% range.

MACRO LIBRARY

Oki Semiconductor supports a wide range of macrocells and macrofunctions, ranging from simple hard macrocells for basic Boolean operations to large, user-parameter configurable macrofunctions. The following figure illustrates the main classes of macrocells and macrofunctions available.

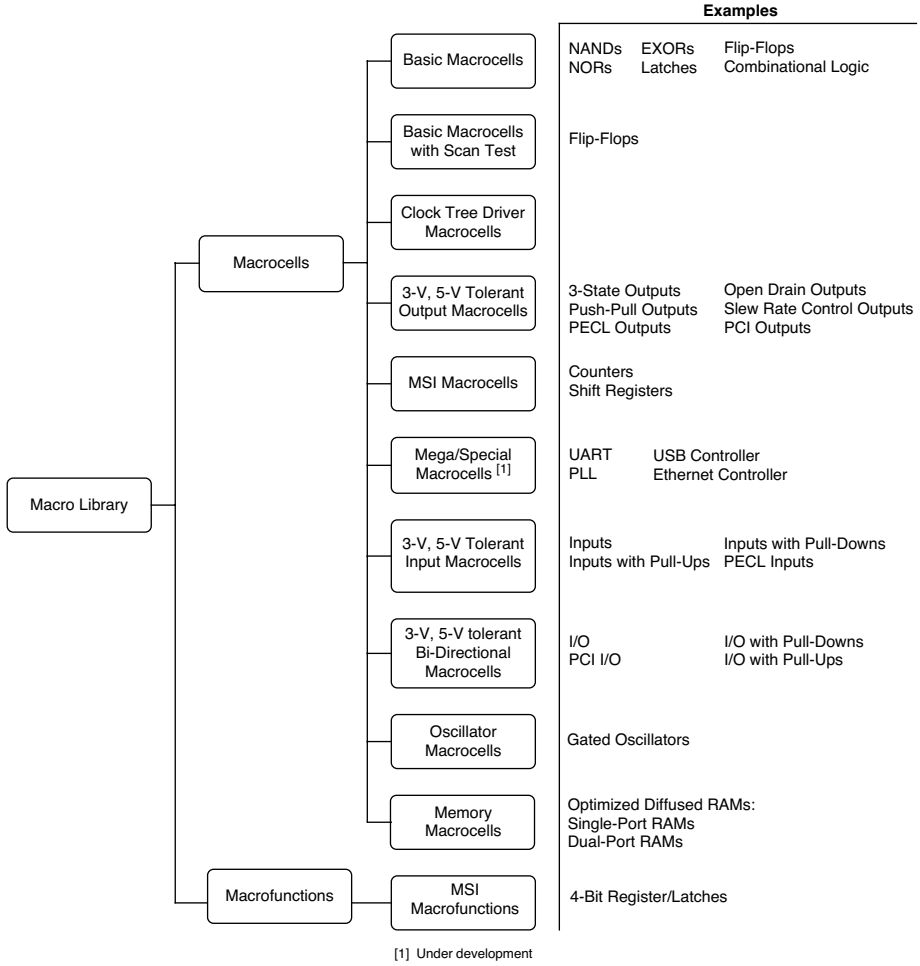


Figure 10. Oki Macrocell and Macrofunction Library

Macrocells for Driving Clock Trees

Oki offers clock-tree drivers that minimize clock skew. The advanced layout software uses dynamic driver placement and sub-trunk allocation to optimize the clock-tree implementation for a particular circuit. Features of the clock-tree driver-macrocells include:

- True RC back annotation of the clock network
- Automatic fan-out balancing
- Dynamic sub-trunk allocation
- Single clock tree driver logic symbol
- Automatic branch length minimization
- Dynamic driver placement
- Up to four clock trunks

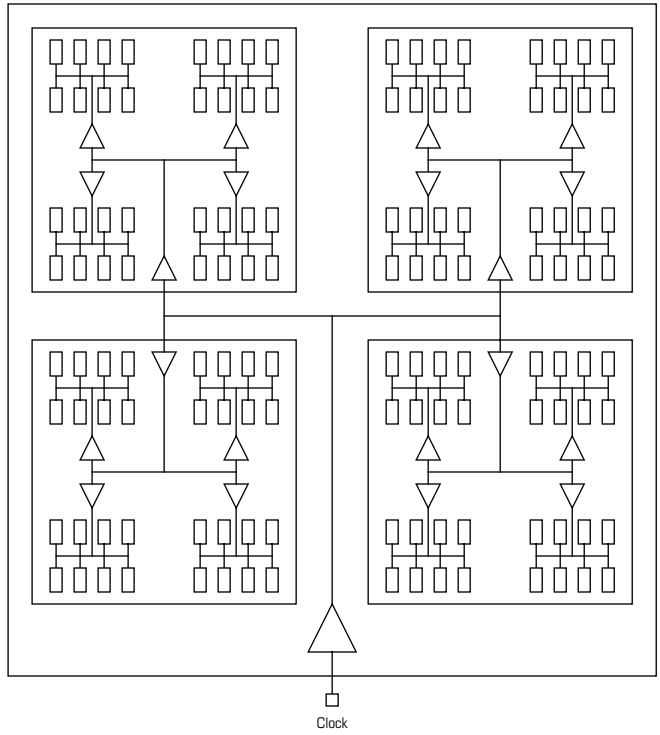


Figure 11. Clock Tree Structure

OKI ADVANCED DESIGN CENTER CAD TOOLS

Oki's advanced design center CAD tools include support for the following:

- Floorplanning for front-end simulation and back-end layout control
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- JTAG Boundary scan support
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements

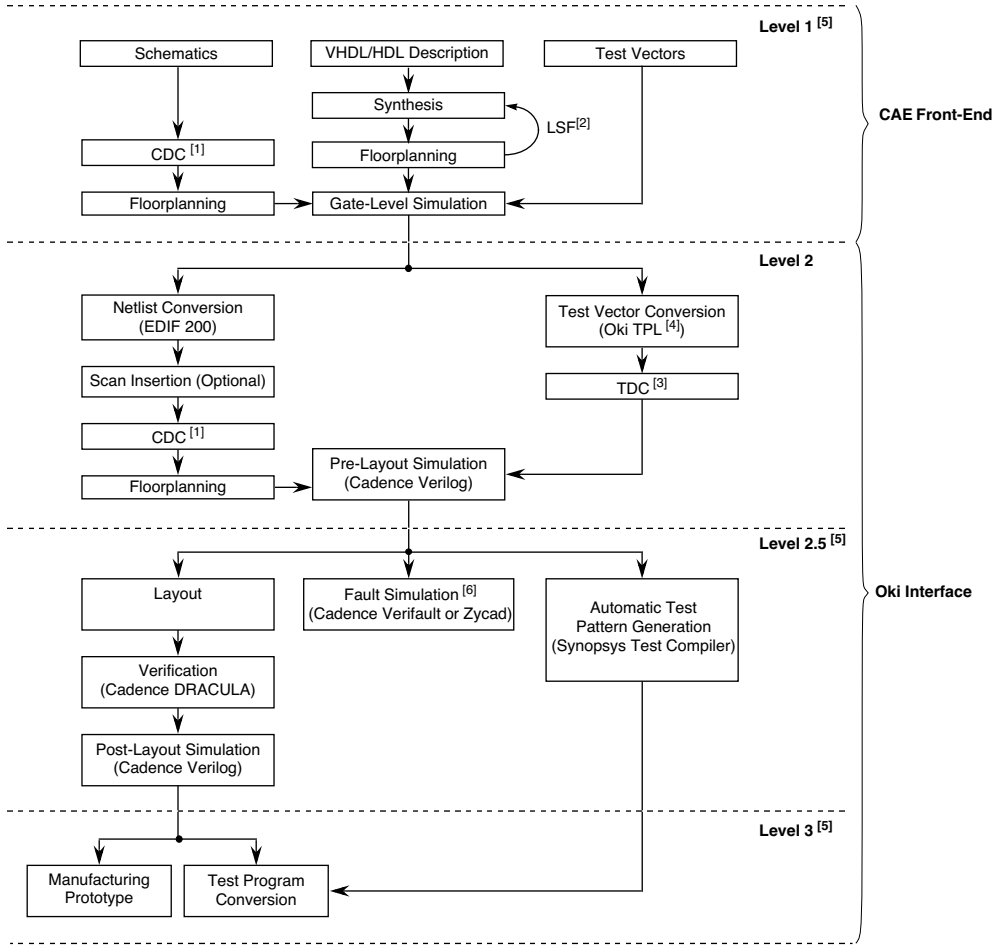
Design Kits

Vendor	Platform	Operating System [1]	Vendor Software/Revision [1]	Description
Cadence	Sun® [2]	Solaris	Ambit Buildgates NC-Verilog™ Verilog XL	Design Synthesis Design Simulation Design Simulation
Syntest	Sun® [2]	Solaris	Turbo Fault	Fault Simulation
Synopsys	Sun® [2]	Solaris	Design Compiler Ultra + Tetramax/ATPG Primetime DFT Compiler/Test Compiler RTL Analyzer VCS	Design synthesis Test Synthesis Static Timing Analysis (STA) Test synthesis RTL check Design Simulation
Model Technology Inc. (MTI)	Sun® [2] NT	Solaris WinNT4.0	MTI-VHDL MTI-Verilog	Design Simulation Design Simulation
Oki	Sun® [2]	Solaris	Floorplanner	Floor planning
Verplex	Sun® [2]	Solaris	Conformal	Formal Verification

1. Contact Oki Application Engineering for current software versions.
2. Sun or Sun-compatible.

Design Process

The following figure illustrates the overall IC design process, also indicating the three main interface points between external design houses and Oki ASIC Application Engineering.



[1] Oki's Circuit Data Check program (CDC) verifies logic design rules
[2] Oki's Link to Synthesis Floorplanning toolset (LSF) transfers post-floorplanning timing for resynthesis
[3] Oki's Test Data Check program (TDC) verifies test vector rules
[4] Oki's Test Pattern Language (TPL)
[5] Alternate Customer-Oki design interfaces available in addition to standard level 2
[6] Standard design process includes fault simulation

Figure 12. Oki's Design Process

Automatic Test Pattern Generation

Oki's 0.35-μm ASIC technologies support ATPG using full scan-path design techniques, including the following:

- Increases fault coverage ≥ 95%
- Uses Synopsys Test Compiler
- Automatically inserts scan structures
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports vector compaction

ATPG methodology is described in detail in Oki's *0.35µm Scan Path Application Note*.

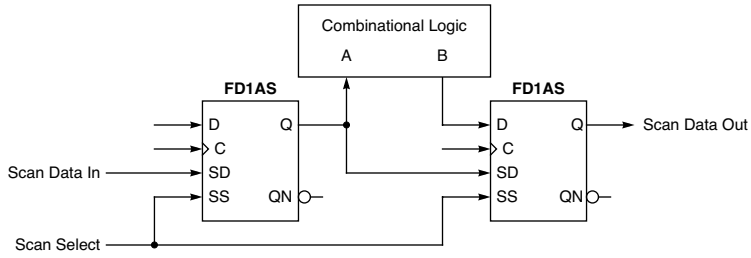


Figure 13. Full Scan Path Configuration

Floorplanning Design Flow

Oki offers three floorplanning tools for high-density ASIC design: Cadence DP3, Gambit GFP, Oki's floorplanner. The two main purposes for Oki's floorplanning tools are to:

- Ensure conformance of critical circuit performance specifications
- Shorten overall design TAT

In a traditional design approach with synthesis tools, timing violations after pre-layout simulation are fixed by manual editing of the netlist. This process is difficult and time consuming. Also, there is no physical cluster information provided in the synthesis tool, and so it is difficult to synthesize logic using predicted interconnection delay due to wire length. Synthesis tools may therefore create over-optimized results.

To minimize these problems, Synopsys proposed a methodology called, "Links to Layout (LTL)". Based on this methodology, Oki developed an interface between Oki's Floorplanner and the Synopsys environment, called Link Synopsys to Floorplanner (LSF). As not every Synopsys user has access to the Synopsys Floorplan Management tool, Oki had developed the LSF system to support both users who can access Synopsys Floorplan Management and users who do not have access to Synopsys Floorplan Management.

More information on OKI's floorplanning capabilities is available in Oki's Application Note, *Using Oki's Floorplanner: Standalone Operation and Links to Synopsys*.

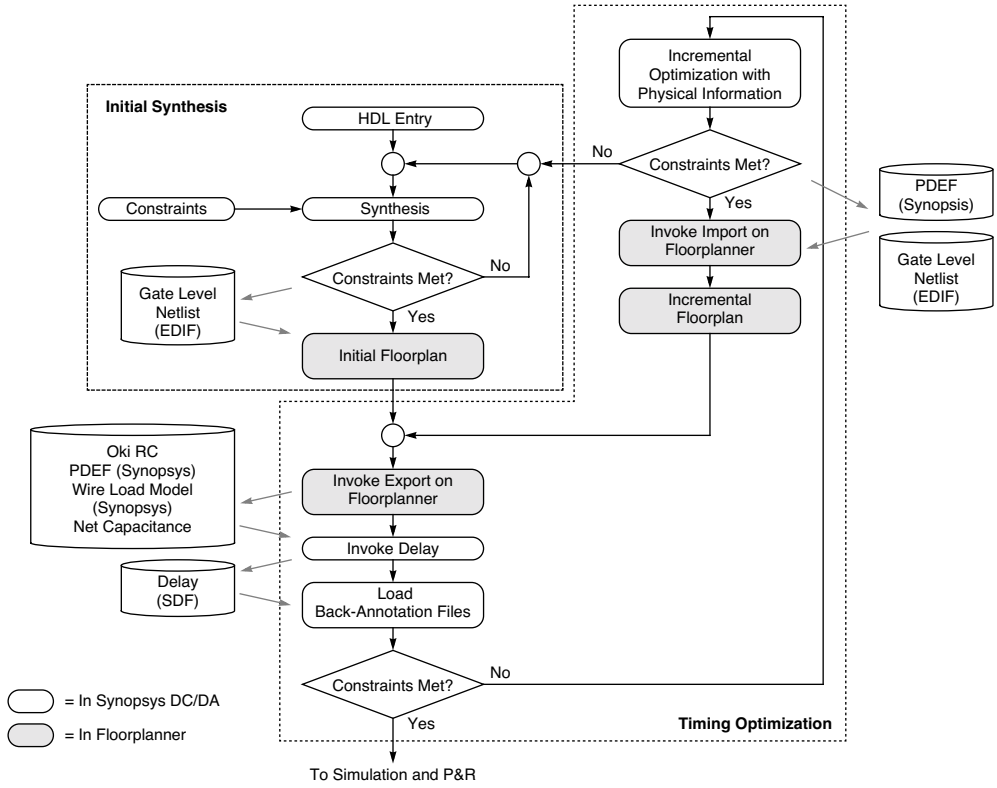


Figure 14. LSF System Design Flow

IEEE JTAG Boundary Scan Support

Boundary scan offers efficient board-level and chip-level testing capabilities. Benefits resulting from incorporating boundary-scan logic into a design include:

- Improved chip-level and board-level testing and failure diagnostic capabilities
- Support for testing of components with limited probe access
- Easy-to-maintain testability and system self-test capability with on-board software
- Capability to fully isolate and test components on the scan path
- Built-in test logic that can be activated and monitored
- An optional Boundary Scan Identification (ID) Register

Oki's boundary scan methodology meets the JTAG Boundary Scan standard, IEEE 1149.1-1990. Oki supports boundary scan on both Sea of Gates (SOG) and Customer Structured Array (CSA) ASIC technologies. Either the customer or Oki can perform boundary-scan insertion. More information is available in Oki's *JTAG Boundary Scan Application Note.* (Contact the Oki Application Engineering Department for interface options.)

PACKAGE OPTIONS

MG73Q/74Q TQFP and LQFP and QFP Package Menu

		TQFP		LQFP			QFP
Base Array	I/O Pads [1]	100	128	144	176	208	208
MG7XQB02	68	—	—	—	—	—	—
MG7XQB04	108	●	—	—	—	—	—
MG7XQB06	148	●	●	❍	—	—	—
MG7XQB08	188	●	●	●	❍	—	—
MG7XQB10	228	●	●	●	●	●	●
MG7XQB12	268	●	●	●	●	●	●
MG7XQB14	308	●	●	●	●	●	●
MG7XQB16	348	●	●	●	●	●	●
MG7XQB18	388	●	●	●	●	❍	❍
MG7XQB20	428	—	—	—	—	—	—
MG7XQB22	468	—	—	—	—	—	—
MG7XQB24	508	—	—	—	—	—	—
MG7XQB26	548	—	—	—	—	—	—
MG7XQB28	588	—	—	—	—	—	—
MG7XQB30	628	—	—	—	—	—	—
MG7XQB32	668	—	—	—	—	—	—
MG7XQB34	708	—	—	—	—	—	—
MG7XQB36	748	—	—	—	—	—	—
MG7XQB38	788	—	—	—	—	—	—
MG7XQB40	828	—	—	—	—	—	—
MG7XQB42	868	—	—	—	—	—	—
Body Size (mm)		14 x 14	14 x 14	20 x 20	24 x 24	28 x 28	28 x 28
Lead Pitch (mm)		0.5	0.4	0.5	0.5	0.5	0.5

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

MG73Q/74Q BGA

Base Array	I/O Pads [1]	BGA 256	352	420	560	660
MG7XQB02	68	—	—	—	—	—
MG7XQB04	108	—	—	—	—	—
MG7XQB06	148	—	—	—	—	—
MG7XQB08	188	—	—	—	—	—
MG7XQB10	228	❍	—	—	—	—
MG7XQB12	268	●	—	—	—	—
MG7XQB14	308	●	—	—	—	—
MG7XQB16	348	●	—	—	—	—
MG7XQB18	388	●	●	●	—	—
MG7XQB20	428	●	●	●	—	—
MG7XQB22	468	●	●	●	—	—
MG7XQB24	508	●	●	●	—	—
MG7XQB26	548	●	●	●	—	—
MG7XQB28	588	●	●	●	❍	—
MG7XQB30	628	●	●	●	❍	—
MG7XQB32	668	—	●	●	❍	❍
MG7XQB34	708	—	●	●	—	❍
MG7XQB36	748	—	●	●	—	❍
MG7XQB38	788	—	●	—	—	—
MG7XQB40	828	—	—	—	—	—
MG7XQB42	868	—	—	—	—	—
Body Size (mm)		27 x 27	35 x 35	35 x 35	35 x 35	40 x 40
Lead Pitch (mm)		1.27	1.27	1.27	1.00	1.00
Number of Signal Pins		231	304	352	400	496
Number of Fixed V_{DD} Pins		12	16	32	80	82
Number of Fixed Gnd Pins		13	32	36	80	82
Number of Substrate Layers		2	2	2		

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

MSM98Q/99Q TQFP and LQFP Package Menu

Base Array	I/O Pads [1]	TQFP			LQFP		
		64	80	100	144	176	208
98Q/99Q044X044	176	●	●	●	●	●	—
98Q/99Q048X048	192	●	●	●	●	●	—
98Q/99Q050X050	200	●	●	●	●	●	—
98Q/99Q052X052	208	●	●	●	●	●	●
98Q/99Q056X056	224	—	●	●	●	●	●
98Q/99Q060X060	240	—	●	●	●	●	●
98Q/99Q064X064	256	—	●	●	●	●	●
98Q/99Q068X068	272	—	●	●	●	●	●
98Q/99Q072X072	288	—	●	●	●	●	●
98Q/99Q076X076	304	—	—	●	●	●	●
98Q/99Q080X080	320	—	—	●	●	●	●
98Q/99Q084X084	336	—	—	●	●	●	●
98Q/99Q088X088	352	—	—	—	●	●	●
98Q/99Q092X092	368	—	—	—	●	●	●
98Q/99Q096X096	384	—	—	—	●	●	●
98Q/99Q100X100	400	—	—	—	●	●	●
98Q/99Q104X104	416	—	—	—	●	●	●
98Q/99Q108X108	432	—	—	—	●	●	●
Body Size (mm)		10 x 10	12 x 12	14 x 14	20 x 20	24 x 24	28 x 28
Lead Pitch (mm)		0.5	0.5	0.5	0.5	0.5	0.5

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

MSM98Q/99Q PQFP Package Menu

Base Array	I/O Pads [1]	PQFP			
		128	160	208	240
98Q/99Q044X044	176	●	●	—	—
98Q/99Q048X048	192	●	●	—	—
98Q/99Q050X050	200	●	●	—	—
98Q/99Q052X052	208	●	●	—	—
98Q/99Q056X056	224	●	●	●	—
98Q/99Q060X060	240	●	●	●	●
98Q/99Q064X064	256	●	●	●	●
98Q/99Q068X068	272	●	●	●	❍
98Q/99Q072X072	288	●	❍	●	❍
98Q/99Q076X076	304	●	❍	●	❍
98Q/99Q080X080	320	●	●	●	●
98Q/99Q084X084	336	●	●	●	●
98Q/99Q088X088	352	●	●	●	●
98Q/99Q092X092	368	●	●	●	●
98Q/99Q096X096	384	●	●	●	●
98Q/99Q100X100	400	●	●	●	●
98Q/99Q104X104	416	●	●	❍	●
98Q/99Q108X108	432	●	●	●	●
Body Size (mm)		28 x 28	28 x 28	28 x 28	32 x 32
Lead Pitch (mm)		0.80	0.65	0.5	0.5

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

MSM98Q/99Q BGA Package Menu

Base Array	I/O Pads [1]	BGA 256	BGA 352	BGA 420	BGA 560
98Q/99Q036X036	144	—	—	—	—
98Q/99Q038X038	152	—	—	—	—
98Q/99Q040X040	160	—	—	—	—
98Q/99Q042X042	168	●	—	—	—
98Q/99Q044X044	176	●	—	—	—
98Q/99Q048X048	192	●	—	—	—
98Q/99Q050X050	200	●	—	—	—
98Q/99Q052X052	208	●	—	—	—
98Q/99Q056X056	224	●	—	—	—
98Q/99Q060X060	240	●	—	—	—
98Q/99Q064X064	256	●	—	—	—
98Q/99Q068X068	272	●	●	—	—
98Q/99Q072X072	288	●	●	—	—
98Q/99Q076X076	304	●	●	—	—
98Q/99Q080X080	320	●	●	●	—
98Q/99Q084X084	336	●	●	●	—
98Q/99Q088X088	352	●	●	●	—
98Q/99Q092X092	368	●	●	●	—
98Q/99Q096X096	384	●	●	●	—
98Q/99Q100X100	400	—	●	●	—
98Q/99Q104X104	416	—	●	●	—
98Q/99Q108X108	432	—	●	●	—
Body Size (mm)		27 x 27	35 x 35	35 x 35	35 x 35
Lead Pitch (mm)		1.27	1.27	1.27	1.00
Number of Signal Pins		231	304	352	400
Number of Fixed V_{DD} Pins		12	16	32	80
Number of Fixed Gnd Pins		13	32	36	80
Number of Substrate Layers		2	2	2	2

1. I/O Pads can be used for input, output, bi-directional, power, or ground.

● = Available now; ❍ = In development

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