

SpeedREACH™ AR8201 — ADSL AFE for CPE with +5 V Line Driver+DCXO

OVERVIEW

Asymmetric digital subscriber line (ADSL) technology provides a viable solution to meet the emerging need for high-bandwidth communications to the home while utilizing existing twisted-pair copper infrastructure. LSI Logic's SpeedREACH analog front ends (AFEs) meet this need by boosting the performance of customer premise and central office equipment, creating new market opportunities for OEMs. The SpeedREACH AR8201 is a highly integrated AFE designed to perform all of the analog functions of the receive (RX) and transmit (TX) paths for ADSL customer premise modems — full-rate and G.lite. The AR8201 is also the industry's first AFE to offer the integrated combination of a +5 V line driver and digitally controlled crystal oscillator (DCXO), eliminating the need for a +12 V supply required when using an external line driver.

The RX portion of the chip consists of a low-noise programmable gain amplifier (PGA) having a gain range of -6 dB to +38 dB in 0.25 dB steps, an anti-aliasing filter, and a 16-bit analog-to-digital converter (ADC). The TX portion consists of a 16-bit digital-to-analog converter (DAC), a transmit low-pass filter, and a programmable attenuation amplifier (PAA) with an attenuation of 0 dB to -24 dB in 1 dB steps. To simplify the overall system design, DAC droop compensation is handled internally, removing this burden from the back-end signal processing.

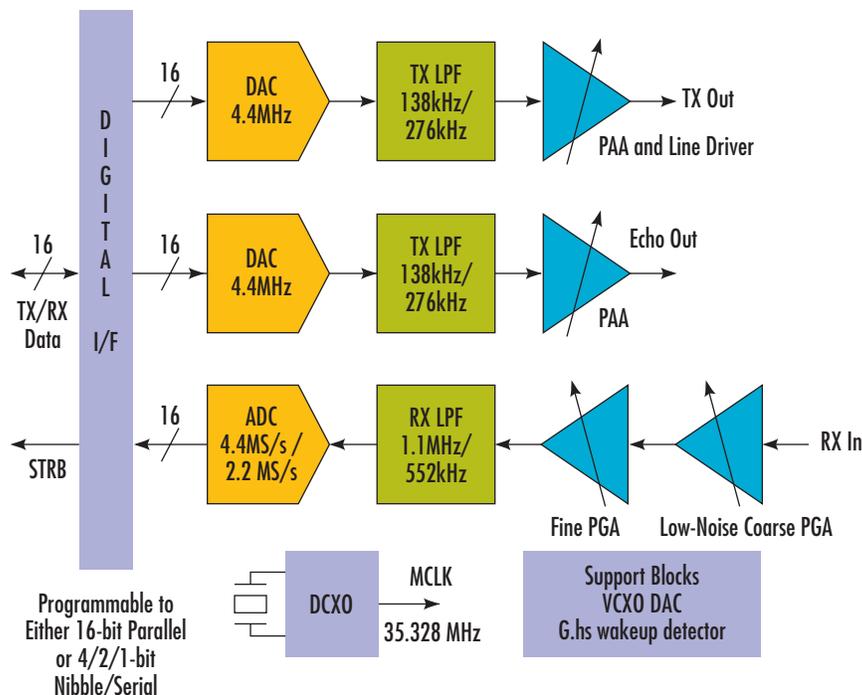


Figure 1. Block diagram of the SpeedREACH AR8201.

FEATURES

- ADSL CPE AFE with full RX and TX analog signal path
- Compatible with both ITU G.992.1 and (G.dmt) and G.992.2 (G.lite) standards
- Integrated line driver capable of driving +13 dBm onto the line using a 4.25:1 transformer
- Low-power wakeup detector for G.hs (G.994.1) and ANSI T1E1.413 Issue 7 wakeup protocol
- Programmable interface for RX/TX digital data
- Integrated DCXO
- Power: 1W (driving +13 dBm DMT signal onto the line)
- Line driver total harmonic distortion for 138 kHz sinewave at 7.4 V peak-to-peak differential with either (a) 11 Ω resistance load or (b) 5.5 Ω resistance and 4.25:1 transformer: -85 dB
- 14-bit linear 4.4 MS/s ADCs and 14-bit linear 4.4 MS/s DACs
- 4th-order low-pass filters for RX/TX paths with a $\pm 5\%$ cutoff frequency accuracy
- TX channel: support for 138 kHz and 276 kHz (for ADSL over ISDN)
- RX channel: support for both 552 kHz (G.lite) and 1.104 MHz (G.dmt)
- Entire RX channel linearity: 80 dB MTPR and TX channel linearity: 80 dB MTPR
- RX input-referred noise at peak gain: -160 dBm/Hz at 300 kHz

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This device includes an integrated TX line driver and, with an appropriate 4.25:1 step up transformer, can drive +13 dBm onto the twisted pair line, as required for the upstream channel in both G.992.1 and G.992.2. Total harmonic distortion of the entire TX channel including the driver is better than -80 dB at full power (+13 dBm on the line).

Apart from the primary signal paths, the chip also contains support circuitry for other functions required in an ADSL modem. To assist in timing recovery, a 12-bit DAC is present to drive an off-chip voltage controlled crystal oscillator (VCXO). An on-chip DCXO is also present, allowing the modem manufacturer to replace an expensive external VCXO module with a low-cost crystal. An all-analog "wakeup" detector is present when the ADSL line is unused, all of the back-end digital and analog circuitry in the modem can thus be powered down, facilitating significant power savings.

A 4-wire serial port provides a simple DSP interface. The serial port is used to modify internal register values, which in turn control attenuation/gain settings, filter bandwidths and the power down of individual blocks. The chip is powered off a +5 V supply while all digital I/Os run off a +3.3 V supply. The AR8201 is available in a 100-pin LQFP plastic package. The operating temperature range is between -40°C and +85°C.

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