# TECHNICAL MANUAL

# LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller

**June 2003**

*Version 2.1*

LSI LOGIC®

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# Preface

This book is the primary reference and technical manual for the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller. It contains a functional description for the LSI53C1030 and the physical and electrical specifications for the LSI53C1030.

## Audience

This document assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the LSI53C1030 for use in a system
- Engineers who are designing the LSI53C1030 into a system

## Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, provides an overview of the LSI53C1030 features and capabilities.
- Chapter 2, **Functional Description**, provides a detailed functional description of the LSI53C1030 operation. This chapter describes how the LSI53C1030 implements the PCI, PCI-X, and SCSI bus specifications.
- Chapter 3, **Signal Description**, provides a detailed signal description for the LSI53C1030.
- Chapter 4, **PCI Host Register Description**, provides a bit level description of the host register set of the LSI53C1030.

- Chapter 5, **Specifications**, provides the electrical and physical specifications for the device.
- Appendix A, **Register Summary**, provides a register map for the LSI53C1030.

## Related Publications

**LSI Logic Documents**
*Fusion-MPT Device Management User's Guide, Version 2.0, DB15-000186-02*

**LSI Logic World Wide Web Home Page**
www.lsilogic.com

**ANSI**
11 West 42nd Street
New York, NY 10036
(212) 642-4900

**Global Engineering Documents**
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740

**ENDL Publications**
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

**Prentice Hall**
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

**SCSI Electronic Bulletin Board**
(719) 533-7950

**PCI Special Interest Group**
2575 N. E. Katherine
Hillsboro, OR 97214
(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

## Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end with a "/."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

## Revision History

| Revision | Date | Remarks |
|---|---|---|
| Version 2.1 | 6/2003 | Updated the external memory timing diagrams.<br>Updated the default Subsystem ID value.<br>Updated the ZCR behavior description.<br>Updated the Multi-ICE test interface description. |
| Version 2.0 | 4/2002 | Added register summary appendix.<br>Updated the electrical characteristics.<br>Updated the Index. |
| Preliminary Version 1.0 | 12/2001 | Updated the description of Fusion-MPT architecture in Chapter 1.<br>Updated External Memory Interface descriptions in Chapter 2.<br>Added Test Interface description to Chapter 2.<br>Added Zero Channel RAID interface description to Chapters 2 and 3.<br>Updated the MAD Power-On Sense pin description in Chapter 3.<br>Updated signal descriptions and lists to include the ZCR-related pins.<br>Updated electrical and environmental characteristics in Chapter 5.<br>Removed figures relating to SE SCSI electrical and timing characteristics from Chapter 5.<br>Removed SCSI timing information from Chapter 5 and referred readers to the SCSI specification.<br>Removed PSBRAM interface and all related information. |
| Advance Version 0.1 | 2/2001 | Initial release of document. |

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# Chapter 1
# Introduction

This chapter provides a general overview of the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller. This chapter contains the following sections:



## 1.1 General Description

The LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller brings Ultra320 SCSI performance to host adapter, workstation, and server designs, making it easy to add a high-performance SCSI bus to any PCI or PCI-X system. The LSI53C1030 supports both the *PCI Local Bus Specification, Revision 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*.[1]

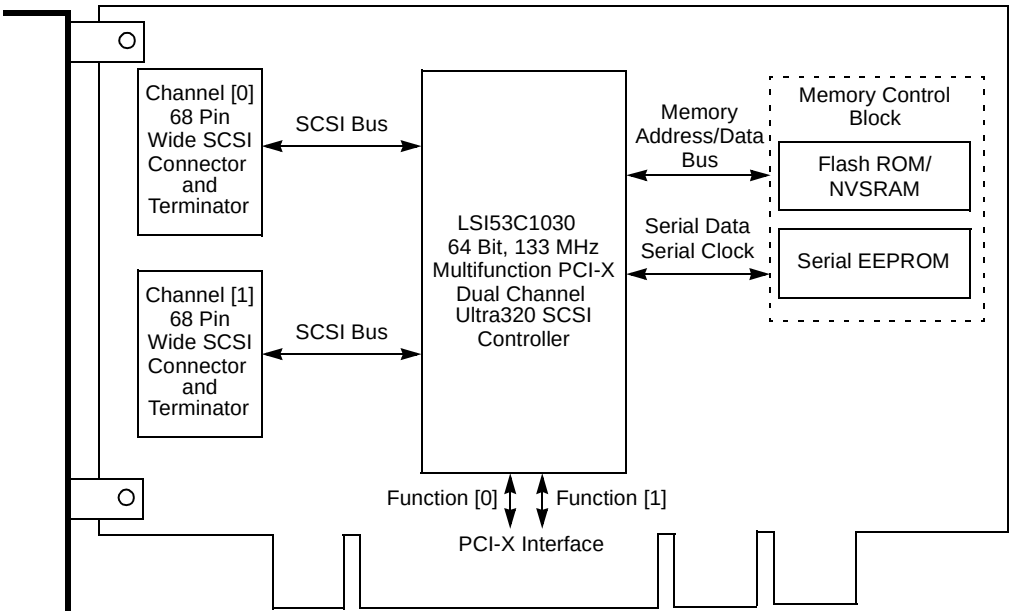
1. In some instances, this manual references PCI-X explicitly. References to the PCI bus may be inclusive of both the PCI specification and PCI-X addendum, or they may refer only to the PCI bus depending on the operating mode of the device.

The LSI53C1030 is pin compatible with the LSI53C1010R PCI to Dual Channel Ultra160 SCSI Multifunction Controller to provide an easy and safe migration path to Ultra320 SCSI. The LSI53C1030 supports up to a 64-bit, 133 MHz PCI-X bus. The Ultra320 SCSI features for the LSI53C1030 include: double transition (DT) clocking, packetized protocol, paced transfers, quick arbitrate and select (QAS), skew compensation, intersymbol interference (ISI) compensation, cyclic redundancy check (CRC), and domain validation technology. These features comply with the American National Standard Institute (ANSI) T10 SCSI Parallel Interface-4 (SPI-4) draft specification.

DT clocking enables the LSI53C1030 to achieve data transfer rates of up to 320 megabytes per second (Mbytes/s) on each SCSI channel, for a total bandwidth of 640 Mbytes/s on both SCSI channels. Packetized protocol increases data transfer capabilities with SCSI information units. QAS minimizes SCSI bus latency by allowing the bus to directly enter the arbitration/selection bus phase after a SCSI disconnect and skip the bus free phase. Skew compensation permits the LSI53C1030 to adjust for cable and bus skew on a per-device basis. Paced transfers enable high speed data transfers during DT data phases by using the REQ/ACK transition as a free running data clock. Precompensation enables the LSI53C1030 to adjust the signal drive strength to compensate for the charge present on the cable. CRC improves the SCSI data transmission integrity through enhanced detection of communication errors. SureLINK™ Domain Validation detects the SCSI bus configuration and adjusts the SCSI transfer rate to optimize bus interoperability and SCSI data transfer rates. SureLINK Domain Validation provides three levels of domain validation, assuring robust system operation.

The LSI53C1030 supports a local memory bus, which supports a standard serial EEPROM and allows local storage of the BIOS in Flash ROM memory. The LSI53C1030 supports programming of local Flash ROM memory for BIOS updates. Figure 1.1 shows a typical LSI53C1030 board application connected to external ROM memory.

**Figure 1.1 Typical LSI53C1030 Board Application**

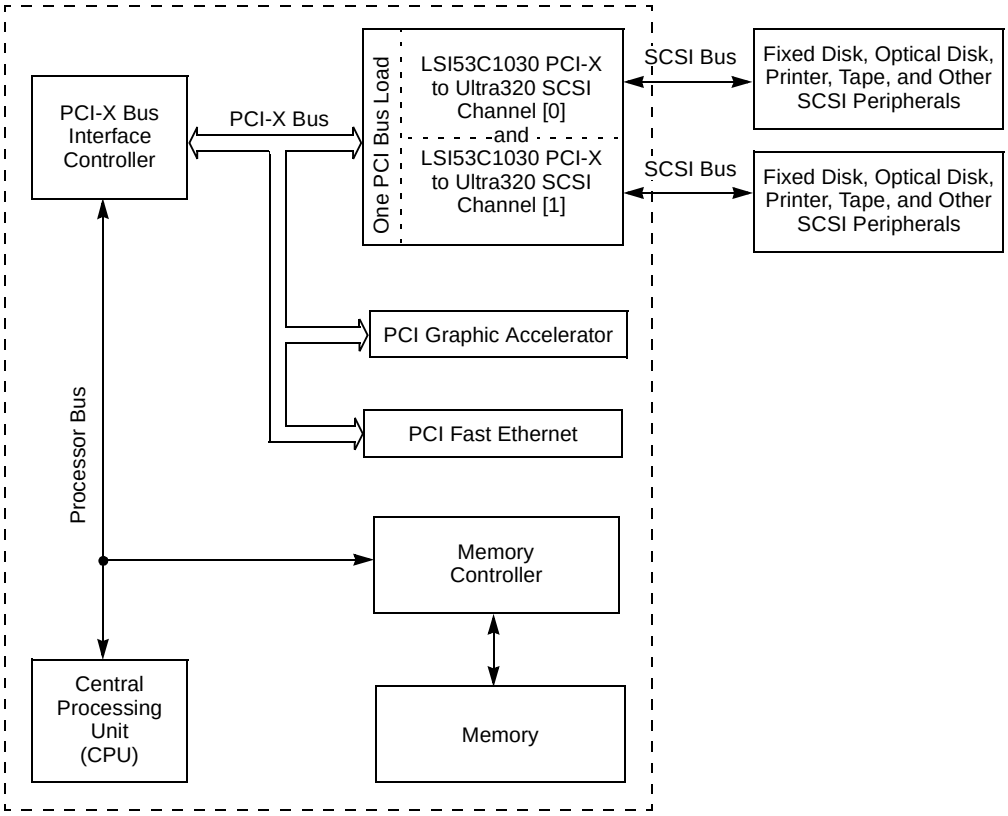



The LSI53C1030 integrates two high-performance SCSI Ultra320 cores and a 64-bit, 133 MHz PCI-X bus master DMA core. The LSI53C1030 employs three ARM966E-S processors to meet the data transfer flexibility requirements of the Ultra320 SCSI, PCI, and PCI-X specifications. Separate ARM® processors support each SCSI channel and the PCI/PCI-X interface.

These processors implement the LSI Logic Fusion-MPT™ architecture, a multithreaded I/O algorithm that supports data transfers between the host system and SCSI devices with minimal host processor intervention. Fusion-MPT technology provides an efficient architecture that solves the protocol overhead problems of previous intelligent and nonintelligent adapter designs.

LVDlink™ technology is the LSI Logic implementation of Low Voltage Differential (LVD) SCSI. LVDlink transceivers allow the LSI53C1030 to perform either Single-Ended (SE) or LVD transfers. Figure 1.2 illustrates a typical LSI53C1030 system application.

**Figure 1.2 Typical LSI53C1030 System Application**




The LSI53C1030 supports the LSI Logic Integrated Mirroring™ (IM) technology, which provides physical mirroring of the boot volume through LSI53C1030 firmware. This feature provides extra reliability for the system's boot volume without burdening the host CPU. Keeping a second disk as a mirror requires the LSI Logic Fusion-MPT firmware, which performs writes to both the boot drive and the mirrored drive. The runtime mirroring of the boot drive is transparent to the BIOS, drivers, and operating system.

The IM firmware requires a configuration mechanism, which enables configuration of the mirroring attributes during initial setup or reconfiguration after hardware failures or changes in the system environment. Use the LSI Logic BIOS Configuration Utility or the IM DOS Configuration Utility to configure the IM firmware attributes. Using the LSI Logic BIOS and drivers adds support of physical device recognition for

the purpose of Domain Validation and Ultra320 SCSI expander configuration. Host based status software monitors the state of the mirrored drives and reports error conditions as they arise.

## 1.2 Benefits of the Fusion-MPT Architecture

The Fusion-MPT architecture provides an open architecture that is ideal for SCSI, Fibre Channel, and other emerging interfaces. The I/O interface is interchangable at the system and application level; embedded software uses the same device interface for SCSI and Fibre Channel implementations just as application software uses the same storage management interfaces for SCSI and Fibre Channel implementations. LSI Logic provides Fusion-MPT device drivers that are binary compatible between Fibre Channel and Ultra320 SCSI interfaces.

The Fusion-MPT architecture improves overall system performance by requiring only a thin device driver, which off loads the intensive work of managing SCSI I/Os from the system processor to the LSI53C1030. Developed from the proven LSI Logic SDMS™ solution, the Fusion-MPT architecture delivers unmatched performance of up to 100,000 Ultra320 SCSI I/Os per second with minimal system overhead or device maintenance. The use of thin, easy to develop, common OS device drivers accelerates time to market by reducing device driver development and certification times.

The Fusion-MPT architecture provides an *interrupt coalescing* feature. Interrupt coalescing allows an I/O controller to send multiple reply messages in a single interrupt to the host processor. Sending multiple reply messages per interrupt reduces context switching of the host processor and maximizes the host processor efficiency, which results in a significant improvement of system performance. To use the interrupt coalescing feature, the host processor must be able to accept and manage multiple replies per interrupt.

The Fusion-MPT architecture also provides built-in device driver stability since the device driver need not change for each revision of the LSI53C1030 silicon or firmware. This architecture is a reliable, constant interface between the host device driver and the LSI53C1030. Changes within the LSI53C1030 are transparent to the host device driver, operating system, and user. The Fusion-MPT architecture also saves the

user significant development and maintenance effort since it is not necessary to alter or redevelop the device driver when a revision of the LSI53C1030 device or firmware occurs.

## 1.3 Benefits of PCI-X

PCI-X doubles the maximum clock frequency of the conventional PCI bus. The *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*, defines enhancements to the proven *PCI Local Bus Specification, Revision 2.2*. PCI-X provides more efficient data transfers by enabling registered inputs and outputs, improves buffer management by including transaction information with each data transfer, and reduces bus overhead by restricting the use of wait states and disconnects. PCI-X also reduces host processor overhead by providing a wide range of error recovery implementations.

The LSI53C1030 supports up to a 133 MHz, 64-bit PCI-X bus and is backward compatible with previous versions of the PCI/PCI-X specification. The LSI53C1030 is a true multifunction PCI-X device and presents a single electrical load to the PCI bus. The LSI53C1030 uses a single REQ/-GNT/ pair to arbitrate for PCI bus mastership. Separate interrupt signals for PCI Function [0] and PCI Function [1] allow independent control of the two PCI functions.

Per the PCI-X addendum, the LSI53C1030 includes transaction information with all PCI-X transactions to enable more efficient buffer management schemes. Each PCI-X transaction contains a transaction sequence identifier (Tag), the identity of the initiator, and the number of bytes in the sequence. The LSI53C1030 clocks PCI-X data directly into and out of registers, which creates a more efficient data path. The LSI53C1030 increases bus efficiency since it does not insert wait states after the initial data phase when acting as a PCI-X target and never inserts wait states when acting as a PCI-X initiator.

## 1.4 Benefits of Ultra320 SCSI

Ultra320 SCSI is an extension of the SPI-4 draft specification that allows faster synchronous SCSI data transfer rates than Ultra160 SCSI. When enabled, Ultra320 SCSI performs 160 megatransfers per second

resulting in approximately double the synchronous data transfer rates of Ultra160 SCSI. The LSI53C1030 performs 16-bit, Ultra320 SCSI synchronous data transfers as fast as 320 Mbytes/s on each SCSI channel. This advantage is most noticeable in heavily loaded systems or large block size applications, such as video on-demand and image processing.

Ultra320 SCSI doubles both the data and clock frequencies from Ultra160 SCSI. Due to the increased data and clock speeds, Ultra320 SCSI introduces skew compensation and intersymbol interference (ISI) compensation. These new features simplify system design by resolving timing issues at the chip level. Skew compensation adjusts for timing differences between data and clock signals caused by cabling, board traces, etc. ISI compensation enhances the first pulse after a change in state to ensure data integrity.

Ultra320 SCSI includes CRC, which offers higher levels of data reliability by ensuring complete integrity of transferred data. CRC is a 32-bit scheme, referred to as CRC-32. CRC guarantees detection of all single or double bit errors, as well as any combination of bit errors within a single 32-bit range.

## 1.5 Benefits of SureLINK (Ultra320 SCSI Domain Validation)

SureLINK Domain Validation software ensures robust SCSI interconnect management and low risk Ultra320 SCSI implementations by extending the domain validation guidelines documented in the SPI-4 specifications. Domain validation verifies that the system is capable of transferring data at Ultra320 SCSI speeds, allowing the LSI53C1030 to renegotiate to a lower data transfer speed and bus width if necessary. SureLINK Domain Validation is the software control for the domain validation manageability enhancements in the LSI53C1030. SureLINK Domain Validation software provides domain validation management at boot time as well as during system operation.

SureLINK Domain Validation ensures robust system operation by providing 3 levels of integrity checking on a per-device basis: Basic (Level 1) with inquiry command, Enhanced (Level 2) with read/write buffer and Margined (Level 3) with margining of drive strength and slew rates.

## 1.6 Benefits of LVDlink Technology

The LSI53C1030 supports Low Voltage Differential (LVD) through LVDlink technology. This signalling technology increases the reliability of SCSI data transfers over longer distances than are supported by SE (Single Ended) SCSI. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. To allow the use of the LSI53C1030 in both legacy and Ultra320 SCSI applications, this device features universal LVDlink transceivers that support LVD SCSI and SE SCSI.

## 1.7 Benefits of TolerANT® Technology

The LSI53C1030 features TolerANT technology, which provides active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven high rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps ensure correct clocking of data. TolerANT input signal filtering is a built-in feature of the LSI53C1030 and all LSI Logic Fast SCSI, Ultra SCSI, Ultra2 SCSI, Ultra160 SCSI, and Ultra320 SCSI devices.

TolerANT technology increases noise immunity, balances duty cycles, and improves SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power-up or power-down, which protects other devices on the bus from data corruption. When used with the LVDlink transceivers, TolerANT technology provides excellent signal quality and data reliability in real world cabling environments. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

## 1.8 Summary of LSI53C1030 Features

This section provides a summary of the LSI53C1030 features and benefits. It contains information on SCSI Performance, PCI Performance, Integration, Flexibility, Reliability, and Testability.

### 1.8.1 SCSI Performance

The LSI53C1030 contains the following SCSI performance features:

- Supports Ultra320 SCSI
  - Paced transfers using a free running clock
  - 320 Mbyte/s data transfer rate on each SCSI channel
  - Mandatory packetized protocol
  - Quick arbitrate and select (QAS)
  - Skew compensation with bus training
  - Transmitter precompensation to overcome ISI effects for SCSI data signals
  - Retained training information (RTI)
- Offers a performance optimized architecture
  - Three ARM966E-S processors provide high performance with low latency
  - Two independent Ultra320 SCSI channels
  - Designed for optimal packetized performance
- Uses proven integrated LVDlink transceivers for direct attach to either LVD or SE SCSI buses with precision-controlled slew rates
- Supports expander communication protocol (ECP)
- Uses the Fusion-MPT (Message Passing Technology) drivers to provide support for Windows, Linux, Solaris, SCO Openserver, UnixWare, OpenUnix 8, and NetWare operating systems

### 1.8.2 PCI Performance

The LSI53C1030 supports these PCI features:

- Has a 133 MHz, 64-bit PCI/PCI-X interface that:
  - Operates at 33 MHz or 66 MHz PCI
  - Operates at up to 133 MHz PCI-X
  - Supports 32-bit or 64-bit data
  - Supports 32-bit or 64-bit addressing through Dual Address Cycles (DAC)
  - Provides a theoretical 1066 Mbytes/s zero wait state transfer rate
  - Complies with the *PCI Local Bus Specification, Revision 2.2*
  - Complies with the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*
  - Complies with *PCI Power Management Interface Specification, Revision 1.1*
  - Complies with *PC2001 System Design Guide*
- Offers unmatched performance through the Fusion-MPT architecture
- Provides high throughput and low CPU utilization to off load the host processor
- Presents a single electrical load to the PCI Bus (True PCI Multifunction Device)
- Uses SCSI Interrupt Steering Logic (SISL) to provide alternate interrupt routing for RAID applications
- Reduces Interrupt Service Routine (ISR) overhead with interrupt coalescing
- Supports 32-bit or 64-bit data bursts with variable burst lengths
- Supports the PCI Cache Line Size register
- Supports the PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands
- Supports the PCI-X Memory Read Dword, Split Completion, Memory Read Block, and Memory Write Block commands
- Supports up to 8 PCI-X outstanding split transactions
- Supports Message Signalled Interrupts (MSI)

### 1.8.3 Integration

These features make the LSI53C1030 easy to integrate:

- Is backward compatible with previous revisions of the PCI and SCSI specifications
- Is pin compatible with the LSI53C1010R PCI to Dual Channel Ultra160 SCSI Multifunction Controller
- Provides a low-risk migration path to Ultra320 SCSI from the LSI53C1010R
- Is a dual channel Ultra320 SCSI to PCI/PCI-X multifunction controller
- Supports a 32-bit or 64-bit PCI/PCI-X DMA bus master
- Reduces time to market with the Fusion-MPT architecture
  - Single driver binary for SCSI and Fibre Channel products
  - Thin, easy to develop drivers
  - Reduced integration and certification effort
- Provides integrated LVDlink transceivers

### 1.8.4 Flexibility

These features increase the flexibility of the LSI53C1030:

- Universal LVD transceivers are backward compatible with SE devices
- Provides a flexible programming interface to tune I/O performance or to adapt to unique SCSI devices
- Supports MSI or pin-based (INTx/ or ALT_INTx/) interrupt signalling
- Can respond with multiple SCSI IDs
- Is compatible with 3.3 V and 5.0 V PCI signalling
  - Drives and receives 3.3 V PCI signals
  - Receives 5.0 V PCI if the PCI5VBIAS pin connects to 5 V, but does not drive 5.0 V signals on the PCI bus

### 1.8.5 Reliability

These features enhance the reliability of the LSI53C1030:

- Supports intersymbol interference (ISI) compensation
- Provides 2 kV ESD protection on SCSI signals
- Provides latch-up protection greater than 150 mA
- Provides voltage feed-through protection
- Supports LSI Logic Integrated Mirroring (IM) technology to provide physical mirroring of the boot volume
- Has a high proportion of power and ground pins
- Provides power and ground isolation of I/O pads and internal chip logic
- Supports CRC checking and generation in Double Transition (DT) phases
- Provides comprehensive SureLINK Domain Validation technology:
  - Basic (Level 1) with inquiry command
  - Enhanced (Level 2) with read/write buffer
  - Margined (Level 3) with margining of drive strength and slew rates
- Supports TolerANT technology, which provides:
  - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved SCSI transfer rates
  - Input signal filtering on SCSI receivers for improved data integrity, even in noisy cabling environments

### 1.8.6 Testability

These features enhance the testability of the LSI53C1030:

- Allows all SCSI signals to be accessed through programmed I/O
- Supports JTAG boundary scan
- Provides ARM Multi-ICE® for debugging purposes

# Chapter 2
# Functional Description

This chapter provides a subsytem level overview of the LSI53C1030, a discussion of the Fusion-MPT architecture, and a functional description of the LSI53C1030 interfaces. This chapter contains the following sections:



The LSI53C1030 is a high performance, intelligent PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller. The LSI53C1030 supports the *PCI Local Bus Specification, Revision 2.2*, the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*, and the proposed *SCSI Parallel Interface-4* (SPI-4) draft standard.

The LSI53C1030 employs the LSI Logic Fusion-MPT architecture to ensure robust system performance, to support binary compatibility of host software between the LSI Logic SCSI and Fibre Channel products, and to significantly reduce software development time. Refer to the *Fusion-MPT Device Management User’s Guide* for more information on the Fusion-MPT architecture.

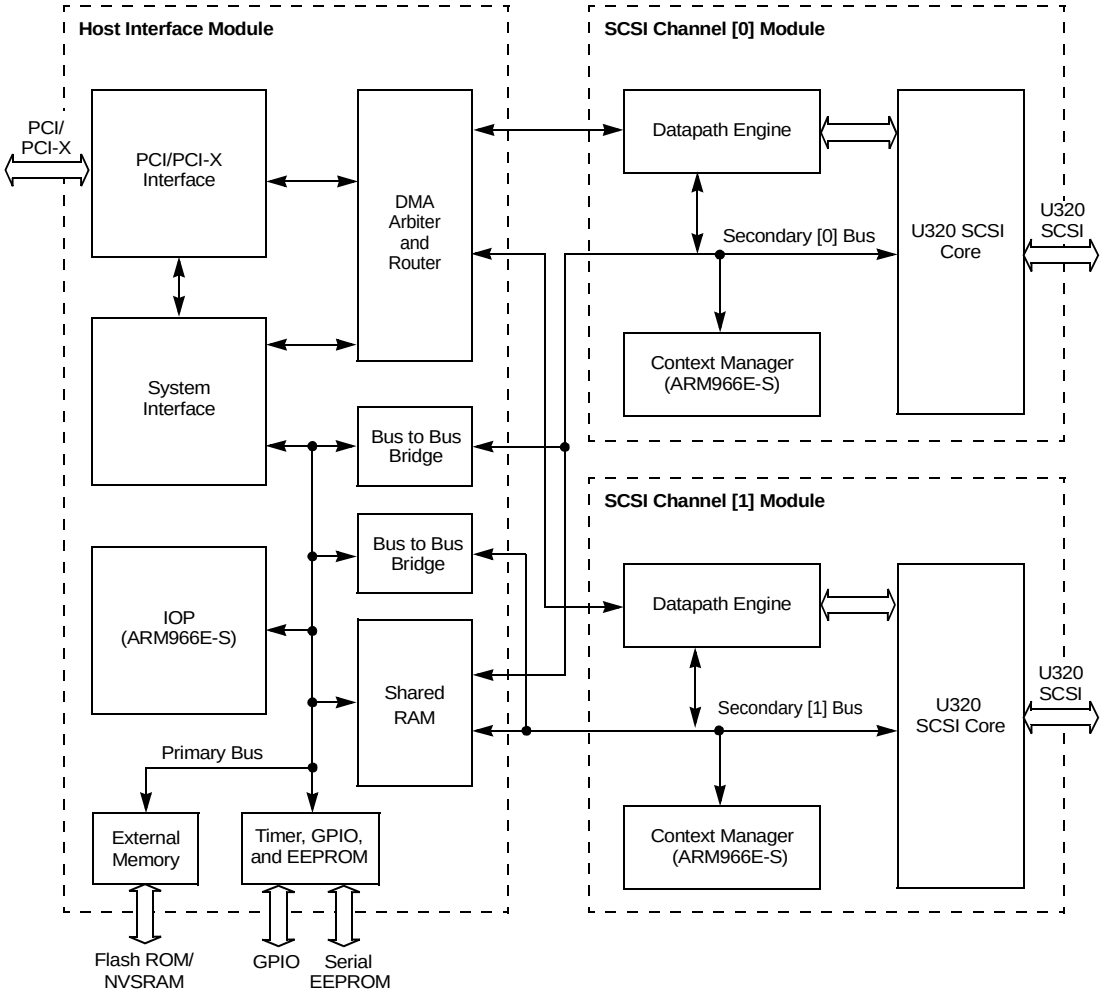
## 2.1 Block Diagram Description

The LSI53C1030 consists of three major modules: a host interface module and two independent Ultra320 SCSI channel modules. The modules consist of the following components:

- Host Interface Module
  - Up to a 64-bit, 133 MHz PCI/PCI-X Interface
  - System Interface
  - I/O Processor (IOP)
  - DMA Arbiter and Router
  - Shared RAM
  - External Memory Interface
    - ◊ Flash ROM Memory Controller
    - ◊ NVSRAM
  - Timer and Configuration Control
    - ◊ Device Configuration Controller
    - ◊ Serial EEPROM Interface Controller
    - ◊ GPIO Interface
    - ◊ Chip Timer
- Two independent Ultra320 SCSI Channel Modules
  - Datapath Engine
  - Context Manager
  - Ultra320 SCSI Core

Figure 2.1 illustrates the relationship between these modules.

**Figure 2.1 LSI53C1030 Block Diagram**




## 2.1.1 Host Interface Module Description

The host interface module provides an interface between the host driver and the two SCSI channels. The host interface module controls system DMA transfers and the host side of the LSI Logic Fusion-MPT architecture. It also supports the external memory, serial EEPROM, and General Purpose I/O (GPIO) interfaces. This section provides a detailed explanation of the host interface submodules.

#### 2.1.1.1 PCI Interface

The LSI53C1030 provides a PCI-X interface that supports up to a 64-bit, 133 MHz PCI-X bus. The interface is compatible with all previous implementations of the PCI specification. For more information on the PCI interface, refer to Section 2.3, “PCI Functional Description.”

#### 2.1.1.2 System Interface

The system interface efficiently passes messages between the LSI53C1030 and other I/O agents using a high performance, packetized, mailbox architecture. The system interface coalesces PCI interrupts to minimize traffic on the PCI bus and maximize system performance.

All host accesses to the IOP, external memory, and timer and configuration subsystems pass through the system interface and use the primary bus. The host system initiates data transactions on the primary bus with the system interface registers. PCI Memory Space [0] and the PCI I/O Base Address registers identify the location of the system interface register set. Chapter 4, "PCI Host Register Description", provides a bit level description of the system interface register set.

#### 2.1.1.3 I/O Processor (IOP)

The LSI53C1030 I/O processor (IOP) is a 32-bit ARM966E-S RISC processor. The IOP controls the system interface and uses the LSI Logic Fusion-MPT architecture to manage the host side of non-DMA accesses to the Ultra320 SCSI bus. The context manager uses the Fusion-MPT architecture to control the SCSI side of data transfers. The IOP and Context Manager completely manage all SCSI I/Os without host intervention. Refer to Section 2.2, “Fusion-MPT Architecture Overview,” for more information on the Fusion-MPT architecture

#### 2.1.1.4 DMA Arbiter and Router

The descriptor based DMA Arbiter and Router subsystem manages the transfer of memory blocks between local memory and the host system. The DMA channel includes PCI bus master interface logic, the internal bus interface logic, and a 256-byte system DMA FIFO.

#### 2.1.1.5 Shared RAM

The host interface module physically contains the 96 Kbyte shared RAM. However, both the host interface module and the SCSI channel modules access the shared RAM. The shared RAM holds a portion of the IOP and context manager firmware, as well as the request message queue and reply message queue. All non-DMA data transfers that use the request and reply message queues pass through the shared RAM.

#### 2.1.1.6 External Memory Controller

The external memory control subsystem provides a direct interface between the primary bus and the external memory subsystem. MAD[7:0] and MADP[0] comprise the external memory bus. The LSI53C1030 supports the Flash ROM and NVSRAM interfaces through the external memory controller. The Flash ROM is optional if the LSI53C1030 is not the boot device and a suitable driver exists to initialize the device. The LSI53C1030 uses the NVSRAM for IM technology. For a detailed description of this block refer to Section 2.5, “External Memory Interface.”

During power up or reset the LSI53C1030 uses the MAD[15:0] and MADP[1:0] signals as Power-On Sense pins, which configure the LSI53C1030 through their pull-up or pull-down settings. Refer to Section 3.10, “Power-On Sense Pins Description,” for a description of the Power-On Sense pin configuration options.

#### 2.1.1.7 Timer, GPIO, and Configuration

This subsystem provides a free running timer to allow event time stamping and also controls the general purpose I/O (GPIO), LED, and serial EEPROM interfaces. The LSI53C1030 uses the free running timer to aid in tracking and managing SCSI I/Os. The LSI53C1030 generates the free running timer’s microsecond time base by dividing the SCSI reference clock by 40.

The LSI53C1030 provides eight GPIO pins (GPIO[7:0]). These pins are under the control of the LSI53C1030 and default to the input mode upon PCI reset. The LSI53C1030 also provides three LED pins: A_LED/, B_LED/, and HB_LED/. Either firmware or hardware control A_LED/ and B_LED/. The LSI53C1030 firmware controls HB_LED/ (heartbeat LED), which indicates that the IOP is operational.

A 2-wire serial interface provides a connection to a nonvolatile external serial EEPROM. The serial EEPROM stores PCI configuration parameters for the LSI53C1030. Refer to Section 2.6, “Serial EEPROM Interface,” for more information concerning the serial EEPROM.

### 2.1.2 SCSI Channel Module Description

The LSI53C1030 provides two independent Ultra320 SCSI bus channels. Separate Ultra320 SCSI cores, datapath engines, and context managers support each SCSI channel. Refer to Section 2.4, “Ultra320 SCSI Functional Description,” for an operational description of the LSI53C1030 SCSI bus channels.

#### 2.1.2.1 Ultra320 SCSI Cores

The Ultra320 SCSI cores control their individual SCSI bus interface.

#### 2.1.2.2 Datapath Engines

The datapath engines manage the SCSI side of DMA transactions between their individual SCSI bus and the host system.

#### 2.1.2.3 Context Managers

The context managers are ARM966E-S processors. Each context manager controls the SCSI channel side of the LSI53C1030 Fusion-MPT architecture for their individual SCSI bus. The context managers control the outbound queues, target mode I/O mapping, disconnect and reselect sequences, scatter/gather lists, and status reports.

## 2.2 Fusion-MPT Architecture Overview

The Fusion-MPT architecture provides two I/O methods for the host system to communicate with the IOP: the system interface doorbell and the message queues.

The system interface doorbell is a simple message passing mechanism that allows the PCI host system and IOP to exchange single 32-bit Dword messages. When the host system writes to the doorbell, the LSI53C1030 hardware generates a maskable interrupt to the IOP, which can then read the doorbell value and take the appropriate action. When

the IOP writes a value to the doorbell, the LSI53C1030 hardware generates a maskable interrupt to the host system. The host system can then read the doorbell value and take the appropriate action.

There are two 32-bit message queues: the request message queue and the reply message queue. The host uses the request queue to request an action by the LSI53C1030, and the LSI53C1030 uses the reply queue to return status information to the host. The request message queue consists of only the request post FIFO. The reply message queue consists of both the reply post FIFO and the reply free FIFO. The shared RAM contains the message queues.

Communication using the message queues occurs through request messages and reply messages. Request message frame descriptors are pointers to the request message frames and are passed through the request post FIFO. The request message frame data structure is up to 128 bytes in length and includes a message header and a payload. The header uniquely identifies the message. The payload contains information that is specific to the request. Reply message frame descriptors have one of two formats and are passed through the reply post FIFO. When indicating the successful completion of a SCSI I/O, the IOP writes the reply message frame descriptor using the Context Reply format, which is a message context. If a SCSI I/O does not complete successfully, the IOP uses the Address Reply format. In this case, the IOP pops a reply message frame from the reply free FIFO, generates a reply message describing the error, writes the reply message to system memory, and writes the address of the reply message frame to the reply post FIFO. The host can then read the reply message and take the appropriate action.

The doorbell mechanism provides both a high-priority communication path that interrupts the host system device driver and an alternative communication path to the message queues. Since data transport through the system doorbell occurs a single Dword at a time, use the LSI53C1030 message queues for normal operation and data transport.

## 2.3 PCI Functional Description

The host PCI interface complies with the *PCI Local Bus Specification, Revision 2.2,* and the *PCI-X Addendum to the PCI Local Bus*

*Specification, Revision 1.0a*. The LSI53C1030 supports up to a 133 MHz, 64-bit PCI-X bus. The LSI53C1030 provides support for 64-bit addressing with Dual Address Cycle (DAC).

The LSI53C1030 is a true multifunction PCI-X device and presents a single electrical load to the PCI bus. The LSI53C1030 uses a single REQ/-GNT/ pair to arbitrate for PCI bus mastership. Separate interrupt signals for PCI Function [0] and PCI Function [1] allow independent control of the two PCI functions.

## 2.3.1 PCI Addressing

The three physical address spaces the PCI specification defines are:

- PCI Configuration Space
- PCI I/O Space for operating registers
- PCI Memory Space for operating registers

The following sections describe the PCI address spaces.

### 2.3.1.1 PCI Configuration Space

The LSI53C1030 defines an independent set of PCI Configuration Space registers for each PCI function. Each configuration space is a contiguous 256 x 8-bit set of addresses. The system BIOS initializes the configuration registers using PCI configuration cycles. The LSI53C1030 decodes C_BE[3:0]/ to determine if a PCI cycle intends to access the configuration register space. The IDSEL signal behaves as a chip select signal that enables access to the configuration register space only. The LSI53C1030 ignores configuration read/write cycles when IDSEL is not asserted.

Since the LSI53C1030 is a multifunction PCI device, bits AD[10:8] decode either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1030 does not respond to any other encodings of AD[10:8]. Bits AD[7:2] select one of the sixty-four Dword registers in the device's PCI Configuration Space. Bits AD[1:0] determine if the configuration command is a Type 0 Configuration Command (AD[1:0] = 0b00) or a Type 1 Configuration Command (AD[1:0] = 0b01). Since the LSI53C1030 is not a PCI Bridge device, all PCI Configuration Commands designated

for the LSI53C1030 must be Type 0. C_BE[3:0]/ address the individual bytes within each Dword and determine the type of access to perform.

#### 2.3.1.2 PCI I/O Space

The PCI specification defines I/O Space as a contiguous 32-bit I/O address that all system resources share, including the LSI53C1030. The I/O Base Address register determines the 256-byte PCI I/O area that the PCI device occupies.

#### 2.3.1.3 PCI Memory Space

The LSI53C1030 contains two PCI memory spaces: PCI Memory Space [0] and PCI Memory Space [1]. PCI Memory Space [0] supports normal memory accesses, while PCI Memory Space [1] supports diagnostic memory accesses. The LSI53C1030 requires 64 Kbytes of memory space.

The PCI specification defines memory space as a contiguous 64-bit memory address that all system resources share. The Memory [0] Low and Memory [0] High registers determine which 64 Kbyte memory area PCI Memory Space [0] occupies. The Memory [1] Low and Memory [1] High registers determine which 64 Kbyte memory area PCI Memory Space [1] occupies.

### 2.3.2 PCI Commands and Functions

Bus commands indicate to the target the type of transaction the master is requesting. The master encodes the bus commands on the C_BE[3:0]/ lines during the address phase. The PCI bus command encodings appear in Table 2.1.

**Table 2.1 PCI/PCI-X Bus Commands and Encodings[1]**

| C_BE[3:0]/ | PCI Command | PCI-X Command | Supports as Master | Supports as Slave |
|---|---|---|---|---|
| 0b0000 | Interrupt Acknowledge | Interrupt Acknowledge | No | No |
| 0b0001 | Special Cycle | Special Cycle | No | No |
| 0b0010 | I/O Read | I/O Read | Yes | Yes |

**Table 2.1 PCI/PCI-X Bus Commands and Encodings[1] (Cont.)**

| C_BE[3:0]/ | PCI Command | PCI-X Command | Supports as Master | Supports as Slave |
|---|---|---|---|---|
| 0b0011 | I/O Write | I/O Write | Yes | Yes |
| 0b0100 | Reserved | Reserved | N/A | N/A |
| 0b0101 | Reserved | Reserved | N/A | N/A |
| 0b0110 | Memory Read | Memory Read Dword | Yes | Yes |
| 0b0111 | Memory Write | Memory Write | Yes | Yes |
| 0b1000 | Reserved | Alias to Memory Read Block | PCI: N/A PCI-X: No | PCI: N/A PCI-X: Yes |
| 0b1001 | Reserved | Alias to Memory Write Block | PCI: N/A PCI-X: No | PCI: N/A PCI-X: Yes |
| 0b1010 | Configuration Read | Configuration Read | No | Yes |
| 0b1011 | Configuration Write | Configuration Write | No | Yes |
| 0b1100 | Memory Read Multiple | Split Completion | Yes | Yes[2] |
| 0b1101 | Dual Address Cycle | Dual Address Cycle | Yes | Yes |
| 0b1110 | Memory Read Line | Memory Read Block | Yes | Yes[2] |
| 0b1111 | Memory Write and Invalidate | Memory Write Block | Yes | Yes[3] |

1. The LSI53C1030 ignores reserved commands as a slave and never generates them as a master.
2. When acting as a slave in the PCI mode, the LSI53C1030 supports this command as the PCI Memory Read command.
3. When acting as a slave in the PCI mode, the LSI53C1030 supports this command as the PCI Memory Write command.

The following sections describe how the LSI53C1030 implements these commands.

### 2.3.2.1 Interrupt Acknowledge Command

The LSI53C1030 ignores this command as a slave and never generates it as a master.

#### 2.3.2.2 Special Cycle Command

The LSI53C1030 ignores this command as a slave and never generates it as a master.

#### 2.3.2.3 I/O Read Command

The I/O Read command reads data from an agent mapped in the I/O address space. When decoding I/O commands, the LSI53C1030 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

#### 2.3.2.4 I/O Write Command

The I/O Write command writes data to an agent mapped in the I/O address space. When decoding I/O commands, the LSI53C1030 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

#### 2.3.2.5 Memory Read Command

The LSI53C1030 uses the Memory Read command to read data from an agent mapped in the memory address space. The target can perform an anticipatory read if such a read produces no side effects. The LSI53C1030 supports this command when operating in the PCI bus mode.

#### 2.3.2.6 Memory Read Dword Command

The Memory Read Dword command reads up to a single Dword of data from an agent mapped in the memory address space and can only be initiated as a 32-bit transaction. The target can perform an anticipatory read if such a read produces no side effects. The LSI53C1030 supports this command when operating in the PCI-X bus mode.

#### 2.3.2.7 Memory Write Command

The Memory Write command writes data to an agent mapped in the memory address space. The target assumes responsibility for data

coherency when it returns “ready.” The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

#### 2.3.2.8 Alias to Memory Read Block Command

This command is reserved for future implementations of the PCI specification. The LSI53C1030 never generates this command as a master. When a slave, the LSI53C1030 supports this command using the Memory Read Block command.

#### 2.3.2.9 Alias to Memory Write Block Command

This command is reserved for future implementations of the PCI specification. The LSI53C1030 never generates this command as a master. When a slave, the LSI53C1030 supports this command using the Memory Write Block command.

#### 2.3.2.10 Configuration Read Command

The Configuration Read command reads the configuration space of a device. The LSI53C1030 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSI53C1030 by asserting its IDSEL signal when AD[1:0] equal 0b00. During the address phase of a configuration cycle, AD[7:2] address one of the 64 Dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each Dword register and determine the type of access to perform. Bits AD[10:8] address either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1030 treats AD[63:11] as logical don’t cares.

#### 2.3.2.11 Configuration Write Command

The Configuration Write command writes the configuration space of a device. The LSI53C1030 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSI53C1030 by asserting its IDSEL signal when bits AD[1:0] equal 0b00. During the address phase of a configuration cycle, bits AD[7:2] address one of the 64 Dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each Dword register and determine the type of access to perform. Bits AD[10:8] decode either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI

Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1030 treats AD[63:11] as logical don't cares.

#### 2.3.2.12 Memory Read Multiple Command

The Memory Read Multiple command is identical to the Memory Read command, except it additionally indicates that the master intends to fetch multiple cache lines before disconnecting. The LSI53C1030 supports PCI Memory Read Multiple functionality when operating in the PCI mode and determines when to issue a Memory Read Multiple command instead of a Memory Read command.

**Burst Size Selection –** The Read Multiple command reads multiple cache lines of data during a single bus ownership. The number of cache lines the LSI53C1030 reads is a multiple of the cache line size, which Revision 2.2 of the PCI specification provides. The LSI53C1030 selects the largest multiple of the cache line size based on the amount of data to transfer.

#### 2.3.2.13 Split Completion Command

Split transactions in PCI-X replace the delayed transactions in conventional PCI. The LSI53C1030 supports up to eight outstanding split transactions when operating in the PCI-X mode. A split transaction consists of at least two separate bus transactions: a split request, which the requester initiates, and one or more split completion commands, which the completer initiates. Revision 1.0a of the PCI-X addendum permits split transaction completion for the Memory Read Block, Alias to Memory Read Block, Memory Read Dword, Interrupt Acknowledge, I/O Read, I/O Write, Configuration Read, and Configuration Write commands. When operating in the PCI-X mode, the LSI53C1030 supports the Split Completion command for all of these commands except the Interrupt Acknowledge command, which the LSI53C1030 neither responds to nor generates.

#### 2.3.2.14 Dual Address Cycles (DAC) Command

The LSI53C1030 performs Dual Address Cycles (DAC), per the *PCI Local Bus Specification, Revision 2.2*. The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

### 2.3.2.15 Memory Read Line Command

This command is identical to the Memory Read command except it additionally indicates that the master intends to fetch a complete cache line. The LSI53C1030 supports this command when operating in the PCI mode.

### 2.3.2.16 Memory Read Block Command

The LSI53C1030 uses this command to read from memory. The LSI53C1030 supports this command when operating in the PCI-X mode.

### 2.3.2.17 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except it additionally guarantees a minimum transfer of one complete cache line. The master uses this command when it intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI Cache Line Size register. The LSI53C1030 determines when to issue a Write and Invalidate command instead of a Memory Write command and supports this command when operating in the PCI bus mode.

**Alignment –** The LSI53C1030 uses the calculated line size value to determine if the current address aligns to the cache line size. If the address does not align, the LSI53C1030 bursts data using a noncache command. If the starting address aligns, the LSI53C1030 issues a Memory Write and Invalidate command using the cache line size as the burst size.

**Multiple Cache Line Transfers –** The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The LSI53C1030 issues a burst transfer as soon as it reaches a cache line boundary. The PCI Local Bus specification states that the transfer size must be a multiple of the cache line size. The LSI53C1030 selects the largest multiple of the cache line size based on the transfer size. When the DMA buffer contains less data than the value Cache Line Size register specifies, the LSI53C1030 issues a Memory Write command on the next cache boundary to complete the data transfer.

#### 2.3.2.18 Memory Write Block Command

The LSI53C1030 uses this command to burst data to memory. The LSI53C1030 supports this command when operating in the PCI-X bus mode.

### 2.3.3 PCI Arbitration

The LSI53C1030 contains independent bus mastering functions for each of the SCSI functions and for the system interface. The system interface bus mastering function manages DMA operations as well as the request and reply message frames. The SCSI channel bus mastering functions manage data transfers across the SCSI channels.

The LSI53C1030 uses a single REQ/-GNT/ signal pair to arbitrate for access to the PCI bus. To ensure fair access to the PCI bus, the internal arbiter uses a round robin arbitration scheme to decide which of the three internal bus mastering functions can arbitrate for access to the PCI bus.

### 2.3.4 PCI Cache Mode

The LSI53C1030 supports an 8-bit Cache Line Size register. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. The LSI53C1030 determines when to issue a PCI cache command (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate), or PCI noncache command (Memory Read or Memory Write command).

### 2.3.5 PCI Interrupts

The LSI53C1030 signals an interrupt to the host processor either using PCI interrupt pins, INTx/ and ALT_INTx/, or using Message Signalled Interrupts (MSI). If using the PCI interrupt pins, the Interrupt Request Routing Mode bits in the Host Interrupt Mask register configure the routing of each interrupt to either the INTx/ and/or the ALT_INTx/ pin. The Interrupt Pin register configures the routing of each PCI function's interrupt signals to either the interrupt A pins (INTA/, ALT_INTA/) or the interrupt B pins (INTB/ or ALT_INTB/).

If using MSI, the LSI53C1030 does not signal interrupts on INTx/ or ALT_INTx/. Note that enabling MSI to mask PCI interrupts is a violation of the PCI specification. Each PCI function of the LSI53C1030

implements its own MSI register set. The LSI53C1030 supports one requested message and disables MSI after the chip powers-up or resets.

The Host Interrupt Mask register also prevents the assertion of a PCI interrupt to the host processor by selectively masking reply interrupts and system doorbell interrupts. This register masks both pin-based and MSI-based interrupts.

### 2.3.6 Power Management

The LSI53C1030 complies with the *PCI Power Management Interface Specification, Revision 1.1,* and the *PC2001 System Design Guide*. The LSI53C01030 supports the D0, D1, D2, $D3_{hot}$, and $D3_{cold}$ power states. D0 is the maximum power state, and D3 is the minimum power state. Power State D3 is further categorized as $D3_{hot}$ or $D3_{cold}$. Powering a function off places it in the $D3_{cold}$ Power State.

Bits [1:0] of the Power Management Control/Status register independently control the power state of each PCI device on the LSI53C1030. Table 2.2 provides the power state bit settings.

**Table 2.2 Power States**

| Power Management Control and Status Register, Bits [1:0] | Power State | Function |
|---|---|---|
| 0b00 | D0 | Maximum Power |
| 0b01 | D1 | Snooze Mode |
| 0b10 | D2 | Coma Mode |
| 0b11 | D3 | Minimum Power |

The following sections describe the PCI Function Power States D0, D1, D2, and D3. As the device transitions from one power level to a lower one, the attributes that occur in the higher power state level carry into the lower power state level. For example, Power State D2 includes the attributes for Power State D1, as well as the attributes defined for Power State D2. The following sections describe the PCI Function power states in conjunction with each SCSI function. Power state actions are separate for each SCSI function.

#### 2.3.6.1 Power State D0

Power State D0 is the maximum power state and is the power-up default state for each function. The LSI53C1030 is fully functional in this state.

#### 2.3.6.2 Power State D1

Per the *PCI Power Management Interface Specification,* Power State D1 must have an equal or lower power level than Power State D0. A function in Power State D1 places the SCSI core in the snooze mode. In the snooze mode, a SCSI reset does not generate an IRQ/ signal.

#### 2.3.6.3 Power State D2

Per the *PCI Power Management Interface Specification,* Power State D2 must have an equal or lower power level than Power State D1. A function in this state places the SCSI core in the coma mode. Placing the PCI Function in Power State D2 disables the SCSI and DMA interrupts, and suppresses the following PCI Configuration Space Command register enable bits:

- I/O Space Enable
- Memory Space Enable
- Bus Mastering Enable
- SERR/Enable
- Enable Parity Error Response

Therefore, the function's memory and I/O spaces cannot be accessed, and the PCI function cannot be a PCI bus master.

If the PCI function is changed from Power State D2 to Power State D1 or D0, the PCI function restores the previous values of the PCI Command register and asserts any interrupts that were pending before the function entered Power State D2.

#### 2.3.6.4 Power State D3

Per the *PCI Power Management Interface Specification,* Power State D3 must have an equal or lower power level than Power State D2. Power State D3 is the minimum power state and includes the $D3_{hot}$ and $D3_{cold}$ settings. $D3_{hot}$ allows the device to transition to D0 using software.

$D3_{cold}$ removes power from the LSI53C1030. $D3_{cold}$ can transition to D0 by applying VCC and resetting the device.

Placing a function in Power State D3 puts the LSI53C1030 core in the coma mode, clears the function's PCI Command register, and continually asserts the function's soft reset. Asserting soft reset clears all pending interrupts and 3-states the SCSI bus.

## 2.4 Ultra320 SCSI Functional Description

The LSI53C1030 provides two independent Ultra320 SCSI channels on a single chip. Each channel supports wide SCSI synchronous transfer rates up to 320 Mbytes/s across an SE or LVD SCSI bus. The integrated LVDlink transceivers support both LVD and SE signals and do not require external transceivers. The LSI53C1030 controller supports the Ultra320 SCSI, Ultra160 SCSI, Ultra2 SCSI, Ultra SCSI, and Fast SCSI interfaces.

### 2.4.1 Ultra320 SCSI Features

This section describes how the LSI53C1030 implements the features in the SPI-4 draft specification.

#### 2.4.1.1 Parallel Protocol Request (PPR)

A SCSI extended message negotiates the PPR parameters. The PPR parameters include the (1) transfer period, (2) maximum REQ/ACK offset, (3) QAS, (4) margin control settings (MCS), (5) transfer width, (6) IU_Request, (7) write flow, (8) read streaming, (9) RTI, (10) precompensation enable, (11) information unit transfers, and the (12) DT data phases between an initiator and a target.

#### 2.4.1.2 Double Transition (DT) Clocking

Ultra160 SCSI and Ultra320 SCSI implement DT clocking to provide speeds up to 80 megatransfers per second (megatransfers/s) for Ultra160 SCSI, and up to 160 megatransfers/s for Ultra320 SCSI. When implementing DT clocking, a SCSI device samples data on both the asserting and deasserting edge of REQ/ACK. DT clocking is only valid using an LVD SCSI bus.

### 2.4.1.3 Intersymbol Interference (ISI) Compensation

ISI Compensation uses paced transfers and precompensation to enable high data transfer rates. Ultra320 SCSI data transfers require the use of ISI Compensation.

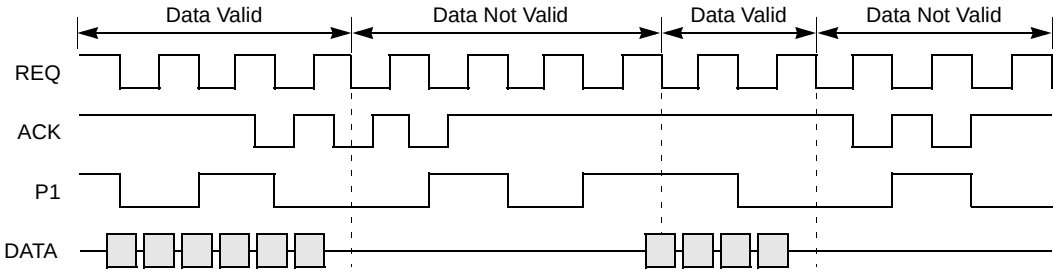
**Paced Transfers –** The initiator and target must establish a paced transfer agreement that specifies the REQ/ACK offset and the transfer period before using this feature. Devices can only perform paced transfers during Ultra320 SCSI DT data phases. In paced transfers, the device sourcing the data drives the REQ/ACK signal as a free running clock. The transition of the REQ/ACK signal, either the assertion or the negation, clocks data across the bus. For successful completion of a paced transfer, the number of ACK transitions must equal the number of REQ transitions and both the REQ and ACK lines must be negated.

The P1 line indicates valid data in 4-byte quantities by using its phase. The transmitting device indicates the start of valid data state by holding the state of the P1 line for the first two data transfer periods. Beginning on the third data transfer period, the transmitting device continues the valid data state by toggling the state of the P1 line every two data transfer periods for as long as the data is valid. The transmitting device must toggle the P1 line coincident with the REQ/ACK assertion. The method provides a minimum data valid period of two transfer periods.

To pause the data transfer, the transmitting device reverses the phase of P1 by withholding the next transition of P1 at the start of the first two invalid data transfer periods. Beginning with the third invalid data transfer period, the transmitting device toggles the P1 line every two invalid data transfer periods until it sends valid data. The transmitting device returns to the valid data state by reversing the phase of the P1 line. The invalid data state must experience at least one P1 transition before returning to the valid data state. This method provides a minimum data invalid period of four transfer periods.

Figure 2.2 provides a waveform diagram of paced data transfers and illustrates the use of the P1 line.

**Figure 2.2 Paced Transfer Example**

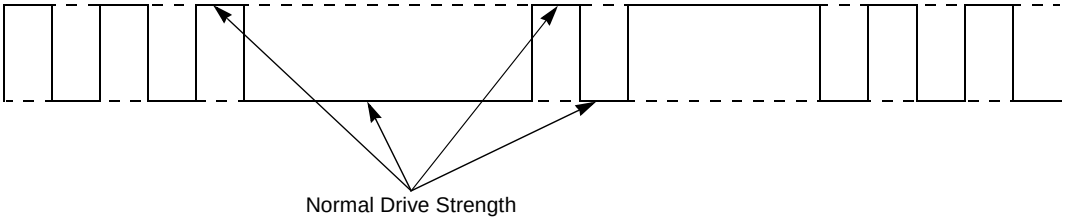



The LSI53C1030 uses the PPR negotiation that the SPI-4 draft standard describes to establish a paced transfer agreement for each initiator-target pair.

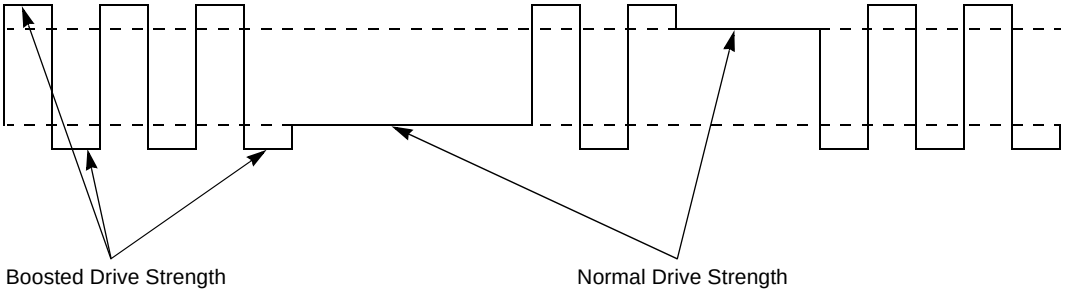
**Precompensation –** When transmitting in the Ultra320 SCSI mode, the LSI53C1030 uses precompensation to adjust the strength of the REQ, ACK, parity, and data signals. When a signal transitions to HIGH or LOW, the LSI53C1030 boosts the signal drive strength for the first data transfer period, and then lowers the signal drive strength on the second data transfer period if the signal remains in the same state. The LSI53C1030 maintains the lower signal drive strength until the signal again transitions HIGH or LOW. Figure 2.3 illustrates the drivers performance with precompensation enabled and disabled.

**Figure 2.3 Example of Precompensation**

**a. Drivers with Precompensation Disabled**




**b. Drivers with Precompensation Enabled**




### 2.4.1.4 Packetized Transfers

Packetized transfers are also referred to as *information unit transfers*. They reduce overhead on the SCSI bus by merging several of the SCSI bus phases. Packetized transfers can only occur in DT Data phases. The initiator and target must establish either a DT synchronous transfer agreement or a paced transfer agreement before performing packetized transfers.

The number of bytes in an information unit transfer is always a multiple of four. If the number of bytes to transfer in the information unit is not a multiple of four, the LSI53C1030 transmits pad bytes to bring the byte count to a multiple of four.

### 2.4.1.5 Quick Arbitration and Selection (QAS)

When using packetized transfers, QAS allows devices to arbitrate for the bus immediately after the message phase. QAS reduces the bus

overhead and maximizes bus bandwidth by skipping the bus free phase that normally follows a SCSI connection.

To perform QAS, the target sends a QAS request message to the initiator during the message phase of the bus. QAS capable devices snoop the SCSI bus for the QAS request message. If a QAS request message is seen, devices can immediately move to the arbitration phase without going to the bus free phase. The LSI53C1030 employs a fairness algorithm to ensure that all devices have equal bus access.

#### 2.4.1.6 Skew Compensation

The LSI53C1030 provides a method to account for and control system skew between the clock and data signals. Skew compensation is only available when the device operates in the Ultra320 SCSI mode. The initiator-target pair uses the training sequences in the SPI-4 draft standard to determine the skew compensation. Depending on the state of the RTI bit in the PPR negotiation, the LSI53C1030 can either execute this training pattern during each connection, or can execute the training pattern, store the adjustment parameters, and recall them on subsequent connections with the given device. The target determines when to execute the training pattern.

#### 2.4.1.7 Cyclic Redundancy Check (CRC)

Ultra320 SCSI and Ultra160 SCSI devices employ CRC as an error detection code during the DT Data phases. These devices transfer four CRC bytes during the DT Data phases to ensure reliable data transfers.

#### 2.4.1.8 SureLINK Domain Validation

SureLINK Domain Validation establishes the integrity of a SCSI bus connection between an initiator and a target. Under the SureLINK Domain Validation procedure, a host queries a device to determine its ability to communicate at the negotiated data transfer rate.

SureLINK Domain Validation provides 3 levels of integrity checking: Basic (Level 1) with inquiry command, Enhanced (Level 2) with read/write buffer, and Margined (Level 3) with drive strength margining and slew rate control. The basic check consists of an inquiry command to detect gross problems. The enhanced check sends a known data pattern using the read and write buffer commands to detect additional

problems. The margined check verifies that the physical parameters have a reasonable operating margin. Use SureLINK Domain Validation only during the diagnostic system checks and not during normal system operation. If transmission errors occur during any of these checks, the system can reduce the transmission rate on a per-target basis to ensure robust system operation.

## 2.4.2 SCSI Bus Interface

This section describes the SCSI bus modes that the LSI53C1030 supports and the SCSI bus termination methods necessary to operate a high speed SCSI bus.

### 2.4.2.1 SCSI Bus Modes

The LSI53C1030 supports SE and LVD transfers. To increase device connectivity and SCSI cable length, the LSI53C1030 features LVDlink technology, which is the LSI Logic implementation of LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI and a long-term migration path for faster SCSI transfer rates.

The A_DIFFSENS or B_DIFFSENS signals detect the different input voltages for HVD, LVD, and SE. The LSI53C1030 drivers are tolerant of HVD signal strengths, but do not support the HVD bus mode. The LSI53C1030 SCSI device 3-states its SCSI drivers when it detects an HVD signal level.

### 2.4.2.2 SCSI Termination

The terminator networks pull signals to an inactive voltage level and match the impedance seen at the end of the cable to the characteristic impedance of the cable. Install terminators at the extreme ends of the SCSI chain, and only at the ends; all SCSI buses must have exactly two terminators.

Note: If using the LSI53C1030 in a design with an 8-bit SCSI bus, designers must terminate all 16 data lines.

## 2.5 External Memory Interface

The LSI53C1030 provides Flash ROM, NVSRAM, and serial EEPROM interfaces. The Flash ROM interface stores the SCSI BIOS and firmware image. The Flash ROM is optional if the LSI53C1030 is not the boot device and a suitable driver exists to initialize the LSI53C1030. Integrated Mirroring (IM) technology requires an NVSRAM. The nonvolatile external serial EEPROM stores configuration parameters for the LSI53C1030.

### 2.5.1 Flash ROM Interface

The Flash ROM interface multiplexes the 8-bit address and data buses on the MAD[7:0] pins. The interface latches the address into three 8-bit latches to support up to 1 Mbyte of address space. The interface supports byte, word, and Dword accesses. The LSI53C1030 Dword aligns Dword reads, word aligns word reads, and byte aligns byte reads. The remaining bits from word and byte reads are meaningless.

The MAD[2:1] Power-On sense pin configurations define the size of the Flash ROM address space. Table 2.3 provides the pin encoding for these pins. By default, internal logic pulls these pins down to indicate that no Flash ROM is present.

**Table 2.3 Flash ROM Size Programming**

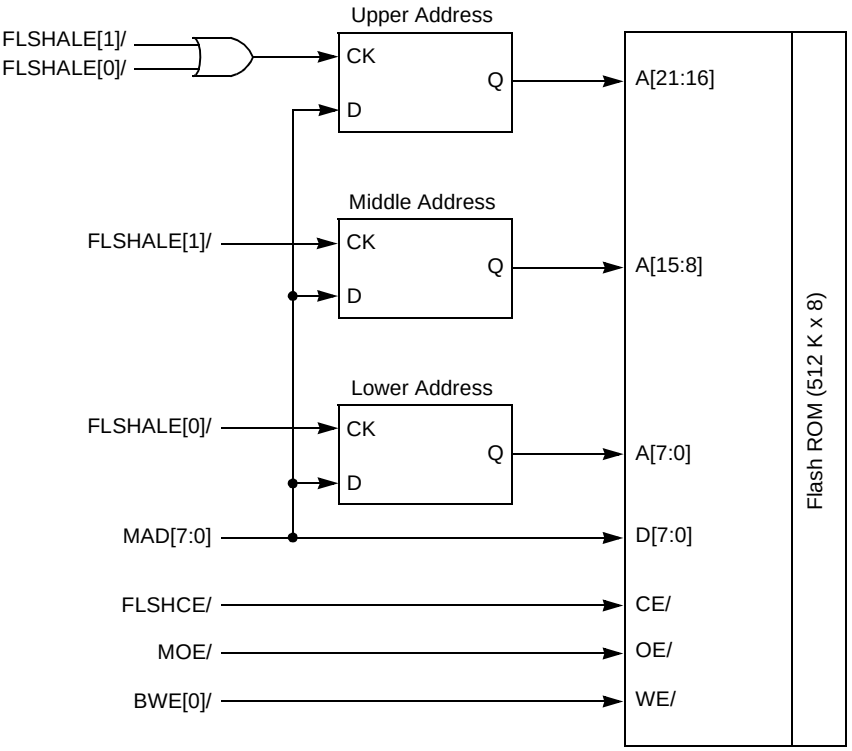
| MAD[2:1] Options | Flash ROM Size |
|---|---|
| 0b00 | No Flash ROM present (Default) |
| 0b01 | Up to 1024 Kbytes[1] |
| 0b10 | Reserved |
| 0b11 | |

1. Choose this setting for a 128 Kbyte or 512 Kbyte Flash ROM.

The LSI53C1030 defines only the middle (MA[15:8]) and lower (MA[7:0]) address ranges if the Flash ROM addressable space is 64 Kbytes or less. The LSI53C1030 defines the upper (MA[21:16]), middle (MA[15:8]), and lower (MA[7:0]) address ranges if the Flash ROM addressable space

is 128 Kbytes or more. Figure 2.4 provides an example of a Flash ROM configuration.

**Figure 2.4 Flash ROM Block Diagram**




The LSI53C1030 implements a Flash signature recognition mechanism to determine if the Flash contains a valid image. The Flash can be present and not contain a valid image either before its initial programming or during board testing. The first access to the Flash is a 16-byte burst read beginning at Flash address 0x000000. The LSI53C1030 compares the values read to the Flash signature values that Table 2.4 provides. If the signature values match, the LSI53C1030 performs the instruction located at Flash address 0x000000. If the signature values do not match, the LSI53C1030 records an error and ignores the Flash instruction. The Flash signature does not include the first three bytes of Flash memory as these bytes contain a branch offset instruction.

**Table 2.4 Flash Signature Value**

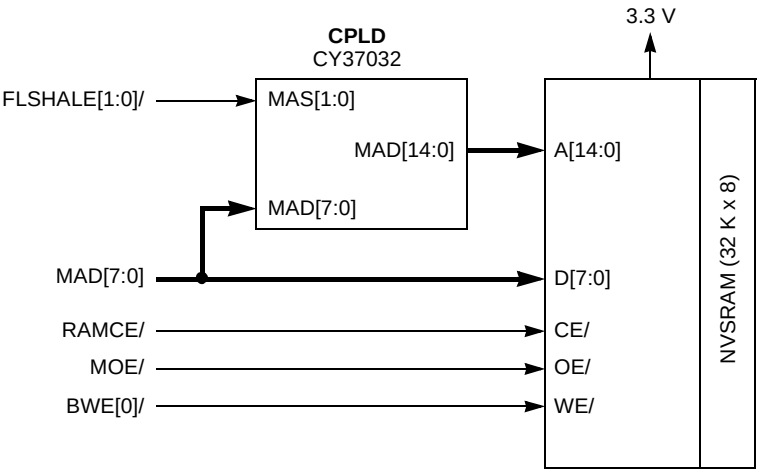
| Flash Address | Flash Signature Values | | | |
|---|---|---|---|---|
| Bytes [3:0] | 0xEA | XX | XX | XX |
| Bytes [7:4] | 0x5A | 0xEA | 0xA5 | 0x5A |
| Bytes [11:8] | 0xA5 | 0x5A | 0xEA | 0xA5 |
| Bytes [15:12] | 0x5A | 0xA5 | 0x5A | 0xEA |

### 2.5.2 NVSRAM Interface

Write journaling for IM requires an NVSRAM. The LSI53C1030 Fusion-MPT firmware is capable of maintaining a second disk as a mirror of the boot drive. To do so, the LSI Logic Fusion-MPT firmware writes to both the boot drive and the mirror drive. The mirroring of the boot drive is transparent to the BIOS, drivers, and operating system. Figure 2.5 provides a block diagram illustrating how to connect the NVSRAM. This design employs the CPLD to latch the address instead of using separate address latches.

When using an NVSRAM, pull the MAD[3] Power-On Sense pin HIGH during board boot-up. This configures the external memory interface as an NVSRAM interface. During operation, RAMCE/ selects the NVSRAM when MAD[3] is pulled HIGH.

**Figure 2.5 NVSRAM Diagram**




## 2.6 Serial EEPROM Interface

The nonvolatile external serial EEPROM stores configuration fields for the LSI53C1030. The serial EEPROM contains fields for the Subsystem ID(s), Subsystem Vendor ID(s), and the size of the PCI Diagnostic Memory Space. The LSI53C1030 must establish each of these parameters prior to reading system BIOS and loading the PCI Configuration Space registers. The power-on option settings enable the download of PCI configuration data from the serial EEPROM. For more information on the setting of the power-on options, refer to Section 3.10, "Power-On Sense Pins Description."

A 2-wire serial interface provides the connection to the serial EEPROM. During initialization, the firmware checks if a serial EEPROM exists. Firmware uses the checksum byte to determine if the configuration held in the serial EEPROM is valid. If the checksum fails the firmware checks for a valid NVData signature. If a valid NVData signature is found the firmware individually checksums each persistent configuration page to find the invalid page or pages. Table 2.5 provides the structure of the configuration record in the serial EEPROM.

**Table 2.5 PCI Configuration Record in Serial EEPROM**

| EEPROM Address | Configuration Data |
|---|---|
| 0x00 | PCI Function [0] Subsystem ID, bits [7:0] |
| 0x01 | PCI Function [0] Subsystem ID, bits [15:8] |
| 0x02 | PCI Function [0] Subsystem Vendor ID, bits [7:0] |
| 0x03 | PCI Function [0] Subsystem Vendor ID, bits [15:8] |
| 0x04 | PCI Diagnostic Memory Size |
| 0x05 | Reserved |
| 0x06 | PCI Function [1] Subsystem ID, bits [7:0] |
| 0x07 | PCI Function [1] Subsystem ID, bits [15:8] |
| 0x08 | PCI Function [1] Subsystem Vendor ID, bits [7:0] |
| 0x09 | PCI Function [1] Subsystem Vendor ID, bits [15:8] |
| 0x0A | Checksum |

## 2.7 Zero Channel RAID

Zero channel RAID (ZCR) capabilities enable the LSI53C1030 to respond to accesses from a PCI RAID controller card or chip that is able to generate ZCR cycles. The LSI53C1030's ZCR functionality is controlled through the ZCR_EN/ and the IOPD_GNT/ signals. Both of these signals have internal pull-ups and are active LOW.

The ZCR_EN/ signal enables ZCR support on the LSI53C1030. Pulling ZCR_EN/ HIGH disables ZCR support on the LSI53C1030 and causes the LSI53C1030 to behave as a normal PCI-X to Ultra320 SCSI controller. When ZCR is disabled, the IOPD_GNT/ signal has no effect on the LSI53C1030 operation.

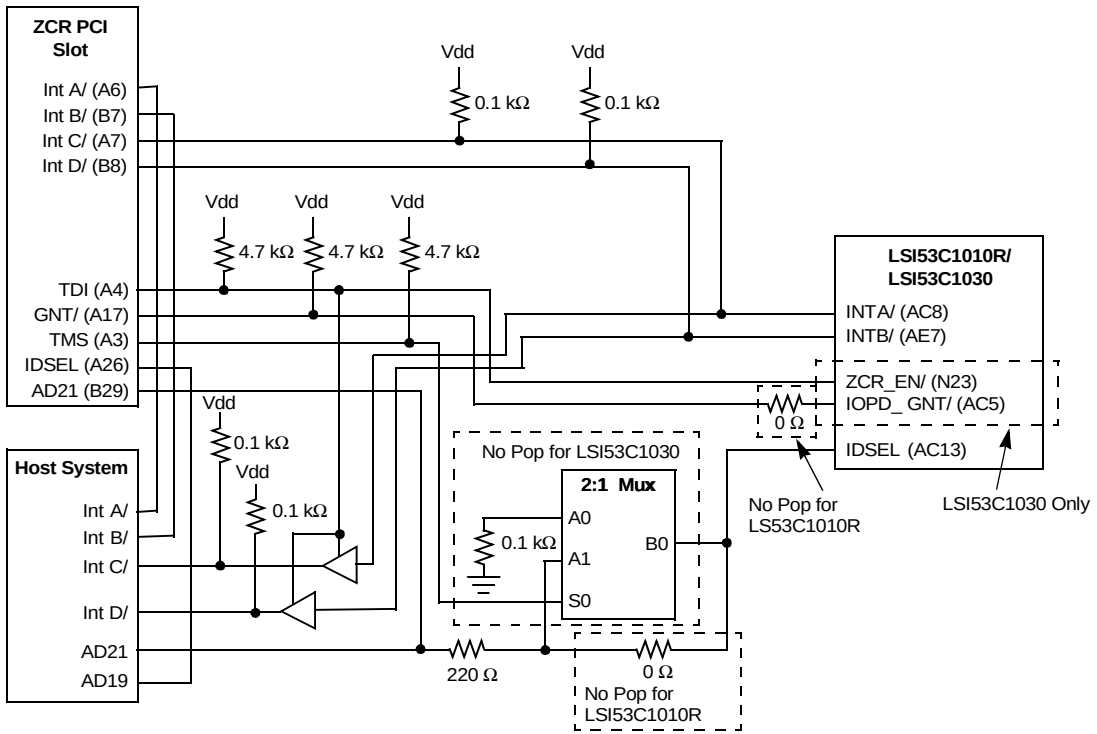
Pulling ZCR_EN/ LOW enables ZCR operation. When ZCR is enabled, the LSI53C1030 responds to PCI configuration cycles when the IOPD_GNT/ and IDSEL signal are asserted. Connect the IOPD_GNT/ pin on the LSI53C1030 to the PCI GNT/ signal of the external I/O processor. This allows the I/O processor to perform PCI configuration

cycles to the LSI53C1030 when the I/O processor is granted the PCI bus. This configuration also prevents the system processor from accessing the LSI53C1030 PCI configuration registers.

LSI53C1030 based designs do not use the M66EN pin to determine the PCI bus speed.

Figure 2.6 illustrates how to connect the LSI53C1030 to enable ZCR. This figure also contains information for connecting the LSI53C1010R based designs to a ZCR design and migrating from LSI53C1010R based designs to LSI53C1030 based designs. Notice that the LSI53C1030 does not require the 2:1 mux.

**Figure 2.6 ZCR Circuit Diagram for LSI53C1030 and LSI53C1010R**




Note: To maintain proper interrupt mapping, select the address line for use as IDSEL on the LSI53C1010R/LSI53C1030 to be +2 address lines above IDSEL on ZCR slot.

## 2.8 Multi-ICE Test Interface

This section describes the LSI Logic requirements for the Multi-ICE test interface. LSI Logic recommends that all test signals be routed to a header on the board.

The Multi-ICE test interface header is a 20-pin header for Multi-ICE debugging through the ICE JTAG port. This header is essential for debugging both the firmware and the design functionality and must be included in board designs. The connector is a 20-pin header that mates with the IDC sockets mounted on a ribbon cable. Table 2.6 details the pinout of the 20 pin header.

**Table 2.6 20-Pin Multi-ICE Header Pinout**

| Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|
| 1 | VDD | 2 | VDD |
| 3 | TRST_ICE/[1] | 4 | VSS |
| 5 | TDI_ICE[1] | 6 | VSS |
| 7 | TMS_ICE[1] | 8 | VSS |
| 9 | TCK_ICE[1] | 10 | VSS |
| 11 | RTCK_ICE | 12 | VSS |
| 13 | TDO_ICE | 14 | VSS |
| 15 | No Connect | 16 | VSS |
| 17 | No Connect | 18 | VSS |
| 19 | No Connect | 20 | VSS |

1. The designer must connect a 4.7 kΩ resistor from this signal to 3.3 V.

# Chapter 3
# Signal Description

This chapter describes the input and output signals of the LSI53C1030. The chapter consists of the following sections:



A slash (/) at the end of a signal indicates that the signal is active LOW. When the slash is absent, the signal is active HIGH. NC designates a No Connect signal.

## 3.1 Signal Organization

The LSI53C1030 has six major interfaces:

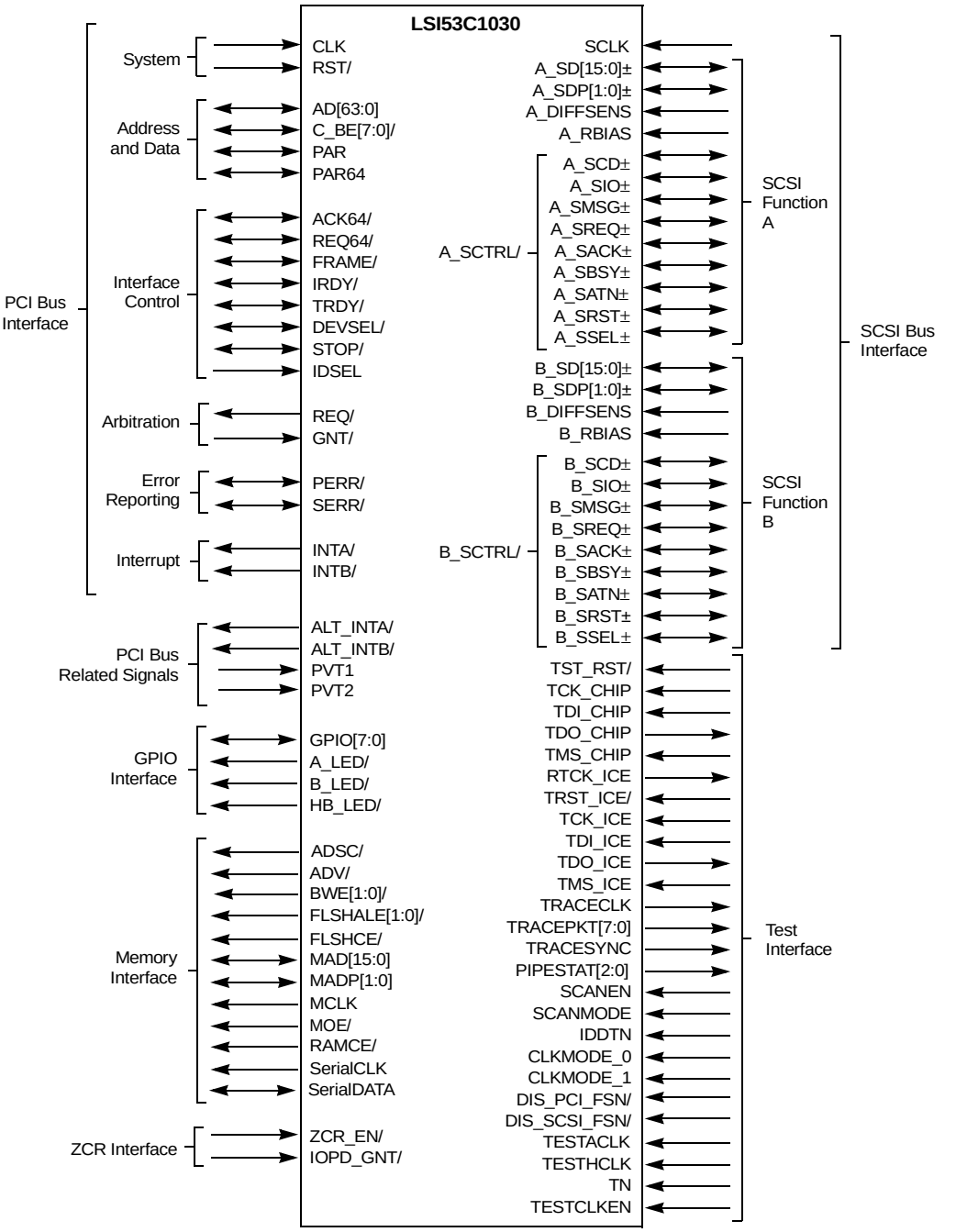
- PCI Bus Interface
- SCSI Bus Interface
- Memory Bus Interface
- ZCR Interface
- Test Interface
- General Purpose I/O (GPIO) Interface

There are five signal types:

| | |
|---|---|
| I | Input, a standard input-only signal |
| O | Output, a standard output driver (typically a Totem Pole output) |
| I/O | Input and output (bidirectional) |
| P | Power |
| G | Ground |

Figure 3.1 contains the functional signal groupings of the LSI53C1030. Figure 5.12 on page 5-22 provides a diagram of the LSI53C1030 456 Ball Grid Array (BGA). Table 5.20 and Table 5.21 on page 5-24 and page 5-26 provide pinout listings for the LSI53C1030.

## Figure 3.1 LSI53C1030 Functional Signal Grouping



## 3.2 PCI Bus Interface Signals

This section describes the PCI interface. The PCI interface consists of the System, Address and Data, Interface Control, Arbitration, Error Reporting, and Interrupt signal groups.

### 3.2.1 PCI System Signals

Table 3.1 describes the PCI System signals group.

**Table 3.1 PCI System Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| CLK | AC22 | I | N/A | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| RST/ | AB10 | I | N/A | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |

### 3.2.2 PCI Address and Data Signals

Table 3.2 describes the PCI Address and Data signals group.

**Table 3.2 PCI Address and Data Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| AD[63:0] | W22, AB25, AC26, AA25, W23, Y25, Y26, V22, U22, V24, V23, U24, V25, W26, U23, U25, T22, T23, T25, R25, R22, P22, P23, R23, P24, P25, T26, R26, M26, L26, N25, N24, AE9, AF8, AE10, AB11, AC11, AE11, AE12, AB12, AC12, AD13, AE13, AF11, AF16, AE14, AC15, AC14, AD17, AE19, AC18, AB17, AB18, AF20, AE20, AC19, AF23, AE22, AB19, AD21, AF24, AC20, AE23, AC21 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| C_BE[7:0]/ | AA23, AC25, Y23, AD26, AB13, AB14, AE18, AE21 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| PAR | AF19 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| PAR64 | AA24 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |

### 3.2.3 PCI Interface Control Signals

Table 3.3 describes the PCI Interface Control signals group.

**Table 3.3 PCI Interface Control Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| ACK64/ | AB20 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| REQ64/ | AD22 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| FRAME/ | AB15 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| IRDY/ | AE15 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| TRDY/ | AE16 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| DEVSEL/ | AC16 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| STOP/ | AB16 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| IDSEL | AC13 | I | N/A | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |

### 3.2.4 PCI Arbitration Signals

Table 3.4 describes the PCI Arbitration signals group.

**Table 3.4 PCI Arbitration Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| REQ/ | AD10 | O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| GNT/ | AE8 | I | N/A | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |

### 3.2.5 PCI Error Reporting Signals

Table 3.5 describes the PCI Error Reporting signals group.

**Table 3.5 PCI Error Reporting Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| PERR/ | AE17 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |
| SERR/ | AC17 | I/O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description. |

### 3.2.6 PCI Interrupt Signals

Table 3.6 describes the PCI Interrupt signals group.

**Table 3.6 PCI Interrupt Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| INTA/ | AC8 | O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description.<br><br>The LSI53C1030 can route interrupts to INTA/ and/or ALT_INTA/. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTA/ and/or ALT_INTA/. |
| INTB/ | AE7 | O | 8 mA PCI | Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a*, for this signal description.<br><br>The LSI53C1030 can route interrupts to INTB/ and/or ALT_INTB/. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTB/ and/or ALT_INTB/. |

## 3.3 PCI-Related Signals

Table 3.7 describes the PCI-related signals.

**Table 3.7 PCI-related Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| ALT_INTA/ | AF7 | O | 8 mA PCI | Active LOW **Alternate Interrupt A** indicates that PCI Function [0] is requesting service from its host device driver. ALT_INTA/ is an open drain signal. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTA/ and/or ALT_INTA/. |
| ALT_INTB/ | AB9 | O | 8 mA PCI | Active LOW **Alternate Interrupt B** indicates that PCI Function [1] is requesting service from its host device driver. ALT_INTB/ is an open drain signal. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTB/ and/or ALT_INTB/. |
| PVT2, PVT1 | AF4, AE5 | I | N/A | **PVT2** and **PVT1** provide biasing for PCI signals. Connect a 49.9 Ω, 1% resistor between PVT2 and PVT1. |

## 3.4 SCSI Interface Signals

The SCSI Interface signals section describes the signals for the SCSI Channel [0] and SCSI Channel [1] interfaces. Table 3.8 describes the SCSI bus clock signal that is common to both SCSI Channel [0] and SCSI Channel [1].

In the LVD mode, the negative and positive signals form the differential pair. In the SE mode, the negative signals represent the signal pin and the positive signals are a virtual ground. The LSI53C1030 does not support the HVD mode. If HVD signalling is present, the SCSI channel 3-states its drivers.

**Table 3.8 SCSI Bus Clock Signal**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| SCLK | F3 | I | N/A | **SCSI Clock** provides the 80 MHz reference clock source for the ARM966E-S processors and all SCSI-related timings. |

### 3.4.1 SCSI Channel [0] Signals

Table 3.9 describes the SCSI Channel [0] Interface signals.

**Table 3.9 SCSI Channel [0] Interface Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| A_SD[15:0]-<br><br>A_SD[15:0]+ | Y1, AA2, AB2, AD1, F2, G2, J4, H1, R4, T5, T2, U2, U5, V2, V4, W4<br><br>W5, Y2, AA3, AC1, D1, G1, H4, H2, P3, R5, R2, T4, U4, U3, V5, V3 | I/O | SE:<br>48 mA<br><br>LVD:<br>12 mA | **SCSI Channel [0] Data** signals. |
| A_SDP[1:0]-<br>A_SDP[1:0]+ | W2, P4<br>W1, P5 | I/O | SE:<br>48 mA<br><br>LVD:<br>12 mA | **SCSI Channel [0] Data Parity** signals. |

**Table 3.9 SCSI Channel [0] Interface Signals (Cont.)**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| A_VDDBIAS | T1 | O | N/A | **A_VDDBIAS** provides power for the A_RBIAS circuit. |
| A_RBIAS | R1 | I | N/A | Connect a 9.76 kΩ or 10.0 kΩ resistor between the A_VDDBIAS and **A_RBIAS** pins to generate the LVD signalling pad bias current. |
| A_DIFFSENS | E2 | I | N/A | The **SCSI Channel [0] Differential Sense** pin detects the present mode of the SCSI bus. This signal is 5 V tolerant and must connect to the DIFFSENS signal on the physical SCSI bus.<br><br>SE Mode: Driving this pin below 0.5 V (LOW) indicates an SE bus and places SCSI Channel [0] in the SE bus mode.<br><br>LVD Mode: Driving this signal between 0.7 V and 1.9 V (intermediate) indicates an LVD mode and places SCSI Channel [0] in the LVD bus mode.<br><br>HVD Mode: Driving this pin above 2.0 V (HIGH) indicates an HVD bus and causes SCSI Channel [0] to 3-state its SCSI drivers. |

Table 3.10 describes the SCSI Channel [0] Control signals.

**Table 3.10 SCSI Channel [0] Control Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| A_SCD–<br>A_SCD+ | K3<br>K4 | I/O | SE:<br>48 mA | SCSI Channel [0] **Command/Data**. |
| A_SIO–<br>A_SIO+ | K5<br>J5 | | LVD:<br>12 mA | SCSI Channel [0] **Input/Output**. |
| A_SMSG–<br>A_SMSG+ | L2<br>L1 | | | SCSI Channel [0] **Message**. |
| A_SREQ–<br>A_SREQ+ | J2<br>J3 | | | SCSI Channel [0] **Request**. |
| A_SACK–<br>A_SACK+ | M5<br>L5 | | | SCSI Channel [0] **Acknowledge**. |
| A_SBSY–<br>A_SBSY+ | N3<br>N4 | | | SCSI Channel [0] **Busy**. |
| A_SATN–<br>A_SATN+ | M4<br>N5 | | | SCSI Channel [0] **Attention**. |
| A_SRST–<br>A_SRST+ | M1<br>M2 | | | SCSI Channel [0] **Bus Reset**. |
| A_SSEL–<br>A_SSEL+ | L4<br>K2 | | | SCSI Channel [0] **Select.** |

### 3.4.2 SCSI Channel [1] Signals

Table 3.11 describes the SCSI Channel [1] Interface signals.

**Table 3.11 SCSI Channel [1] Interface Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| B_SD[15:0]-<br><br>B_SD[15:0]+ | D8, E8, C6, A3, B21, D19, E18, A19, E13, A12, B11, B10, D10, C9, D9, B8<br><br>B7, B6, B5, A4, A23, B20, A20, B19, E12, B12, D11, C10, E11, E10, B9, A8 | I/O | SE: 48 mA<br><br>LVD: 12 mA | **SCSI Channel [1] Data** signals. |
| B_SDP[1:0]-<br>B_SDP[1:0]+ | A7, D12<br>E9, C13 | I/O | SE: 48 mA<br><br>LVD: 12 mA | **SCSI Channel [1] Data Parity** signals. |
| B_VDDBIAS | B13 | O | N/A | **B_VDDBIAS** provides power for the B_RBIAS circuit. |
| B_RBIAS | A11 | I | N/A | Connect a 9.76 kΩ or 10.0 kΩ resistor between the B_VVDBIAS and **B_RBIAS** pins to generate the LVD signalling pad bias current. |
| B_DIFFSENS | B22 | I | N/A | The **SCSI Channel [1] Differential Sense** pin detects the present mode of the SCSI bus. This signal is 5 V tolerant and must connect to the DIFFSENS signal on the physical SCSI bus.<br><br>SE Mode: Driving this pin below 0.5 V (low) indicates an SE bus and places SCSI Channel [1] in the SE mode.<br><br>LVD Mode: Driving this signal between 0.7 V and 1.9 V (intermediate) indicates an LVD bus and places SCSI Channel [1] in the LVD mode.<br><br>HVD Mode: Driving this pin above 2.0 V (high) indicates an HVD bus and causes SCSI Channel [1] to 3-state its SCSI drivers. |

Table 3.12 describes the SCSI Channel [1] Control signals.

**Table 3.12 SCSI Channel [1] Control Signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| B_SCD-<br>B_SCD+ | E16<br>D17 | I/O | SE:<br>48 mA | SCSI Channel [1] **Command/Data**. |
| B_SIO-<br>B_SIO+ | E17<br>D18 | | LVD:<br>12 mA | SCSI Channel [1] **Input/Output**. |
| B_SMSG-<br>B_SMSG+ | B16<br>D16 | | | SCSI Channel [1] **Message**. |
| B_SREQ-<br>B_SREQ+ | B18<br>C18 | | | SCSI Channel [1] **Request**. |
| B_SACK-<br>B_SACK+ | D14<br>E14 | | | SCSI Channel [1] **Acknowledge**. |
| B_SBSY-<br>B_SBSY+ | A15<br>B15 | | | SCSI Channel [1] **Busy**. |
| B_SATN-<br>B_SATN+ | B14<br>D13 | | | SCSI Channel [1] **Attention**. |
| B_SRST-<br>B_SRST+ | E15<br>A16 | | | SCSI Channel [1] **Bus Reset**. |
| B_SSEL-<br>B_SSEL+ | B17<br>C17 | | | SCSI Channel [1] **Select.** |

## 3.5 Memory Interface

Table 3.13 describes the Flash ROM/NVSRAM Interface signals.

**Table 3.13 Flash ROM/NVSRAM Interface Pins**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| MCLK | E20 | O | 4 mA | Reserved. |
| ADSC/ | D21 | O | 4 mA | Reserved. |
| ADV/ | B23 | O | 4 mA | Reserved. |

**Table 3.13 Flash ROM/NVSRAM Interface Pins (Cont.)**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| MAD[15:0] | D22, E21, B25, D23, E22, C24, F22, E23, D26, E25, H22, F24, G23, D25, F23, G22 | I/O | 8 mA | The **Memory Address and Data Bus** carries the memory and address signals for the Flash ROM and NVSRAM interfaces on MAD[7:0]. These pins also provide the Power-On Sense options that configure operating parameters during chip power up or reset. |
| MADP[1:0] | C22, B24 | I/O | 8 mA | The **Memory Address and Data Parity** signals provide parity checking for MAD[15:0]. By default, the LSI53C1030 uses even parity. The user can enable odd parity through the Fusion-MPT architecture. These pins also provide the Power-On Sense options that configure operating parameters during chip power up or reset. |
| MOE/ | G26 | O | 4 mA | The LSI53C1030 asserts active LOW **Memory Output Enable** to indicate that the selected NVSRAM or Flash ROM device can drive data. This signal is typically an asynchronous input to NVSRAM and/or Flash ROM devices. |
| BWE[1:0]/ | E24, H23 | O | 8 mA | The LSI53C1030 asserts active LOW **Memory Byte Write Enables** to allow single byte writes to the NVSRAM. BWE0/ enables writes on MAD[7:0]. |
| RAMCE/ | D20 | O | 8 mA | When MAD[3] is pulled HIGH, the LSI53C1030 asserts active LOW synchronous **RAM Chip Enable** to select the NVSRAM. |
| FLSHCE/ | G25 | O | 8 mA | The LSI53C1030 asserts active LOW **Flash Chip Enable** to enable data transfers with a single 8-bit device. |
| FLSHALE[1:0]/ | J24, K22 | O | 8 mA | The Flash ROM and NVSRAM interfaces use active LOW **Flash Address Latch Enable**. For the Flash ROM, these signals provide clocks for address latches. For the NVSRAM, these signals provide the memory address strobe. |

Table 3.14 describes the serial EEPROM Interface signals.

**Table 3.14 Serial EEPROM Interface Pins**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| SerialCLK | J25 | O | 8 mA | **Serial EEPROM clock**. This signal requires a 4.7 kΩ external pull up resistor when an EEPROM is present. |
| SerialDATA | H26 | I/O | 8 mA | **Serial EEPROM data**. This signal requires a 4.7 kΩ external pull up resistor when an EEPROM is present. |

## 3.6 Zero Channel RAID Interface

Table 3.15 describes the zero channel RAID (ZCR) configuration signals.

**Table 3.15 ZCR Configuration Pins**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| ZCR_EN/ | N23 | I | N/A | This signal enables and disables ZCR support on the LSI53C1030. By default, this signal is internally pulled HIGH to disable ZCR operation. Pull this signal LOW to enable ZCR operation. |
| IOPD_GNT/ | AC5 | I | N/A | When ZCR is enabled on the LSI53C1030 the device only responds to PCI configuration cycles if IOPD_GNT/ or IDSEL is asserted. Connect IOPD_GNT/ to PCI GNT/ on the external I/O processor. |

## 3.7 Test Interface

Table 3.16 describes the JTAG and ICE debug signals.

**Table 3.16 JTAG, ICE, and Debug Pins**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| TST_RST/ | AD5 | I | N/A | Active low **Test Reset** is for test purposes. |
| TCK_CHIP | AC6 | I | N/A | **Chip Test Clock** provides a JTAG test clock signal. |
| TDI_CHIP | AF3 | I | N/A | **Chip Test Data In** provides the JTAG test data in signal. |
| TDO_CHIP | AD6 | O | 8 mA | **Chip Test Data Out** provides the JTAG test data out signal. |
| TMS_CHIP | AE4 | I | N/A | **Chip Test Mode Select** provides the JTAG test mode select signal. |
| RTCK_ICE | AA5 | O | 8 mA | **Test Clock Acknowledge** provides the JTAG test clock acknowledge signal for the In-Circuit Emulator (ICE) debug logic. |
| TRST_ICE/ | AB4 | I | N/A | **Test Reset** provides the JTAG test reset signal for the ICE debug logic. |
| TCK_ICE | AA4 | I | N/A | **Test Clock** provides the JTAG test clock signal for the ICE debug logic. |
| TDI_ICE | AB3 | I | N/A | **Test Data In** provides the JTAG test data in signal for the ICE debug logic. |
| TDO_ICE | AD2 | O | 8 mA | **Test Data Out** provides the JTAG test data out signal for the ICE debug logic. |
| TMS_ICE | Y5 | I | N/A | **Test Mode Select** provides the test mode select signal for the ICE debug logic. |
| TRACECLK | B3 | O | 8 mA | Reserved. |
| TRACEPKT[7:0] | F4, G5, E3, C2, E4, F5, B2, D4 | O | 8 mA | Reserved. |
| TRACESYNC | E5 | O | 8 mA | Reserved. |
| PIPESTAT[2:0] | C3, E6, D5 | O | 8 mA | Reserved. |

Table 3.17 lists the LSI Logic test signals.

**Table 3.17 LSI Logic Test Pins**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| SCANEN | N22 | I | N/A | **SCANEN** is for use only by LSI Logic. |
| SCANMODE | E7 | I | N/A | **SCANMODE** is for use only by LSI Logic. |
| IDDTN | Y4 | I | N/A | **IDDTN** is for use only by LSI Logic. |
| CLKMODE_0 | AA22 | I | N/A | **CLKMODE_0** is for use only by LSI Logic. |
| CLKMODE_1 | AC2 | I | N/A | **CLKMODE_1** is for use only by LSI Logic. |
| DIS_PCI_FSN/ | A24 | I | N/A | Pulling **DIS_PCI_FSN/** LOW disables the PCI FSN. Pulling this pin HIGH allows the chip to enable the PCI FSN when operating in PCI-X mode, or to disable the PCI FSN when operating in PCI mode. The LSI53C1030 controls the PCI FSN. |
| DIS_SCSI_FSN/ | AC4 | I | N/A | **DIS_SCSI_FSN/** is for use only by LSI Logic. |
| TESTACLK | AB6 | I | N/A | **TESTACLK** is for use only by LSI Logic. |
| TESTHCLK | AE2 | I | N/A | **TESTHCLK** is for use only by LSI Logic. |
| TN | C5 | I | N/A | **TN** is for use only by LSI Logic. |
| TESTCLKEN | D7 | I | N/A | **TESTCLKEN** is for use only by LSI Logic. |

## 3.8 GPIO and LED Signals

Table 3.18 describes the GPIO and LED signals group.

**Table 3.18 GPIO and LED signals**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| GPIO[7:0] | K25, L23, L25, M25, H25, K24, AE25, AC23 | I/O | 8 mA | **General purpose I/O pins**. The LSI53C1030 controls these signals and can configure them as inputs or as outputs. These pins default to input mode after chip initialization. |
| A_LED/ | J23 | O | 12 mA | **A_LED/** either drives the SCSI Channel [0] activity LED or provides a General Purpose I/O pin. A_LED can be controlled by firmware or driven by chip activity. |
| B_LED/ | K23 | O | 12 mA | **B_LED/** either drives the SCSI Channel [1] activity LED or provides a General Purpose I/O pin. B_LED/ can be controlled by firmware or driven by chip activity. |
| HB_LED/ | C25 | O | 12 mA | Firmware blinks **Heart Beat LED** at a 1.0 second interval when the IOP is operational. |

## 3.9 Power and Ground Pins

Table 3.19 describes the Power and Ground signals.

**Table 3.19 Power and Ground Pins**

| Signal Name | BGA Position | Type | Strength | Description |
|---|---|---|---|---|
| VDD_IO | A1, A2, A6, A10, A14, A18, A22, A26, C7, C11, C15, C19, C23, D3, E26, F1, G24, H3, J26, K1, L24, M3, N26, P1, R24, T3, U26, V1, W24, Y3, AA26, AB1, AC24, AD4, AD8, AD12, AD16, AD20, AE26, AF1, AF5, AF9, AF13, AF17, AF21, AF25 | P | N/A | **VDD_IO** provides power for the PCI bus drivers/receivers, SCSI bus drivers/receivers, local memory interface drivers/receivers, and other I/O pins. |
| VSS_IO | A5, A9, A13, A17, A21, A25, B1, B26, C4, C8, C12, C16, C20, D24, E1, F26, G3, H24, J1, K26, L3, L11-L16, M11-M16, M24, N1, N11-N16, P11-P16, P26, R3, R11-R16, T11-T16, T24, U1, V26, W3, Y24, AA1, AB26, AC3, AD7, AD11, AD15, AD19, AD23, AE1, AF2, AF6, AF10, AF14, AF18, AF22, AF26 | G | N/A | **VSS_IO** provides ground for the PCI bus drivers/receivers, SCSI bus drivers/receivers, local memory interface drivers/receivers, and other I/O pins. |
| VDDA[1] | AB21, C1 | P | N/A | **VDDA** provides the analog circuit power for the PLL circuit. |
| VSSA[1] | AD24, H5 | G | N/A | **VSSA** provides the analog circuit ground for the PLL circuit. |
| VDDC | D2, D6, D15, E19, J22, M22, N2, AC7, AD3, AD25, AE3, AE24, AF15 | P | N/A | **VDDC** provides power for the core logic. |
| VSSC | B4, C14, C21, C26, F25, G4, L22, P2, AB5, AB7, AB8, AB23, AB24, AD14 | G | N/A | **VSSC** provides ground for the core logic. |
| PCI5VBIAS | M23, W25, Y22, AB22, AC10, AD9, AD18, AE6, AF12 | I | N/A | Connects the **PCI 5V Tolerant** pins to 5 V in a 5 V system or to 3.3 V in a 3.3 V system. |
| NC | AC9 | – | N/A | No Connect. |

1. To reduce signal noise that can affect FSN functionality, place a ferrite bead in series with the VDDA and VSSA pins. LSI Logic recommends a bead with a rating of 150 Ω at 100 MHz.

## 3.10 Power-On Sense Pins Description

In addition to providing the address/data bus for the external memory interface, MAD[15:0] and MADP[1:0] provide eighteen Power-On Sense pins that configure global operating conditions within the LSI53C1030. The MAD[15:0] and MADP[1:0] pins have internal pull-down current sinks and sense a logical 0 if no pull-up resistor is present on the pin. To program a particular option, allow the internal pull-down to pull the pin LOW or connect a 4.7 kΩ resistor between the appropriate pin and VDD to pull the pin HIGH. The LSI53C1030 samples these pins during PCI reset and holds their values upon the removal of PCI reset. Table 3.20 provides the MAD Power-On Sense pin configuration options. LSI Logic expects most configurations to employ the default settings. Provide pull-up options for all MAD pins.

**Table 3.20 MAD Power-On Sense Pin Options**

| MAD Pin | Function | Pulled-Down (Default) | Pulled-Up |
|---|---|---|---|
| MADP[1] | Reserved | | |
| MADP[0] | PCI-X Mode | Enables the PCI-X Mode. | Disables the PCI-X Mode. |
| MAD[15] | 133 MHz PCI-X | Enables 133 MHz PCI-X Mode. | Disables 133 MHz PCI-X Mode. |
| MAD[14] | 64-bit PCI | Configures a 64-bit PCI Bus. | Configures a 32-bit PCI Bus. |
| MAD[13] | 66 MHz PCI | Enables the 66 MHz PCI Mode. | Disables the 66 MHz PCI Mode. |
| MAD[12] | Reserved | | |
| MAD[11] | ID Control [1] | Has no effect. | Sets bit [15] of the PCI Function [1] Subsystem ID register to 0b1. |
| MAD[10] | ID Control [0] | Has no effect. | Sets bit [15] of the PCI Function [0] Subsystem ID register to 0b1. |
| MAD[9:8] | Reserved | | |
| MAD[7] | Serial EEPROM Download Enable | Enables the download of the PCI configuration information from the serial EEPROM. | Disables the download of the PCI configuration information from the serial EEPROM. |
| MAD[6] | IOP Boot Enable | Enables the IOP boot process. | Disables the IOP boot process. |
| MAD[5:4] | PCI/SCSI Configuration | Configures the LSI53C1030 according to Table 3.21. | |

**Table 3.20 MAD Power-On Sense Pin Options (Cont.)**

| MAD Pin | Function | Pulled-Down (Default) | Pulled-Up |
|---|---|---|---|
| MAD[3] | NVSRAM Select | Has no effect. | Configures the LSI53C1030 to support an NVSRAM. |
| MAD[2:1] | Flash ROM Size | Configures the Flash ROM size according to Table 3.22. | |
| MAD[0] | Reserved | | |

- **MADP[1]**, Reserved.
- **MADP[0], PCI-X Mode** – By default, internal logic pulls this pin LOW to enable the PCI-X mode on the LSI53C1030. Pulling this pin HIGH disables the PCI-X mode on the LSI53C1030. Pull this pin HIGH when the host board does not support the PCI-X mode. The setting of this pin must coincide with the setting of the PCI_CAP pin on the host board. When the PCI-X mode is disabled, the PCI-X extended capabilities register structure is not visible in PCI Configuration Space.
- **MAD[15], 133 MHz PCI-X** – By default, internal logic pulls this pin LOW to enable 133 MHz PCI-X operation and to set the 133 MHz Capable bit in the PCI-X Status register. Pulling this pin HIGH disables 133 MHz PCI-X operation and clears the 133 MHz Capable bit in the PCI-X Status register.
- **MAD[14], 64-bit PCI** – By default, internal logic pulls this pin LOW to enable 64-bit PCI operation and to set the 64-bit Enable bit in the PCI-X Status register. Pulling this pin HIGH configures the PCI connection as a 32-bit connection and clears the 64-bit Enable bit in the PCI-X Status register.
- **MAD[13], 66 MHz PCI** – By default, internal logic pulls this pin LOW to enable 66 MHz PCI operation on the LSI53C1030 and to set the 66 MHz Capable bit in the PCI Status register. Pulling this pin HIGH disables 66 MHz PCI operation and clears the 66 MHz Capable bit in the PCI Status register.
- **MAD[12],** Reserved.
- **MAD[11], ID Control [1]** – By default, internal logic pulls this pin LOW. Pulling this signal LOW either allows the serial EEPROM to program bit 15 of the PCI Function [1] Subsystem ID register or

allows this bit to default to 0b0. Pulling this pin HIGH sets this bit to 0b1.

- **MAD[10], ID Control [0]** – By default, internal logic pulls this pin LOW. Pulling this signal LOW either allows the serial EEPROM to program bit 15 of the PCI Function [0] Subsystem ID register or allows this bit to default to 0b0. Pulling this pin HIGH sets this bit to 0b1.
- **MAD[9:8]**, Reserved.
- **MAD[7], Serial EEPROM Download Enable** – By default, internal logic pulls this pin LOW to enable the download of PCI configuration information from the serial EEPROM. Pulling this pin HIGH disables the download of the PCI configuration information from the serial EEPROM. Disabling the download of PCI configuration information defaults the Subsystem Vendor ID register to 0x1000 and defaults Subsystem ID register for the respective PCI Function to either 0x1000 if MAD[11:10] are pulled LOW or to 0x8000 if MAD[11:10] are pulled HIGH.
- **MAD[6], IOP Boot Enable** – By default, internal logic pulls this pin LOW. In the default mode, the IOP starts the boot process and downloads firmware from the Flash ROM. Pulling this pin HIGH causes the IOP to await a firmware download from the host system.
- **MAD[5:4], PCI Single/Multifunction and SCSI Single/Dual Channel Configuration** – These pins work in conjunction with each other to configure the LSI53C1030 as a single function PCI-X to single channel SCSI controller or a multifunction PCI-X to dual channel SCSI controller. By default, hardware internally pulls MAD[5:4] down to configure the LSI53C1030 as multifunction PCI-X to dual channel SCSI controller. The user may pull MAD[5:4] HIGH to configure the LSI53C1030 as a single function PCI-X to single channel SCSI controller. This configuration enables PCI Function [0] and SCSI Channel [0], disables PCI Function [1] and SCSI Channel [1], and programs the PCI Function [0] Header Type register to indicate a single function PCI device. LSI Logic does not support multifunction PCI-X to single channel SCSI or single function PCI-X to dual channel SCSI configurations. Table 3.21 provides the MAD[5:4] pin encoding definitions.

**Table 3.21 PCI-X Function to SCSI Channel Configurations**

| MAD[5:4] Options | LSI53C1030 Configuration |
|---|---|
| 0b00 | Multifunction PCI-X to Dual Channel SCSI Controller |
| 0b01 | Reserved |
| 0b10 | Reserved |
| 0b11 | Single Function PCI-X to Single Channel SCSI Controller |

- **MAD[3], NVSRAM Select** – By default, internal logic pulls this pin LOW, which has no effect on the LSI53C1030. Pulling this pin HIGH configures the external memory interface as an NVSRAM interface.
- **MAD[2:1], ROM Size** – These pins program the size of the Flash ROM memory. Refer to Table 3.22 for the pin encoding. By default, internal logic pulls these pins LOW to indicate that a Flash ROM is not present in the system.

**Table 3.22 Flash ROM Size Programming**

| MAD[2:1] Options | Flash ROM Size |
|---|---|
| 0b00 | Flash ROM not present (Default) |
| 0b01 | Up to 1024 Kbytes[1] |
| 0b10 | Reserved |
| 0b11 | |

1. Choose this setting for a 128 Kbyte or 512 Kbyte Flash ROM.

- **MAD[0]**, Reserved.

## 3.11 Internal Pull-ups and Pull-downs

Table 3.23 describes the pull-up and pull-down signals for the LSI53C1030.

**Table 3.23 Pull-up and Pull-down Conditions**

| Signal Name | BGA Position | Pull Type |
|---|---|---|
| MAD[15:0], MADP[1:0] | D22, E21, B25, D23, E22, C24, F22, E23, D26, E25, H22, F24, G23, D25, F23, G22, C22, B24 | Internal Pull-down. |
| SerialDATA, SerialCLK | H26, J25 | Internal Pull-down. Pull-up externally when connected to a serial EEPROM. |
| GPIO[7:0] | K25, L23, L25, M25, H25, K24, AE25, AC23 | Internal Pull-down. |
| TST_RST/ | AD5 | Internal Pull-up. |
| TCK_CHIP, TDI_CHIP, TMS_CHIP | AC6, AF3, AE4 | Internal Pull-down. |
| TRST_ICE/, TCK_ICE, TDI_ICE, TMS_ICE | AB4, AA4, AB3, Y5 | Internal Pull-down. |
| SCANEN, SCANMODE, IDDTN, CLKMODE_0, CLKMODE_1, TESTACLK, TESTCLKEN | N22, E7, Y4, AA22, AC2, AB6, D7 | Internal Pull-down. |
| DIS_SCSI_FSN/, TESTHCLK, TN | AC4, AE2, C5 | Internal Pull-up. |
| DIS_PCI_FSN/ | A24 | Internal Pull-down. Pull up externally to enable correct operation of the PCI FSN. |
| ZCR_EN/, IOPD_GNT/ | N23, AC5 | Internal Pull-up. |

# Chapter 4
# PCI Host Register Description

This chapter describes the PCI host register space. This chapter consists of the following sections:

- Section 4.1, “PCI Configuration Space Register Description”
- Section 4.2, “PCI I/O Space and Memory Space Register Description”

The register map at the beginning of each register description provides the default bit settings for the register. Shading indicates a reserved bit or register. Do not access the reserved address areas.

There are two PCI functions on the LSI53C1030. Each PCI function has its own independent interrupt pin and its own PCI Address space. The PCI System Address space consists of three regions: Configuration Space, Memory Space, and I/O Space. PCI Configuration Space supports the identification, configuration, initialization and error management functions for the LSI53C1030 PCI devices.

PCI Memory Space [0] and Memory Space [1] form the PCI Memory Space. PCI Memory Space [0] provides normal system accesses to memory and PCI Memory Space [1] provides diagnostic memory accesses. PCI I/O Space provides normal system access to memory.

## 4.1 PCI Configuration Space Register Description

This section provides bit level descriptions of the PCI Configuration Space registers. Table 4.1 defines the PCI Configuration Space registers. A separate set of PCI Configuration Space registers exists for each PCI function.

The LSI53C1030 enables, orders, and locates the PCI extended capability register structures (Power Management, Messaged Signalled

Interrupts, and PCI-X) to optimize device performance. The LSI53C1030 does not hard code the location and order of the PCI extended capability structures. The address and location of the PCI extended capability structures are subject to change. To access a PCI extended capability structure, follow the pointers held in the Capability Pointer registers and identify the extended capability structure with the Capability ID register for the given structure.

**Table 4.1 LSI53C1030 PCI Configuration Space Address Map**

| 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 | Offset | Page |
|---|---|---|---|---|---|---|---|---|---|
| Device ID | | | | Vendor ID | | | | 0x00 | 4-3 |
| Status | | | | Command | | | | 0x04 | 4-3 |
| Class Code | | | | | | Revision ID | | 0x08 | 4-7 |
| Reserved | | Header Type | | Latency Timer | | Cache Line Size | | 0x0C | 4-7 |
| I/O Base Address | | | | | | | | 0x10 | 4-9 |
| Memory [0] Low | | | | | | | | 0x14 | 4-10 |
| Memory [0] High | | | | | | | | 0x18 | 4-10 |
| Memory [1] Low | | | | | | | | 0x1C | 4-11 |
| Memory [1] High | | | | | | | | 0x20 | 4-11 |
| Reserved | | | | | | | | 0x24 | – |
| | | | | | | | | 0x28 | – |
| Subsystem ID | | | | Subsystem Vendor ID | | | | 0x2C | 4-12 |
| Expansion ROM Base Address | | | | | | | | 0x30 | 4-14 |
| Reserved | | | | | | Capabilities Pointer | | 0x34 | 4-15 |
| | | | | | | | | 0x38 | – |
| Maximum Latency | | Minimum Grant | | Interrupt Pin | | Interrupt Line | | 0x3C | 4-16 |
| Reserved | | | | | | | | 0x40–0x7F | – |
| Power Management Capabilities | | | | PM Next Pointer | | PM Capability ID | | | 4-18 |
| PM Data | | PM BSE | | Power Management Control/Status | | | | | 4-19 |
| Reserved | | | | | | | | | – |
| Message Control | | | | MSI Next Pointer | | MSI Capability ID | | | 4-21 |
| Message Address | | | | | | | | | 4-23 |
| Message Upper Address | | | | | | | | | 4-23 |
| Reserved | | | | Message Data | | | | | 4-24 |
| | | | | | | | | | – |
| PCI-X Command | | | | PCI-X Next Pointer | | PCI-X Capability ID | | | 4-25 |
| PCI-X Status | | | | | | | | | 4-27 |
| Reserved | | | | | | | | | – |

## Register: 0x00–0x01
**Vendor ID**
**Read Only**

| 15 | | | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vendor ID | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Vendor ID** **[15:0]**
This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

## Register: 0x02–0x03
**Device ID**
**Read Only**

| 15 | | | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device ID | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**Device ID** **[15:0]**
This 16-bit register identifies the particular device. The default Device ID for the LSI53C1030 is 0x0030.

## Register: 0x04–0x05
**Command**
**Read/Write**

| 15 | | | | | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Command | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Command register provides coarse control over the PCI function's ability to generate and respond to PCI cycles. Writing a zero to this register logically disconnects the LSI53C1030 PCI function from the PCI bus for all accesses except configuration accesses.

**Reserved** **[15:9]**
This field is reserved.

**SERR/ Enable** **8**
Setting this bit enables the LSI53C1030 to activate the SERR/ driver. Clearing this bit disables the SERR/ driver.

**Reserved** **7**
This bit is reserved.

**Enable Parity Error Response** **6**
Setting this bit enables the LSI53C1030 PCI function to detect parity errors on the PCI bus and report these errors to the system. Clearing this bit causes the LSI53C1030 PCI function to set the Detected Parity Error bit, bit 15 in the PCI Status register, but not assert PERR/ when the PCI function detects a parity error. This bit only affects parity checking. The PCI function always generates parity for the PCI bus.

**Reserved** **5**
This bit is reserved.

**Write and Invalidate Enable** **4**
Setting this bit enables the PCI function to generate write and invalidate commands on the PCI bus when operating in the conventional PCI mode.

**Reserved** **3**
This bit is reserved.

**Enable Bus Mastering** **2**
Setting this bit allows the PCI function to behave as a PCI bus master. Clearing this bit disables the PCI function from generating PCI bus master accesses.

**Enable Memory Space** **1**
This bit controls the ability of the PCI function to respond to Memory Space accesses. Setting this bit allows the LSI53C1030 to respond to Memory Space accesses at the address range specified by the Memory [0] Low, Memory [0] High, Memory [1] Low, Memory [1] High, and Expansion ROM Base Address registers. Clearing this bit disables the PCI function's response to PCI Memory Space accesses.

**Enable I/O Space** **0**
This bit controls the LSI53C1030 PCI function's response to I/O Space accesses. Setting this bit enables the PCI

function to respond to I/O Space accesses at the address range the PCI Configuration Space I/O Base Address register specifies. Clearing this bit disables the PCI function's response to I/O Space accesses.

## Register: 0x06–0x07

**Status**
**Read/Write**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Status | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Reads to this register behave normally. To clear a bit location that is currently set, write the bit to one (1). For example, to clear bit 15 when it is set, without affecting any other bits, write 0x8000 to the register.

**Detected Parity Error (from Slave) 15**
This bit is set per the *PCI Local Bus Specification, Revision 2.2*, and *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*.

**Signalled System Error 14**
The LSI53C1030 PCI function sets this bit when asserting the SERR/ signal.

**Received Master Abort (from Master) 13**
A master device sets this bit when a Master Abort command terminates its transaction (except for Special Cycle).

**Received Target Abort (from Master) 12**
A master device sets this bit when a Target Abort command terminates its transaction.

**Reserved 11**
This bit is reserved.

**DEVSEL/ Timing [10:9]**
These two read only bits encode the timing of DEVSEL/ and indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C1030 only

supports medium DEVSEL/ timing. The possible timing values are:

| | |
|---|---|
| 0b00 | Fast |
| 0b01 | Medium |
| 0b10 | Slow |
| 0b11 | Reserved |

**Data Parity Error Reported** **8**
This bit is set per the *PCI Local Bus Specification, Revision 2.2*, and *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*. Refer to bit 0 of the PCI-X Command register for more information.

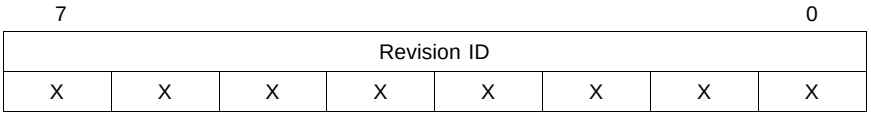
**Reserved** **[7:6]**
This field is reserved.

**66 MHz Capable** **5**
The MAD[13] Power-On Sense pin controls this bit. Allowing the internal pull-down to pull MAD[13] LOW sets this bit and indicates to the host system that the LSI53C1030 PCI function is capable of operating at 66 MHz. Pulling MAD[13] HIGH clears this bit and indicates to the host system that the LSI53C1030 PCI function is not configured to operate at 66 MHz. Refer to Section 3.10, "Power-On Sense Pins Description," for more information.

**New Capabilities** **4**
The LSI53C1030 PCI function sets this read only bit to indicate a list of PCI extended capabilities such as PCI Power Management, MSI, and PCI-X support.

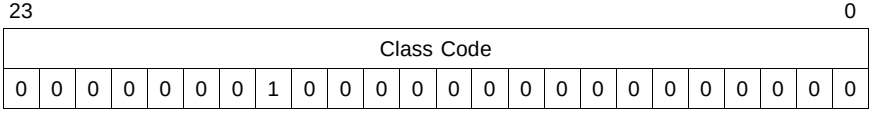
**Reserved** **[3:0]**
This field is reserved.

## Register: 0x08
**Revision ID**
**Read/Write**



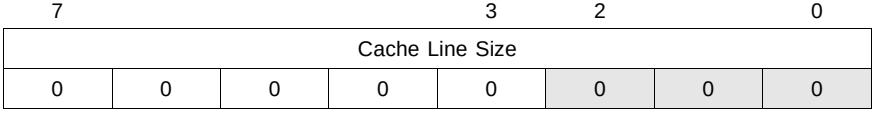

**Revision ID** **[7:0]**
This register indicates the current revision level of the device.

## Register: 0x09–0x0B
**Class Code**
**Read Only**




**Class Code** **[23:0]**
This 24-bit register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 0x010000, which identifies a SCSI controller.

## Register: 0x0C
**Cache Line Size**
**Read/Write**




**Cache Line Size** **[7:3]**
This register specifies the system cache line size in units of 32-bit words. In the conventional PCI mode, the LSI53C1030 PCI function uses this register to determine whether to use Write and Invalidate or Write commands

for performing write cycles. Programming this register to a number other than a nonzero power of two disables the the use of the PCI performance commands to execute data transfers. The PCI function ignores this register when operating in the PCI-X mode.

**Reserved** **[2:0]**
This field is reserved.

## Register: 0x0D
**Latency Timer**
**Read/Write**

| 7 | | | 4 | 3 | | | 0 |
|---|---|---|---|---|---|---|---|
| Latency Timer | | | | | | | |
| 0 | X | 0 | 0 | 0 | 0 | 0 | 0 |

**Latency Timer** **[7:4]**
The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. If the LSI53C1030 initializes in the PCI mode, the default value of this register is 0x00. If the LSI53C1030 initializes in the PCI-X mode, the default value of this register is 0x40.

**Reserved** **[3:0]**
This field is reserved.

## Register: 0x0E
**Header Type**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Header Type | | | | | | | |
| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Header Type** **[7:0]**
This 8-bit register identifies the layout of bytes 0x10 through 0x3F in configuration space and also indicates if the device is a single function or multifunction PCI device. If the LSI53C1030 is configured as a multifunction PCI device, bit 7 is set. If the LSI53C1030 is configured as a single function PCI device, bit 7 is cleared.

## Register: 0x0F
**Reserved**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Reserved** **[7:0]**
This register is reserved.

## Register: 0x10–0x13
**I/O Base Address**
**Read/Write**

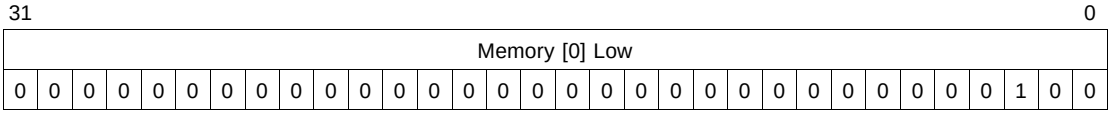
| 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I/O Base Address | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

The I/O Base Address register maps the operating register set into I/O Space. The LSI53C1030 requires 256 bytes of I/O Space for this base address register. Hardware sets bit 0 to 0b1. Bit 1 is reserved and returns 0b0 on all reads.

**I/O Base Address** **[31:2]**
This field contains the I/O Base address.

**Reserved** **[1:0]**
This field is reserved.

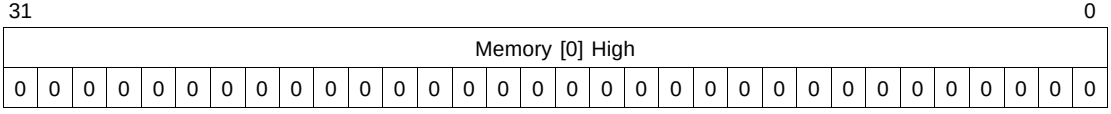
## Register: 0x14–0x17
**Memory [0] Low**
**Read/Write**




The Memory [0] Low register and the Memory [0] High register map SCSI operating registers into Memory Space [0]. This register contains the lower 32 bits of the Memory Space [0] base address. Hardware programs bits [9:0] to 0b0000000100, which indicates that the Memory Space [0] base address is 64 bits wide and that the memory data is not prefetchable. The LSI53C1030 requires 1024 bytes of memory space.

**Memory [0] Low** **[31:0]**
This field contains the Memory [0] Low address.

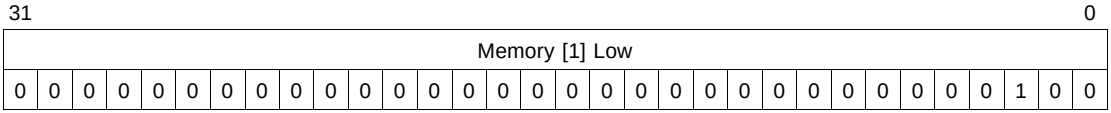
## Register: 0x18–0x1B
**Memory [0] High**
**Read/Write**




The Memory [0] High register and the Memory [0] Low register map SCSI operating registers into Memory Space [0]. This register contains the upper 32 bits of the Memory Space [0] base address. The LSI53C1030 requires 1024 bytes of memory space.

**Memory [0] High** **[31:0]**
This field contains the Memory [0] High address.

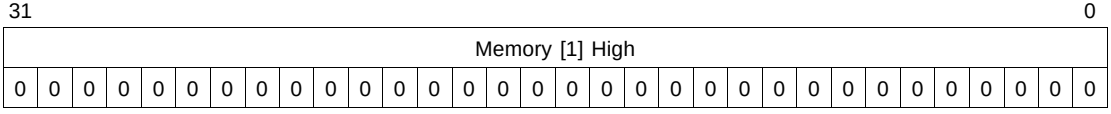
## Register: 0x1C–0x1F
**Memory [1] Low**
**Read/Write**




The Memory [1] Low register and the Memory [1] High register map the RAM into Memory Space [1]. This register contains the lower 32 bits of the Memory Space [1] base address. Hardware programs bits [12:0] to 0b0000000000100, which indicates that the Memory Space [1] base address is 64 bits wide and that the memory data is not prefetchable. The LSI53C1030 requires 64 Kbytes of memory for Memory Space [1].

**Memory [1] Low** **[31:0]**
This field contains the Memory [1] Low address.

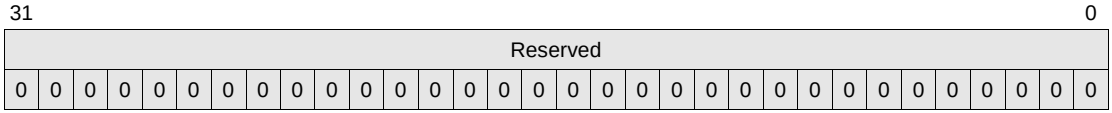
## Register: 0x20–0x23
**Memory [1] High**
**Read/Write**




The Memory [1] High register and the Memory [1] Low register map the RAM into Memory Space [1]. This register contains the upper 32 bits of the Memory Space [1] base address. The LSI53C1030 requires 64 Kbytes of memory for Memory Space [1].

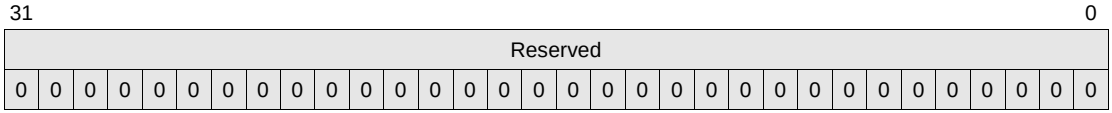
**Memory [1] High** **[31:0]**
This field contains the Memory [1] High address.

## Register: 0x24–0x27
**Reserved**



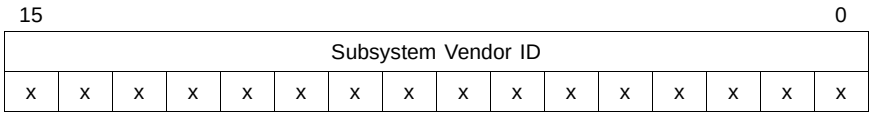

**Reserved** **[31:0]**
This register is reserved.

## Register: 0x28–0x2B
**Reserved**




**Reserved** **[31:0]**
This register is reserved.

## Register: 0x2C–0x2D
**Subsystem Vendor ID**
**Read Only**




**Subsystem Vendor ID** **[15:0]**
This 16-bit register uniquely identifies the vendor that manufactures the add-in board or subsystem where the LSI53C1030 resides. This register provides a mechanism for an add-in card vendor to distinguish their cards from another vendor's cards, even if the cards use the same PCI controller (and have the same Vendor ID and Device ID).

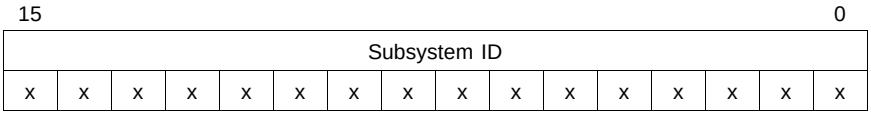
The external serial EEPROM can hold a vendor-specific, 16-bit value for this register, which the board designer must obtain from the PCI Special Interest Group (PCI-SIG). By default, an internal pull-down on the MAD[7] Power-On Sense pin enables the serial

EEPROM interface so that the LSI53C1030 can load this register from the serial EEPROM at power-up. If the download from the EEPROM fails, this register contains 0x0000.

If the board designer disables the EEPROM interface by pulling the MAD[7] Power-On Sense pin HIGH, this register returns a value of 0x1000. Refer to Section 3.10, "Power-On Sense Pins Description," page 3-21, for more information.

## Register: 0x2E–0x2F

**Subsystem ID**
**Read Only**




**Subsystem ID** **[15:0]**

This 16-bit register uniquely identifies the add-in board or subsystem where this PCI device resides. This register provides a mechanism for an add-in card vendor to distinguish their cards from one another even if the cards use the same PCI controller (and have the same Vendor ID and Device ID). The board designer can store a vendor specific, 16-bit value in an external serial EEPROM.

The ID Control Power-On Sense pins (MAD[11] for PCI Function [1]; MAD[10] for PCI Function [0]) and the serial EEPROM enable Power-On Sense pin (MAD[7]) control the value of this register. These pins have internal pull downs. Allowing MAD[7] to remain internally pulled down enables the serial EEPROM interface and permits the LSI53C1030 to load this register from the serial EEPROM at power up. Pulling MAD[7] HIGH disables the serial EEPROM interface. Allowing the ID Control pins to remain internally pulled LOW has no effect on this register. Pulling the ID Control pins HIGH sets bit [15] of this register for the given PCI function. Pulling the ID Control pins HIGH takes precedence over all other settings for bit [15].

Table 4.2 lists the configuration options for the Power-On Sense pins and settings for this register. If the serial

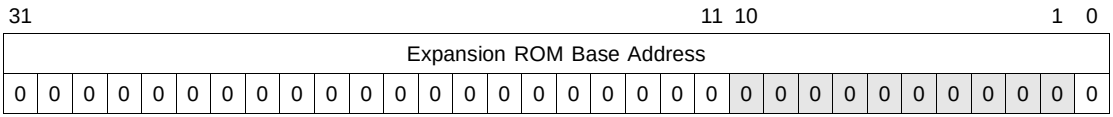
EEPROM interface is disabled and the ID Control pins are internally pulled LOW, this register contains 0x1000. If the serial EEPROM interface is disabled and the ID Control pins are pulled HIGH, this register contains 0x8000. If a download from the serial EEPROM fails and the ID Control pins are internally pulled LOW, this register contains 0x0000. If a download from the serial EEPROM fails and the ID Control pins are pulled HIGH, this register contains 0x8000. Refer to Section 3.10, "Power-On Sense Pins Description,", for additional information.

**Table 4.2 Subsystem ID Register Download Conditions and Values**

| MAD[7] State | MAD[11] or MAD[10] LOW | MAD[11] or MAD[10] HIGH |
|---|---|---|
| **MAD[7] LOW** | Subsystem ID = 0xXXXX<br>Bits [15:0] are downloaded.[1] (Default) | Subsystem ID = 0b1XXXXXXXXXXXXXXX<br>Bits [14:0] are downloaded with Bit [15] set.[2] |
| **MAD[7] HIGH** | Subsystem ID register = 0x1000. | Subsystem ID = 0x8000. |

1. The Subsystem ID register returns 0x0000 if the serial EEPROM download fails.
2. The Subsystem ID register returns 0x8000 if the serial EEPROM download fails.

## Register: 0x30–0x33
### Expansion ROM Base Address
### Read/Write




This four-byte register contains the base address and size information for the expansion ROM.

**Expansion ROM Base Address [31:11]**
These bits correspond to the upper 21 bits of the expansion ROM base address. The host system detects the size of the external memory by first writing 0xFFFFFFFF to this register and then reading the register back. The LSI53C1030 responds with zeros in all don't care locations. The least significant one (1) that remains represents the binary version of the external memory size. For example, to indicate an external memory size of 32

Kbytes, this register returns ones in the upper 17 bits when written with 0xFFFFFFFF and read back.

**Reserved** **[10:1]**
This field is reserved.

**Expansion ROM Enable** **0**
This bit controls if the device accepts accesses to its expansion ROM. Setting this bit enables address decoding. Depending on the system configuration, the device can optionally use an expansion ROM. Note that to access the expansion ROM, the user must also set bit 1 in the PCI Command register.

## Register: 0x34
**Capabilities Pointer**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Capabilities Pointer | | | | | | | |
| X | X | X | X | X | X | X | X |

**Capabilities Pointer** **[7:0]**
This register indicates the location of the first extended capabilities register in PCI Configuration Space. The value of this register varies according to system configuration.

## Register: 0x35–0x37
**Reserved**

| 23 | | | | | | | | | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Reserved** **[23:0]**
This register is reserved.

## Register: 0x38–0x3B
**Reserved**

| 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Reserved** **[31:0]**
This register is reserved.

## Register: 0x3C
**Interrupt Line**
**Read/Write**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Interrupt Line | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Interrupt Line** **[7:0]**
This register communicates interrupt line routing information. Power-On-Self-Test (POST) software writes the routing information into this register as it configures the system. This register indicates the system interrupt controller input to which this PCI function's interrupt pin connects. System architecture determines the values in this register.

## Register: 0x3D
**Interrupt Pin**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Function [0] Interrupt Pin | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Function [1] Interrupt Pin | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Interrupt Pin** **[7:0]**
The encoding of this read only register is unique to each function on the LSI53C1030. It indicates which interrupt pin the function uses. The value for Function [0] is 0x01,

which indicates that Function [0] presents interrupts on the INTA/ or ALT_INTA pins. The value for Function [1] is 0x02, which indicates that Function [1] presents interrupts on the INTB/ or ALT_INTB/ pins. The Interrupt Request Routing Mode bits, bits [9:8] in the Host Interrupt Mask register, determine if the function presents interrupts on INTx/, ALT_INTx/, or both.

## Register: 0x3E

**Minimum Grant**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Minimum Grant | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**Min_Gnt** **[7:0]**

This register specifies the desired settings for the latency timer values in units of 0.25 µs. This register specifies how long of a burst period the device needs. The LSI53C1030 sets this register to 0x10, indicating a burst period of 4.0 µs.

## Register: 0x3F

**Maximum Latency**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Maximum Latency | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Max_Lat** **[7:0]**

This register specifies the desired settings for the latency timer values in units of 0.25 µs. Max_Lat specifies how often the device needs to gain access to the PCI bus. The LSI53C1030 SCSI function sets this register to 0x06 since it requires the PCI bus every 1.5 µs to maintain a data transfer rate of 320 Mbytes/s.

## Register: 0xXX

**Power Management Capability ID**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Power Management Capability ID | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Power Management Capability ID** **[7:0]**
This register indicates the type of the current data structure. It is set to 0x01 to indicate the Power Management Data Structure.

## Register: 0xXX

**Power Management Next Pointer**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Power Management Next Pointer | | | | | | | |
| X | X | X | X | X | X | X | X |

**Power Management Next Pointer** **[7:0]**
This register contains the pointer to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

## Register: 0xXX

**Power Management Capabilities**
**Read Only**

| 15 | | | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Management Capabilities | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**PME_Support** **[15:11]**
These bits define the power management states in which the device asserts the Power Management Event (PME) pin. The LSI53C1030 clears these bits since the LSI53C1030 does not provide a PME signal.

**D2_Support** **10**
The PCI function sets this bit since the LSI53C1030 supports power management state D2.

**D1_Support** **9**
The PCI function sets this bit since the LSI53C1030 supports power management state D1.

**Aux_Current** **[8:6]**
The PCI function clears this field since the LSI53C1030 does not support Aux_Current.

**Device Specific Initialization** **5**
The PCI function clears this bit since no special initialization is required before a generic class device driver can use it.

**Reserved** **4**
This bit is reserved.

**PME Clock** **3**
The LSI53C1030 clears this bit since the chip does not provide a PME pin.

**Version** **[2:0]**
The PCI function programs these bits to 0b010 to indicate that the LSI53C1030 complies with the *PCI Power Management Interface Specification, Revision 1.1*.

## Register: 0xXX

**Power Management Control/Status**
**Read/Write**

| 15 | 14 | 13 | | | | 9 | 8 | 7 | | | | | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Management Control/Status | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PME_Status** **15**
The PCI function clears this bit since the LSI53C1030 does not support PME signal generation from $D3_{cold}$.

**Data_Scale** **[14:13]**
The PCI function clears these bits since the LSI53C1030 does not support the Power Management Data register.

**Data_Select** **[12:9]**
The PCI function clears these bits since the LSI53C1030 does not support the Power Management Data register.

**PME_Enable** **8**
The PCI function clears this bit since the LSI53C1030 does not provide a PME signal and disables PME assertion.

**Reserved** **[7:2]**
This field is reserved.

**Power State** **[1:0]**
These bits determine the current power state of the LSI53C1030. Power states are:

| | |
|---|---|
| 0b00 | D0 |
| 0b01 | D1 |
| 0b10 | D2 |
| 0b11 | $D3_{hot}$ |

## Register: 0xXX

**Power Management Bridge Support Extensions**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Power Management Bridge Support Extensions | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Power Management Bridge Support Extensions [7:0]**
This register indicates PCI Bridge specific functionality. The LSI53C1030 always returns 0x00 in this register.

## Register: 0xXX
**Power Management Data**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| Power Management Data | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Power Management Data** **[7:0]**
This register provides an optional mechanism for the PCI function to report state-dependent operating data. The LSI53C1030 always returns 0x00 in this register.

## Register: 0xXX
**MSI Capability ID**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| MSI Capability ID | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**MSI Capability ID** **[7:0]**
This register indicates the type of the current data structure. This register always returns 0x05, indicating Message Signalled Interrupts (MSI).

## Register: 0xXX
**MSI Next Pointer**
**Read Only**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| MSI Next Pointer | | | | | | | |
| X | X | X | X | X | X | X | X |

**MSI Next Pointer** **[7:0]**
This register points to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

## Register: 0xXX
### Message Control
### Read/Write

| 15 | | | | | | | 8 | 7 | 6 | | 4 | 3 | | | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Message Control | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Reserved** **[15:8]**
This field is reserved.

**64-bit Address Capable** **7**
The PCI function sets this read only bit to indicate support of a 64-bit message address.

**Multiple Message Enable** **[6:4]**
These read/write bits indicate the number of messages that the host allocates to the LSI53C1030. The host system software allocates all or a subset of the requested messages by writing to this field. The number of allocated request messages must align to a power of two. Table 4.3 provides the bit encoding of this field.

**Table 4.3 Multiple Message Enable Field Bit Encoding**

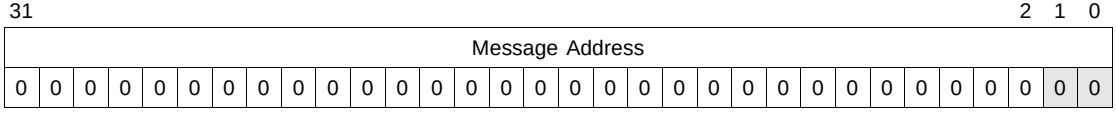
| Bits [6:4] Encoding | Number of Allocated Messages |
|---|---|
| 0b000 | 1 |
| 0b001 | 2 |
| 0b010 | 4 |
| 0b011 | 8 |
| 0b100 | 16 |
| 0b101 | 32 |
| 0b110 | Reserved |
| 0b111 | Reserved |

**Multiple Message Capable** **[3:1]**
These read only bits indicate the number of messages that the LSI53C1030 requests from the host. The host system software reads this field to determine the number

of requested messages. The number of requested messages must align to a power of two. The LSI53C1030 sets this field to 0b000 to request one message. All other encodings of this field are reserved.

**MSI Enable** **0**
System software sets this bit to enable MSI. Setting this bit enables the device to use MSI to interrupt the host and request service. Setting this bit also prohibits the device from using the INTx/ or ALT_INTx/ pins to request service from the host. Setting this bit to mask interrupts on the INTx/ or ALT_INTx/ pins is a violation of the PCI specification.

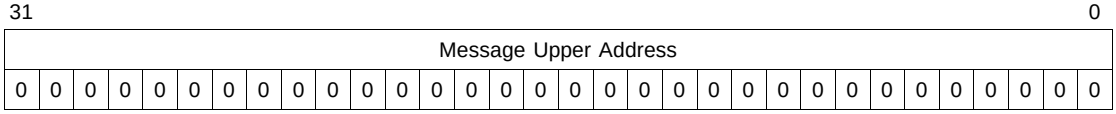
## Register: 0xXX
**Message Address**
**Read/Write**




**Message Address** **[31:2]**
This register contains message address bits [31:2] for the MSI memory write transaction. The host system specifies and Dword aligns the message address. During the address phase, the LSI53C1030 drives Message Address[1:0] to 0b00.

**Reserved** **[1:0]**
This field is reserved.

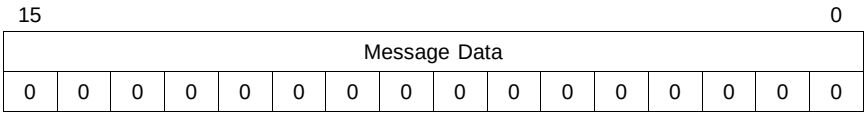
## Register: 0xXX
**Message Upper Address**
**Read/Write**




**Message Upper Address** **[31:0]**
The LSI53C1030 supports 64-bit MSI. This register contains the upper 32 bits of the 64-bit message address,

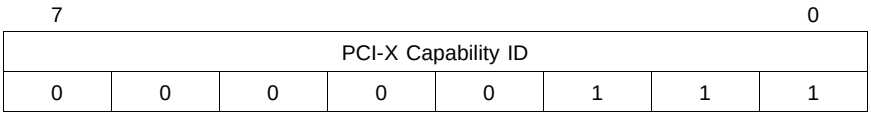
which the system specifies. The host system software can program this register to 0x0000 to force the PCI function to generate 32-bit message addresses.

## Register: 0xXX
**Message Data**
**Read/Write**




**Message Data** **[15:0]**
System software initializes this register by writing to it. The LSI53C1030 sends an interrupt message by writing a Dword to the address held in the Message Address and Message Upper Address registers. This register forms bits [15:0] of the Dword message that the PCI function passes to the host. The PCI function drives bits [31:16] of this message to 0x0000.

## Register: 0xXX
**PCI-X Capability ID**
**Read Only**




**PCI-X Capability ID** **[7:0]**
This register indicates the type of the current data structure. This register returns 0x07, indicating the PCI-X Data Structure.

## Register: 0xXX
### PCI-X Next Pointer
### Read Only

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| PCI-X Next Pointer | | | | | | | |
| X | X | X | X | X | X | X | X |

**PCI-X Next Capabilities Pointer** **[7:0]**
This register points to the next item in the device's capabilities list. The value of this register varies according to system configuration.

## Register: 0xXX
### PCI-X Command
### Read/Write

| 15 | | | | | | | | 7 | 6 | | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCI-X Command | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Reserved** **[15:7]**
This field is reserved.

**Maximum Outstanding Split Transactions** **[6:4]**
These bits indicate the maximum number of split transactions the LSI53C1030 can have outstanding at one time. The LSI53C1030 uses the most recent value of this register each time it prepares a new sequence. Note that if the LSI53C1030 prepares a sequence before the setting of this field changes, the PCI function initiates the prepared sequence with the previous setting. Table 4.4 provides the bit encodings for this field.

**Table 4.4 Maximum Outstanding Split Transactions**

| Bits [6:4] Encoding | Maximum Outstanding Split Transactions |
|---|---|
| 0b000 | 1 |
| 0b001 | 2 |

**Table 4.4 Maximum Outstanding Split Transactions (Cont.)**

| Bits [6:4] Encoding | Maximum Outstanding Split Transactions |
|---|---|
| 0b010 | 3 |
| 0b011 | 4 |
| 0b100 | 8 |
| 0b101 | Reserved |
| 0b110 | Reserved |
| 0b111 | Reserved |

**Maximum Memory Read Byte Count** **[3:2]**
These bits indicate the maximum byte count the LSI53C1030 uses when initiating a sequence with one of the burst memory read commands. Table 4.5 provides the bit encodings for this field.

**Table 4.5 Maximum Memory Read Count**

| Bits [3:2] Encoding | Maximum Memory Read Byte Count |
|---|---|
| 0b00 | 512 |
| 0b01 | 1024 |
| 0b10 | 2048 |
| 0b11 | Reserved |

**Reserved** **1**
This bit is reserved.

**Data Parity Error Recovery Enable** **0**
The host device driver sets this bit to allow the LSI53C1030 to attempt to recover from data parity errors. If the user clears this bit and the LSI53C1030 is operating in the PCI-X mode, the LSI53C1030 asserts SERR/ whenever the Master Data Parity Error bit in the PCI Status register is set.

## Register: 0xXX
### PCI-X Status
### Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 8 | 7 | 3 | 2 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCI-X Status | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

**Reserved** **[31:30]**
This field is reserved.

**Received Split Completion Error Message** **29**
The LSI53C1030 sets this bit upon receipt of a split completion message if the split completion error attribute bit is set. Write a one (1) to this bit to clear it.

**Designed Maximum Cumulative Read Size** **[28:26]**
These read only bits indicate a number greater than or equal to the maximum cumulative size of all outstanding burst memory read transactions for the LSI53C1030 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1030 reports 0b001 in this field to indicate a designed maximum cumulative read size of 2 Kbytes.

**Designed Maximum Outstanding Split Transactions** **[25:23]**
These read only bits indicate a number greater than or equal to the maximum number of all outstanding split transactions for the LSI53C1030 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1030 reports 0b100 in this field to indicate that the designed maximum number of outstanding split transactions is eight.

**Designed Maximum Memory Read Byte Count** **[22:21]**
These read only bits indicate a number greater than or equal to the maximum byte count for the LSI53C1030 device. The PCI function uses this count to initiate a sequence with one of the burst memory read commands. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1030 reports 0b10 in this field to indicate that the designed maximum memory read bytes count is 2048.

**Device Complexity** **20**
The PCI function clears this read only bit to indicate that the LSI53C1030 is a simple device.

**Unexpected Split Completion** **19**
The PCI function sets this read only bit when it receives an unexpected split completion. Once set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

**Split Completion Discarded** **18**
The PCI function sets this read only bit when it discards a split completion. Once set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

**133 MHz Capable** **17**
The MAD[15] Power-On Sense pin controls this read only bit. Allowing the internal pull-downs to pull MAD[15] LOW sets this bit and enables 133 MHz operation of the PCI bus. Pulling MAD[15] HIGH clears this bit and disables 133 MHz operation of the PCI bus. Refer to Section 3.10, "Power-On Sense Pins Description," for more information concerning the Power-On Sense pins.

**64-bit Device** **16**
The MAD[14] Power-On Sense pin controls this read only bit. Allowing the internal pull-downs to pull MAD[14] LOW sets this bit and indicates a 64-bit PCI Address/Data bus. Pulling MAD[14] HIGH clears this bit and indicates a 32-bit PCI Address/Data bus. If using the LSI53C1030 on an add-in card, this bit must indicate the size of the card's PCI Address/Data bus. Refer to Section 3.10, "Power-On Sense Pins Description," for more information concerning the Power-On Sense pins.

**Bus Number** **[15:8]**
These read only bits indicate the number of the LSI53C1030 bus segment. This PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

**Device Number** **[7:3]**
These read only bits indicate the device number of the LSI53C1030. This PCI function uses this number as part

of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

**Function Number** **[2:0]**
These read only bits indicate the number in the Function Number field (AD[10:8]) of a Type 0 PCI configuration transaction. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

## 4.2 PCI I/O Space and Memory Space Register Description

This section describes the host interface registers in the PCI I/O Space and PCI Memory Space. These address spaces contain the Fusion-MPT interface register set. PCI Memory Space [0] and PCI Memory Space [1] form the PCI Memory Space. PCI Memory [0] supports normal memory accesses while PCI Memory Space [1] supports diagnostic memory accesses. For all registers except the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers, access the address offset through either PCI I/O Space or PCI Memory Space [0]. Access to the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers is only through PCI I/O Space.

When the LSI53C1030 operates as a multifunction PCI device, the entire PCI Memory and PCI I/O Space register sets are visible to both PCI functions. When the LSI53C1030 operates as a single function PCI device, only PCI Function [0] register sets are accessible. Refer to Section 3.10, “Power-On Sense Pins Description,” for information on how to configure the LSI53C1030 as a single or multifunction PCI device.

Table 4.6 defines the PCI I/O Space address map.

### Table 4.6 PCI I/O Space Address Map

| 31 0 | Offset | Page |
|---|---|---|
| System Doorbell | 0x0000 | 4-31 |
| Write Sequence | 0x0004 | 4-31 |
| Host Diagnostic | 0x0008 | 4-32 |
| Test Base Address | 0x000C | 4-34 |
| Diagnostic Read/Write Data | 0x0010 | 4-34 |
| Diagnostic Read/Write Address | 0x0014 | 4-35 |
| Reserved | 0x0018–0x002F | – |
| Host Interrupt Status | 0x0030 | 4-36 |
| Host Interrupt Mask | 0x0034 | 4-37 |
| Reserved | 0x0038–0x003F | – |
| Request FIFO | 0x0040 | 4-38 |
| Reply FIFO | 0x0044 | 4-38 |
| Reserved | 0x0048–0x007F | – |

Table 4.7 defines the PCI Memory Space [0] address map.

### Table 4.7 PCI Memory [0] Address Map

| 31 0 | Offset | Page |
|---|---|---|
| System Doorbell | 0x0000 | 4-31 |
| Write Sequence | 0x0004 | 4-31 |
| Host Diagnostic | 0x0008 | 4-32 |
| Test Base Address | 0x000C | 4-34 |
| Reserved | 0x0010–0x002F | – |
| Host Interrupt Status | 0x0030 | 4-36 |
| Host Interrupt Mask | 0x0034 | 4-37 |
| Reserved | 0x0038–0x003F | – |
| Request FIFO | 0x0040 | 4-38 |
| Reply FIFO | 0x0044 | 4-38 |
| Reserved | 0x0048–0x007F | – |
| Shared Memory | 0x0080–<br>0x(Sizeof(Mem0)–1) | – |

Table 4.8 defines the PCI Memory Space [1] address map.

### Table 4.8 PCI Memory [1] Address Map

| 31 0 | |
|---|---|
| Diagnostic Memory | 0x0000–<br>0x(Sizeof(Mem1)–1) |

A bit level description of the PCI Memory and PCI I/O Spaces follows.

## Register: 0x00
**System Doorbell**
**Read/Write**

| 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| System Doorbell | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The System Doorbell register is a simple message passing mechanism that allows the system to pass single word messages to the embedded IOP processor and vice-versa. There is a unique system doorbell for each PCI function.

When a host system PCI master writes to the Host Registers->Doorbell register, the LSI53C1030 generates a maskable interrupt to the IOP. The value written by the host system is available for the IOP to read in the System Interface Registers->Doorbell register. The IOP clears the interrupt status after reading the value.

Conversely, when the IOP processor writes to the System Interface Registers->Doorbell register, the LSI53C1030 generates a maskable interrupt to the PCI system. The host system can read the value written by the IOP in the Host Registers->Doorbell register. The host system clears the interrupt status bit and interrupt pin by writing any value to the Host Registers->Interrupt Status register.

**Host Doorbell Value** **[31:0]**
During a write, this register contains the doorbell value that the host system passes to the IOP. During a read, this register contains the doorbell value that the IOP passes to the host system.

## Register: 0x04
**Write Sequence**
**Read/Write**

| 31 | | | | | | | | | | | | | | | | | | | | | | | | | | 4 | 3 | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write Sequence | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

The Write Sequence register provides a protection mechanism against inadvertent writes to the Host Diagnostic register. There is one Write

Sequence register that is visible to both PCI functions. The two PCI functions physically share this register.

**Reserved** **[31:4]**
This field is reserved.

**Write I/O Key** **[3:0]**
To enable write access to the Diagnostic Read/Write Data, Diagnostic Read/Write Address, and Host Diagnostic registers, perform five data-specific writes to the Write I/O Key. Writing an incorrect value to the Write I/O Key invalidates the key sequence and the host must rewrite the entire sequence. The Write I/O Key sequence is: 0x0004, 0x000B, 0x0002, 0x0007, and 0x000D. To disable write access to the Diagnostic Read/Write Data, Diagnostic Read/Write Address, and Host Diagnostic registers, perform a write of any value, except the Write I/O Key sequence, to the Write Sequence register. The Diagnostic Write Enable bit, bit 7 in the Host Diagnostic register, indicates the write access status.

## Register: 0x08
**Host Diagnostic**
**Read/Write**

| 31 | | | | | | | | | | | | | | | | | | | | | | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Host Diagnostic | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | X | 0 |

The Host Diagnostic register contains diagnostic controls and status information. There is one Host Diagnostic register that is visible to both PCI functions. The two PCI functions physically share this register. However, the Reset History bit operates independently for each PCI function. This register can only be written when bit 7 of this register is set.

**Reserved** **[31:8]**
This field is reserved.

**Diagnostic Write Enable** **7**
The LSI53C1030 sets this read only bit when the host writes the correct Write I/O Key to the Write Sequence register. The LSI53C1030 clears this bit when the host

writes a value other than the Write I/O Key to the Write Sequence register.

**Flash Bad Signature** **6**
The LSI53C1030 sets this bit if the IOP ARM966E-S processor encounters a bad Flash signature when booting from Flash ROM. The LSI53C1030 also sets the DisARM bit (bit 1 in this register) to hold the IOP ARM processor in a reset state. The LSI53C1030 maintains this state until the PCI host clears both the Flash Bad Signature and DisARM bits.

**Reset History** **5**
The LSI53C1030 sets this bit if it experiences a Power On Reset (POR), PCI Reset, or TestReset/. A host driver can clear this bit to help coordinate recovery between multiple driver instances in a multifunction PCI implementation.

**Diagnostic Read/Write Enable** 4
Setting this bit enables access to the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers.

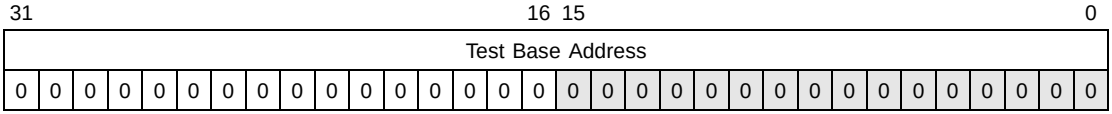
**TTL Interrupt** **3**
Setting this bit configures PCI INTA/ as a TTL output. Clearing this bit configures PCI INTA/ as an open-drain output. Use this bit for test purposes only.

**Reset Adapter** **2**
Setting this write only bit causes a hard reset within the LSI53C1030. The bit self-clears after eight PCI clock periods. After deasserting this bit, the IOP ARM processor executes from its default reset vector.

**DisARM** **1**
Setting this bit disables the ARM processor.

**Diagnostic Memory Enable** **0**
Setting this bit enables diagnostic memory accesses through PCI Memory Space [1]. Clearing this bit disables diagnostic memory accesses to PCI Memory Space [1] and returns 0xFFFF on reads.

## Register: 0x0C
**Test Base Address**
**Read/Write**

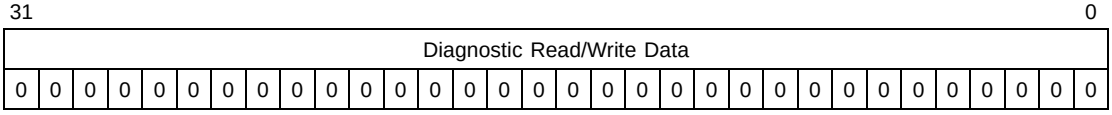



The Test Base Address register specifies the base address for Memory Space [1] accesses. There is one Test Base Address register that is visible to both PCI functions. The two PCI functions physically share this register. Because Diagnostic Memory is visible only to PCI Function [0], PCI Function [1] cannot write to this register.

**Test Base Address** **[31:16]**
The number of significant bits is determined by the size of the PCI Memory Space [1] in the serial EEPROM.

**Reserved** **[15:0]**
This field is reserved.

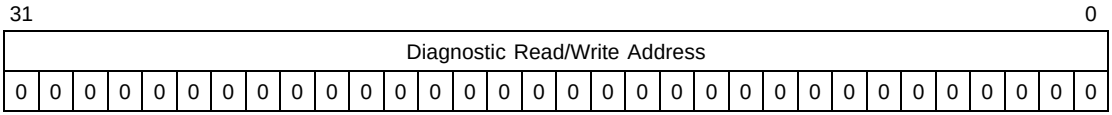
## Register: 0x10
**Diagnostic Read/Write Data**
**Read/Write**




This register reads or writes Dword locations on the LSI53C1030 internal bus. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write I/O Key to the Write Sequence register and setting bit 4, the Diagnostic Write Enable bit, of the Host Diagnostic register. A write of any value other than the correct Write I/O Key to the Write Sequence register disables write access to this register. There is one Diagnostic Read/Write Data register that is visible to both PCI functions. The two PCI functions physically share this register.

**Diagnostic Read/Write Data** **[31:0]**
Using this register, the LSI53C1030 reads/writes data at the address that the Diagnostic Read/Write Address register specifies.

## Register: 0x14
### Diagnostic Read/Write Address
### Read/Write




The Diagnostic Read/Write Address register specifies a Dword location on the internal bus. The address increments by a Dword whenever the host system accesses the Diagnostic Read/Write Address register. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write I/O Key to the Write Sequence register and setting bit 4, the Diagnostic Write Enable bit, of the Host Diagnostic register. A write of any value other than the correct Write I/O Key to the Write Sequence register disables write access to this register. There is one Diagnostic Read/Write Address register that is visible to both PCI functions. The two PCI functions physically share this register.

**Diagnostic Read/Write Address** **[31:0]**
This register holds the address that the Diagnostic Read/Write Data register writes data to or reads data from.

## Register: 0x30
### Host Interrupt Status
### Read/Write

| 31 | 30 | | | | | | | | | | | | | | | | | | | | | | | | | | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Host Interrupt Status | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | X | X | 0 | |

The Host Interrupt Status register provides read only interrupt status information to the PCI Host. A write to this register of any value clears the associated System Doorbell interrupt. There is a unique Host Interrupt Status register for each PCI function.

**IOP Doorbell Status** **31**
The LSI53C1030 sets this bit when the IOP receives a message from the system doorbell but has yet to process it. The IOP processes the System Doorbell message by clearing the corresponding system request interrupt.

**Reserved** **[30:4]**
This field is reserved.

**Reply Interrupt** **3**
The LSI53C1030 sets this bit when the Reply Post FIFO is not empty. The LSI53C1030 generates a PCI interrupt when this bit is set and the corresponding mask bit in the Host Interrupt Mask register is cleared.

**Reserved** **[2:1]**
This field is reserved.

**System Doorbell Interrupt** **0**
The LSI53C1030 sets this bit when the IOP writes a value to the System Doorbell. The host can clear this bit by writing any value to this register. The LSI53C1030 generates a PCI interrupt when this bit is set and the corresponding mask bit in the Host Interrupt Mask register is cleared.

## Register: 0x34
### Host Interrupt Mask
### Read/Write

| 31 | | | | | | | | | | | | | | | | | | | | 10 | 9 | 8 | 7 | | | | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Host Interrupt Mask | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | X | X | X | X | 1 | X | X | 1 | |

The Host Interrupt Mask register masks and/or routes the interrupt conditions that the Host Interrupt Status register reports. There is a unique Host Interrupt Mask register for each PCI function.

**Reserved** **[31:10]**
This field is reserved.

**Interrupt Request Routing Mode** **[9:8]**
This field routes PCI interrupts to the INTx/ or ALT_INTx/ pins according to the bit encodings in Table 4.9. If the host system enables MSI, the LSI53C1030 does not signal PCI interrupts on the INTx/ or ALT_INTx/ pins.

**Table 4.9 Interrupt Signal Routing**

| Bits [9:8] Encodings | Interrupt Signal Routing |
|---|---|
| 0b00 | INTx/ and ALT_INTx/ |
| 0b01 | INTx/ only |
| 0b10 | ALT_INTx/ only |
| 0b11 | INTx/ only |

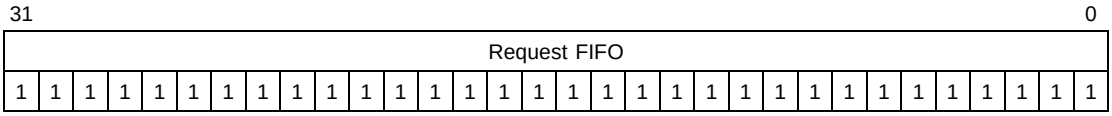
**Reserved** **[7:4]**
This field is reserved.

**Reply Interrupt Mask** **3**
Setting this bit masks reply interrupts and prevents the assertion of a PCI interrupt for all reply interrupt conditions.

**Reserved** **[2:1]**
This field is reserved.

**Doorbell Interrupt Mask** **0**
Setting this bit masks System Doorbell interrupts and prevents the assertion of a PCI interrupt for all System Doorbell interrupt conditions.

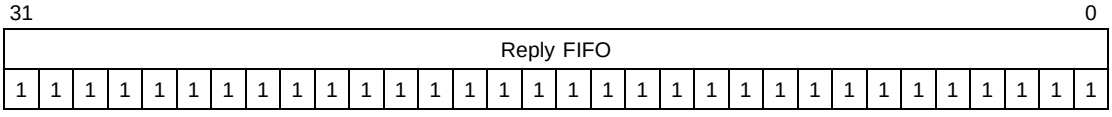
## Register: 0x40
**Request FIFO**
**Read/Write**




The Request FIFO provides Request Free Message Frame Addresses (MFAs) to the host system on reads and accepts Request Post MFAs from the host system on writes. There is one Request FIFO register that is visible to both PCI functions. The two PCI functions physically share this register.

**Request FIFO** **[31:0]**
For reads, the Request Free MFA is empty and this register contains 0xFFFFFFFF. For writes, the register contains the Request Post MFA.

## Register: 0x44
**Reply FIFO**
**Read/Write**




The Reply FIFO provides Reply Post MFAs to the host system on reads and accepts Reply Free MFAs from the host system on writes. There is a unique Reply FIFO register for each PCI function.

**Reply FIFO** **[31:0]**
For reads, the Request Free MFA is empty and this register contains 0xFFFFFFFF. For writes, the register contains the Reply Free MFA.

# Chapter 5
# Specifications

This chapter specifies the LSI53C1030 electrical and mechanical characteristics. It is divided into the following sections:

- Section 5.1, “DC Characteristics”
- Section 5.2, “TolerANT Technology Electrical Characteristics”
- Section 5.3, “AC Characteristics”
- Section 5.4, “External Memory Timing Diagrams”
- Section 5.5, “Package Drawings”

Please refer to the *PCI Local Bus Specification*, the *PCI-X Addendum to the PCI Local Bus Specification*, and the *SCSI Parallel Interface-4 Draft Specification* for PCI, PCI-X, and SCSI timings and timing diagrams. The LSI53C1030 timings conform to the timings these specifications provide.

## 5.1 DC Characteristics

This section of the manual describes the LSI53C1030 DC characteristics. Tables 5.1 through 5.11 give current and voltage specifications. Figures 5.1 and 5.2 are LVD transceiver schematics.

### Table 5.1 Absolute Maximum Stress Ratings[1]

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –40 | 125 | °C | – |
| $V_{DD\text{-}Core}$ | Supply voltage | –0.3 | 2.2 | V | – |
| $V_{DD\text{-}IO}$ | I/O Supply voltage | –0.3 | 3.9 | V | – |
| $V_{IN}$ | Input voltage | –0.5 | $V_{DD}$ + 0.5 | V | – |
| $I_{LP}$[2] | Latch-up current | ±150 | – | mA | $-2\ V < V_{PIN} < 8\ V$ |
| T[2] | Lead temperature | – | 125 | °C | – |
| ESD[2] | Electrostatic discharge | – | 2000 | V | MIL-STD 883C, Method 3015.7 |

1. Stresses beyond those listed above can damage the device. These are stress ratings only; functional operation of the device at or beyond these values is not implied.
2. SCSI pins only.

### Table 5.2 Operating Conditions[1]

| Symbol | Parameter | Min | Nominal | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD\text{-}Core}$ | Core and analog supply voltage | 1.71 | 1.80 | 1.89 | V | – |
| $V_{DD\text{-}IO}$ | I/O supply voltage | 2.97 | 3.30 | 3.63 | V | – |
| $I_{DD\text{-}Core}$ | Core and analog supply current (dynamic)[2] | – | 1.50 | 1.80 | A | – |
| $I_{DD\text{-}I/O}$ | I/O supply current (dynamic) | – | 0.50 | 1.00 | A | – |
| $T_j$ | Junction temperature | – | – | 115 | °C | – |
| $T_A$ | Operating free air | 0 | – | 70.0 | °C | – |
| $\theta_{JA}$ | Thermal resistance (junction to ambient air) | – | – | 15.0 | °C/W | 0 Linear Feet/Minute |

1. Conditions that exceed the operating limits can cause the device to function incorrectly.
2. Core and analog supply only.

The core voltage must come up before I/O voltage. The following equation must hold at all times: VDD_I/O ≤ (VDD_CORE + 2 V).

**Table 5.3 LVD Driver SCSI Signals[1]— SACK±, SATN±, SBSY±, SCD±, SD[15:0]±, SDP[1:0]±, SIO±, SMSG±, SREQ±, SRST±, SSEL±**

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_O+$ | Source (+) current | –6.5 | –13.5 | mA | Asserted state |
| $I_O–$ | Sink (–) current | 6.5 | 13.5 | mA | Asserted state |
| $I_O+$ | Source (+) current | 2.5 | 9.5 | mA | Negated state |
| $I_O–$ | Sink (–) current | –2.5 | –9.5 | mA | Negated state |
| $I_{OZ}$ | 3-state leakage | – | 20 | µA | – |

1. $V_{CM}$ = 0.7–1.8 V (Common Mode, nominal ~1.2 V), Rbias = 10.0 kΩ.

**Figure 5.1 LVD Driver**

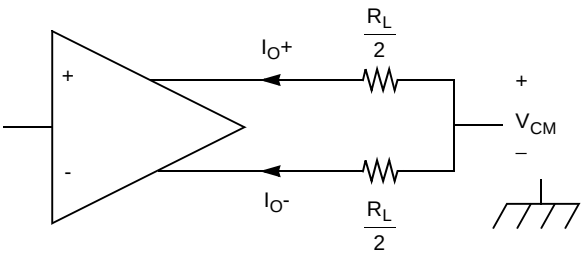



**Table 5.4 LVD Receiver SCSI Signals[1]— SACK±, SATN±, SBSY±, SCD±, SD[15:0]±, SDP[1:0]±, SIO±, SMSG±, SREQ±, SRST±, SSEL±**

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_I$ | LVD receiver voltage asserting | \|30\| | - | mV | Differential voltage |
| $V_I$ | LVD receiver voltage negating | | \|30\| | mV | Differential voltage |

1. $V_{CM}$ = 0.7–1.8 V (Common Mode Voltage, nominal ~1.2 V.)

**Figure 5.2 LVD Receiver**

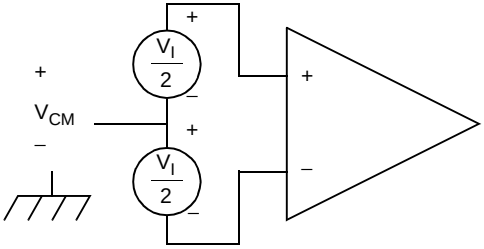



**Table 5.5 A_DIFFSENS and B_DIFFSENS SCSI Signals**

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | HVD sense voltage | 2.4 | 3.6 | V | Note 1 |
| $V_S$ | LVD sense voltage | 0.7 | 1.9 | V | Note 1 |
| $V_{IL}$ | SE sense voltage | VSS – 0.35 | 0.5 | V | Note 1 |
| $I_{OZ}$ | 3-state leakage | –10 | 10 | µA | $V_{PIN}$ = 0 V, 3.6 V |

1. $V_{IH}$, $V_{IL}$, and $V_s$ are specified in the SPI-4 draft specification.

**Table 5.6 Input Capacitance**

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $C_I$ | Input capacitance of input pads | – | 7 | pF | Guaranteed by design |
| $C_{IO}$ | Input capacitance of I/O pads | – | 15 | pF | Guaranteed by design |
| $C_{PCI}$ | Input capacitance of PCI pads | – | 8 | pF | Guaranteed by design |
| $C_{LVD}$ | Input capacitance of LVD pads | – | 8 | pF | 6.5 pf pad<br>1.5 pf package |

**Table 5.7 8 mA Bidirectional Signals — GPIO[7:0], MAD[15:0], MADP[1:0], SerialDATA**

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | 3.6 | V | – |
| $V_{IL}$ | Input low voltage | –0.3 | 0.8 | V | – |
| $V_{OH}$ | Output high voltage | 2.4 | VDD | V | –8 mA |
| $V_{OL}$ | Output low voltage | VSS | 0.4 | V | 8 mA |
| $I_{OZ}$ | 3-state leakage | –10 | 10 | µA | $V_{PIN}$ = 0 V, 5.25 V |
| $I_{PULL}$ | Pull up current | 25 | – | µA | – |

**Table 5.8 8 mA PCI Bidirectional Signals — ACK64/, AD[63:0], C_BE[7:0]/, DEVSEL/, FRAME/, IRDY/, PAR, PAR64, PERR/, REQ64/, SERR/, STOP/, TRDY/**

| Symbol | Parameters | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.5 VDD | PCI5VBIAS[1] | V | – |
| $V_{IL}$ | Input low voltage | –0.5 | 0.3 VDD | V | – |
| $V_{OH}$ | Output high voltage | 0.9 VDD | VDD | V | –500 µA |
| $V_{OL}$ | Output low voltage | VSS | 0.1 VDD | V | 1500 µA |
| $I_{OZ}$ | 3-state leakage | –10 | 10 | µA | $V_{PIN}$ = 0 V, 5.25 V |
| $I_{PULL-DOWN}$ | Pull-down current[2] | 25 | – | µA | – |

1. The maximum PCI input voltage depends upon the operating mode of the PCI bus, which PCI5VBIAS determines. The maximum input voltage in a 5 V PCI system is 5 V. The maximum input voltage in a 3.3 V PCI system is VDD. Refer to the signal description in Section 3.9, “Power and Ground Pins,” for more information concerning PCI5VBIAS.
2. Pull-down text does not apply to AD[31:0] and C_BE[3:0]/.

**Table 5.9 Input Signals[1] — CLK, CLKMODE_0, CLKMODE_1, DIS_PCI_FSN/, DIS_SCSI_FSN/, GNT/, IDDTN, IDSEL, IOPD_GNT/, PVT1, PVT2, SCANEN, SCANMODE, SCLK, TCK_CHIP, TCK_ICE, TESTACLK, TESTCLKEN, TESTHCLK, TDI_CHIP, TDI_ICE, TMS_CHIP, TMS_ICE, TN, TRST_ICE/, TST_RST/, ZCR_EN/**

| Symbol | Parameters | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | VDD + 0.5 | V | – |
| $V_{IL}$ | Input low voltage | –0.3 | 0.8 | V | – |
| $I_{IN}$ | 3-state leakage | –10 | 10 | µA | $V_{PIN}$ = 0 V, VDD + 0.5 V |
| $I_{PULL-UP}$ | Pull current | 25 | – | µA | – |

1. Do not place pulls on CLK, GNT/, IDSEL, RST/, and SCLK. The pull information given does not apply to these signals.

**Table 5.10 8 mA Output Signals[1] — ADSC/, ADV/, ALT_INTA/, ALT_INTB/, BWE[1:0]/, FLSHALE[1:0]/, FLSHCE/, INTA/, INTB/, MCLK, MOE/, PIPESTAT[2:0], RAMCE/, REQ/, RTCK_ICE, SerialCLK, SERR/, TDO_CHIP, TDO_ICE, TRACECLK, TRACEPKT[7:0], TRACESYNC**

| Symbol | Parameters | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | 2.4 | VDD | V | –8 mA |
| $V_{OL}$ | Output low voltage | VSS | 0.4 VDD | V | 8 mA |
| $I_{OZ}$ | 3-state leakage | –10 | 10 | µA | $V_{PIN}$ = 0 V, 3.6 V |
| $I_{PULL-UP}$ | Pull current | 25 | – | µA | – |

1. Do not place pulls on REQ/ and SERR/. The pull information given does not apply to these signals.

**Table 5.11 12 mA Output Signals — A_LED/, B_LED/, HB_LED/**

| Symbol | Parameters | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | 2.4 | VDD | V | –12 mA |
| $V_{OL}$ | Output low voltage | VSS | 0.4 VDD | V | 12 mA |
| $I_{OZ}$ | 3-state leakage | –10 | 10 | µA | $V_{PIN}$ = 0 V, 3.6 V |
| $I_{PULL-UP}$ | Pull current | 25 | – | µA | – |

## 5.2 TolerANT Technology Electrical Characteristics

The LSI53C1030 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators.

Table 5.12 provides electrical characteristics for SE SCSI signals. Figure 5.3 and Figure 5.4 provide the reference information for testing SCSI signals.

**Table 5.12 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]**

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$[2] | Output high voltage | 2.5 | 3.7 | V | $I_{OH}$ = 0 mA |
| $V_{OL}$ | Output low voltage | 0.0 | 0.5 | V | $I_{OL}$ = 48 mA |
| $V_{IH}$ | Input high voltage | 1.9 | 5.50 | V | Signal FALSE State |
| $V_{IL}$ | Input low voltage | –0.5 | 1.0 | V | Referenced to $V_{SS}$ Signal TRUE State |
| $V_{IK}$ | Input clamp voltage | – | –0.75 | V | $V_{pp}$ = Min; $I_1$ = –20 mA |
| $V_{TH}$ | Threshold, HIGH to LOW | 1.00 | – | V | – |
| $V_{TL}$ | Threshold, LOW to HIGH | – | 1.90 | V | – |
| $V_{TH}$–$V_{TL}$ | Hysteresis | 375 | – | mV | – |
| $I_{ih.hp}$ | Hot Plug High Level Current Peak | – | 1.5 | mA | Transient duration of 10% of peak equals 20 µs. This applies during physical insertion only. |
| $I_{OH2}$ | Output high current | 0 | 7 | mA | $V_{OH}$ = 2.2 V |
| $I_{OL}$ | Output low current | 48 | – | mA | $V_{OL}$ = 0.5 V |
| $I_{OSH2}$ | Short-circuit output high current | 48 | – | mA | Short to $V_{DD}$[3] |
| $I_{OSL}$ | Short-circuit output low current | 22 | – | mA | Short to $V_{SS}$ |

**Table 5.12 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1] (Cont.)**

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{LH}$ | Input high leakage | – | 20 | µA | $-0.5<V_{DD}<5.25$ $V_{PIN}$ = 2.7 V |
| $I_{LL}$ | Input low leakage | – | 20 | µA | $-0.5<V_{DD}<5.25$ $V_{PIN}$ = 0.5 V |
| $R_I$ | Input resistance | 20 | – | MΩ | Receivers disabled |
| $C_P$ | Capacitance per pin | – | 8 | pF | PQFP |
| dVH/dt | Slew rate LOW to HIGH | 110 | 540 | mV/ns | Figure 5.3 |
| dVL/dt | Slew rate HIGH to LOW | 110 | 540 | mV/ns | Figure 5.3 |
| $ESD_{HBM}$ | Electrostatic discharge (HBM) | 2 | – | kV | MIL-STD-883C; Method 3015-7; 100 pF at 1.5 kΩ |
| $ESD_{CDM}$ | Electrostatic discharge (CDM) | 0.5 | – | kV | ESD DS5.3.1-1996 |
| | Latch-up | 100 | – | mA | – |
| | Filter delay | 20 | 30 | ns | Figure 5.4 |
| | Ultra filter delay | 10 | 15 | ns | Figure 5.4 |
| | Ultra2 filter delay | 5 | 8 | ns | Figure 5.4 |
| | Extended filter delay | 40 | 60 | ns | Figure 5.4 |

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, and SACK/. SCSI SE mode only (minus pins).
3. Single pin only; irreversible damage can occur if sustained for longer than one second.

**Figure 5.3 Rise and Fall Time Test Condition**

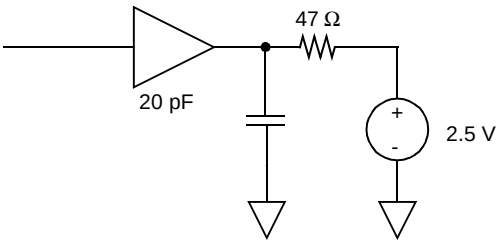
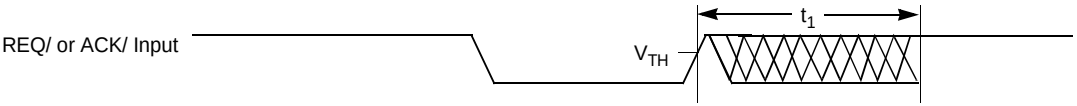


**Figure 5.4 SCSI Input Filtering**




Note: $t_1$ is the input filtering period.

## 5.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Section 5.1, "DC Characteristics"). Chip timing is based on simulation at worst case voltage, temperature, and processing. Timing was developed with a load capacitance of 50 pF. Table 5.13 and Figure 5.5 provide external clock timing data.

**Table 5.13 External Clock**

| Symbol | Parameter | 133 MHz PCI-X | | 66 MHz PCI-X | | 66 MHz PCI | | 33 MHz PCI | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_1$ | PCI Bus clock period[1] | 7.5 | 20 | 15 | 20 | 15 | 30 | 30 | 250 | ns |
| | SCSI clock period | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | ns |
| $t_2$ | PCI CLK LOW time[2] | 3 | – | 6 | – | 6 | – | 11 | – | ns |
| | SCLK LOW time | 10 | 15 | 10 | 15 | 10 | 15 | 10 | 15 | ns |
| $t_3$ | PCI CLK HIGH time | 3 | – | 6 | – | 6 | – | 11 | – | ns |
| | SCLK HIGH time | 10 | 15 | 10 | 15 | 10 | 15 | 10 | 15 | ns |
| $t_4$ | PCI CLK slew rate | 1.5 | 4 | 1.5 | 4 | 1.5 | 4 | 1 | 4 | V/ns |

1. For frequencies above 33 MHz, the clock frequency can not be changed beyond the spread spectrum limits except while RST/ is asserted.
2. Duty cycle not to exceed 60/40.

**Figure 5.5 External Clock**

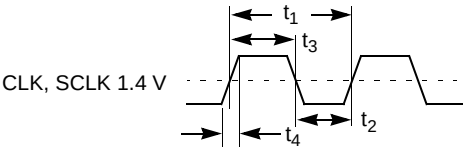



Table 5.14 and Figure 5.6 provide reset input timing data.

**Table 5.14 Reset Input**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_1$ | Reset pulse width | 10 | – | ns |
| $t_2$ | Reset deasserted setup to CLK HIGH | 0 | – | ns |
| $t_3$ | MAD setup time to CLK HIGH (for configuring the MAD bus only) | 20 | – | ns |
| $t_4$ | MAD hold time from CLK HIGH (for configuring the MAD bus only) | 20 | – | ns |

**Figure 5.6 Reset Input**

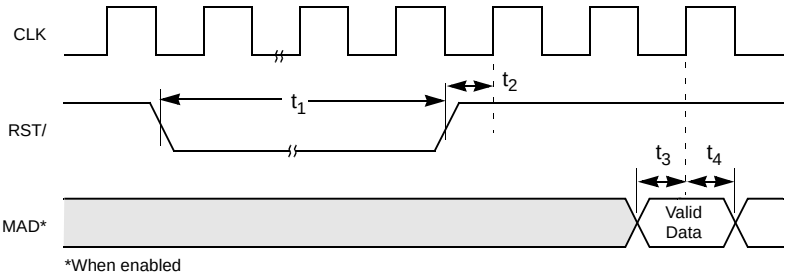
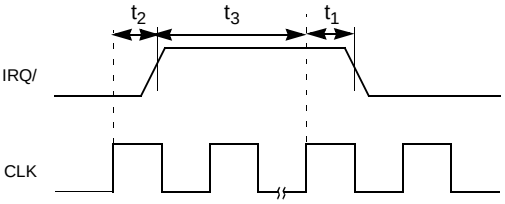



Table 5.15 and Figure 5.7 provide Interrupt Output timing data.

**Table 5.15 Interrupt Output**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_1$ | CLK HIGH to IRQ/ LOW | 2 | 11 | ns |
| $t_2$ | CLK HIGH to IRQ/ HIGH | 2 | 11 | ns |
| $t_3$ | IRQ/ deassertion time | 3 | – | CLK |

**Figure 5.7 Interrupt Output**




## 5.4 External Memory Timing Diagrams

This section provides timing diagrams and data for NVSRAM and Flash ROM timings.

### 5.4.1 NVSRAM Timing

Table 5.16 and Figure 5.8 provide the timing information for the Memory Address and Data (MAD) bus NVSRAM read accesses.

**Table 5.16 NVSRAM Read Cycle Timing**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_1$ | Address setup to FLSHALE/ HIGH | 25 | – | ns |
| $t_2$ | Address hold from FLSHALE/ HIGH | 25 | – | ns |
| $t_3$ | FLSHALE/ pulse width | 25 | – | ns |
| $t_4$ | Address valid to data clocked in | 135 | – | ns |
| $t_5$ | RAMCE/ LOW to data clocked in | 85 | – | ns |
| $t_6$ | MOE/ LOW to data clocked in | 75 | – | ns |
| $t_7$ | Data setup to MOE/ HIGH | 10 | – | ns |
| $t_8$ | Data setup to RAMCE/ HIGH | 10 | – | ns |
| $t_9$ | Data hold from RAMCE/ HIGH | 0 | – | ns |

**Figure 5.8 NVSRAM Read Cycle**

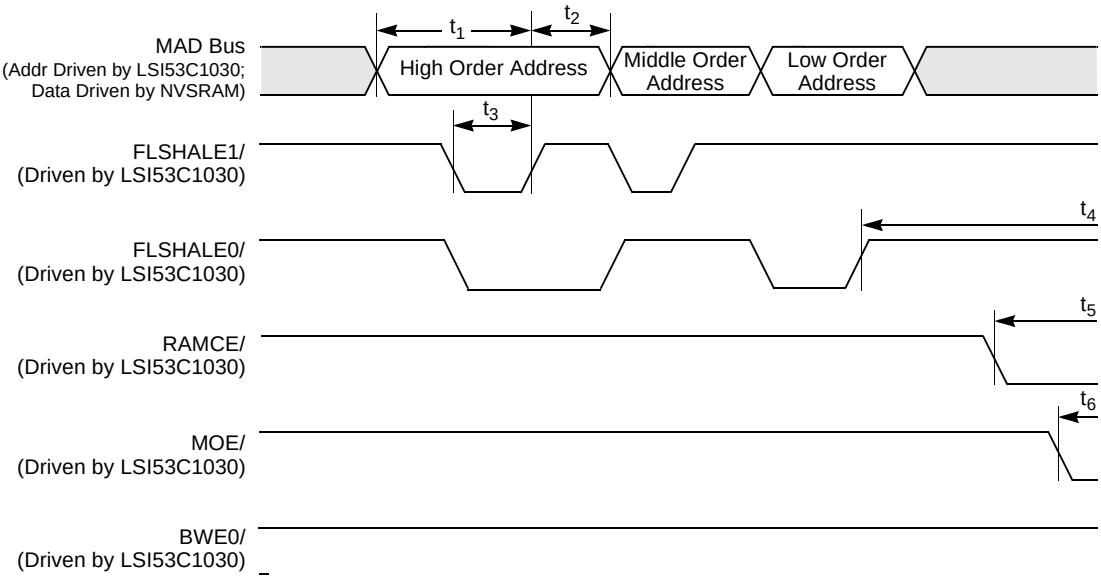



**Figure 5.8 NVSRAM Read Cycle (Cont.)**

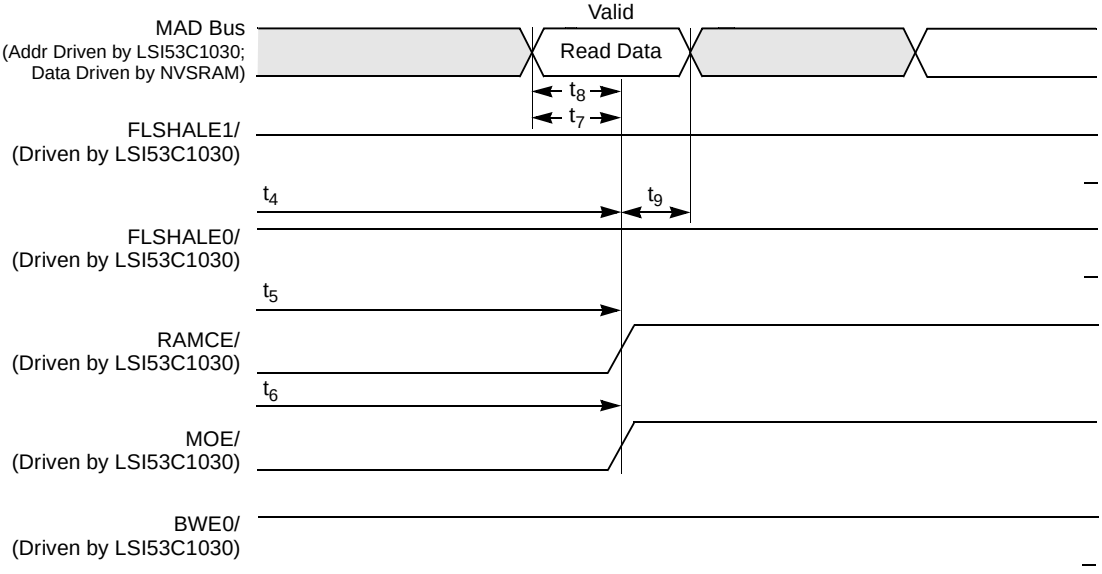


Table 5.17 and Figure 5.9 provide the timing information for NVSRAM write accesses.

**Table 5.17 NVSRAM Write Cycle**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{11}$ | Address setup to FLSHALE/ HIGH | 25 | – | ns |
| $t_{12}$ | Address hold from FLSHALE/ HIGH | 25 | – | ns |
| $t_{13}$ | FLSHALE/ pulse width | 25 | – | ns |
| $t_{20}$ | Data setup to BWE0/ LOW | 40 | – | ns |
| $t_{21}$ | Data hold from BWE0/ HIGH | 30 | – | ns |
| $t_{22}$ | BWE0/ pulse width | 20 | – | ns |
| $t_{23}$ | Address setup to BWE0/ LOW | 75 | – | ns |
| $t_{24}$ | RAMCE/ LOW to BWE0/ HIGH | 60 | – | ns |
| $t_{25}$ | RAMCE/ LOW to BWE0/ LOW | 25 | – | ns |
| $t_{26}$ | BWE0/ HIGH to RAMCE/ HIGH | 25 | – | ns |
| $t_{27}$ | RAMCE/ pulse width | 100 | – | ns |

**Figure 5.9 NVSRAM Write Cycle**

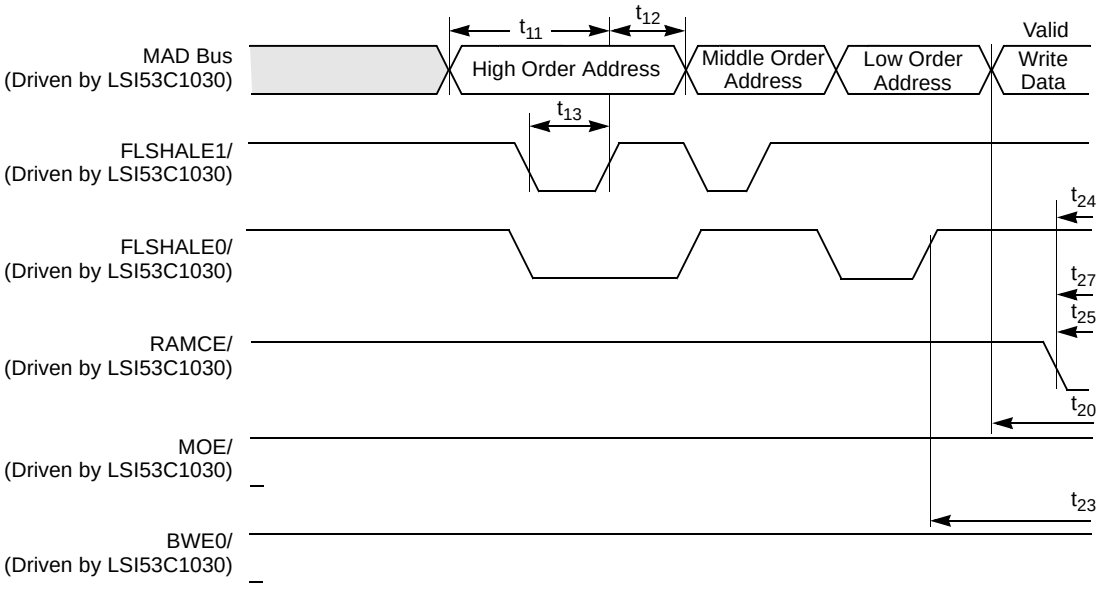
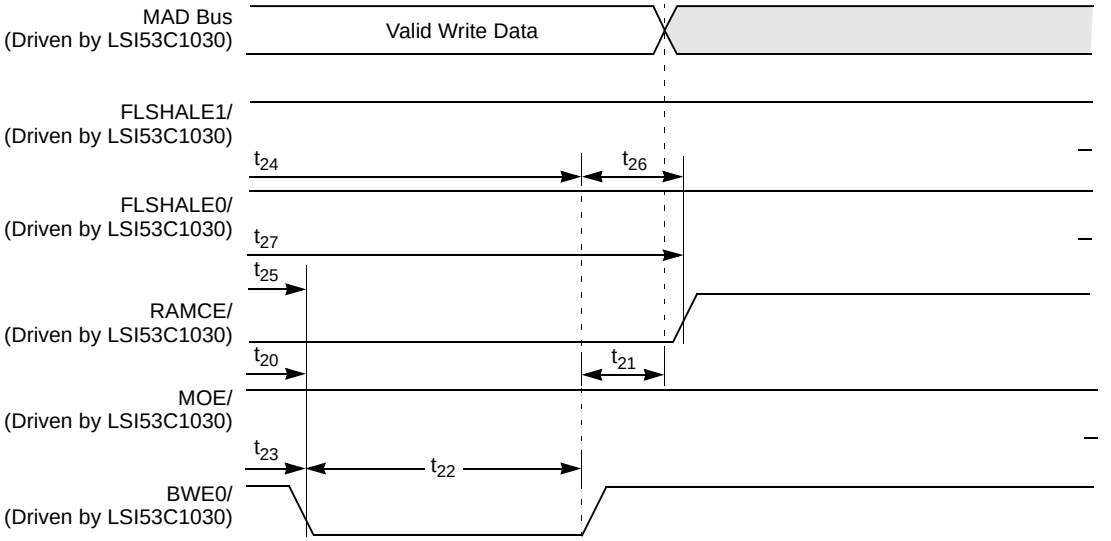



**Figure 5.9 NVSRAM Write Cycle (Cont.)**



## 5.4.2 Flash ROM Timing

Table 5.18 and Figure 5.10 provide the timing information for Flash ROM read accesses.

**Table 5.18 Flash ROM Read Cycle Timing**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_1$ | Address setup to FLSHALE/ HIGH | 25 | – | ns |
| $t_2$ | Address hold from FLSHALE/ HIGH | 25 | – | ns |
| $t_3$ | FLSHALE/ pulse width | 25 | – | ns |
| $t_4$ | Address valid to data clocked in | 135 | – | ns |
| $t_5$ | FLSHCE/ LOW to data clocked in | 85 | – | ns |
| $t_6$ | MOE/ LOW to data clocked in | 75 | – | ns |
| $t_7$ | Data setup to MOE/ HIGH | 10 | – | ns |
| $t_8$ | Data setup to FLSHCE/ HIGH | 10 | – | ns |
| $t_9$ | Data hold from FLSHCE/ HIGH | 0 | – | ns |

**Figure 5.10 Flash ROM Read Cycle**

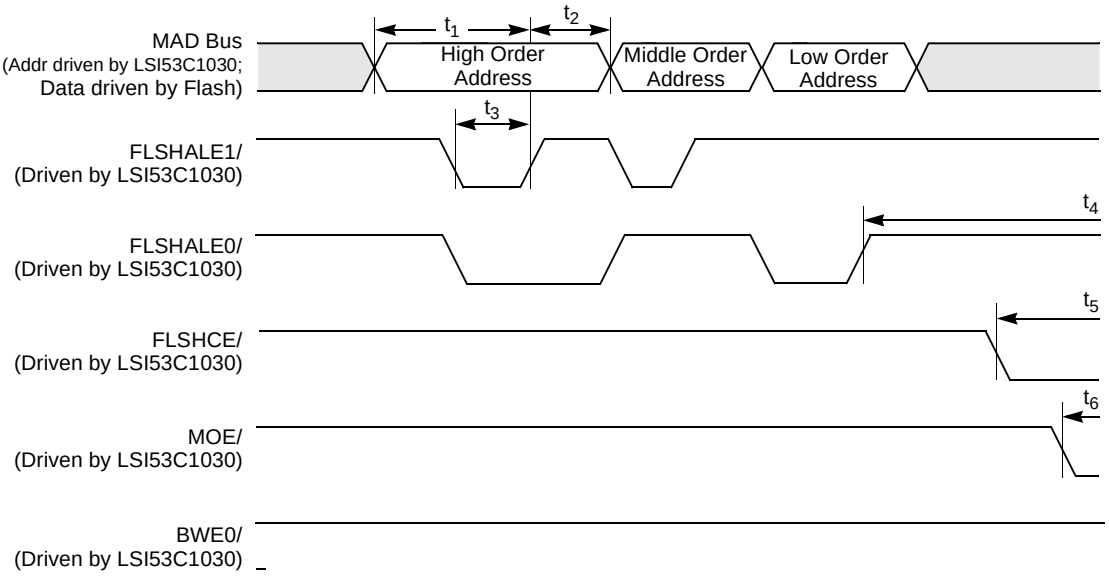



**Figure 5.10 Flash ROM Read Cycle (Cont.)**

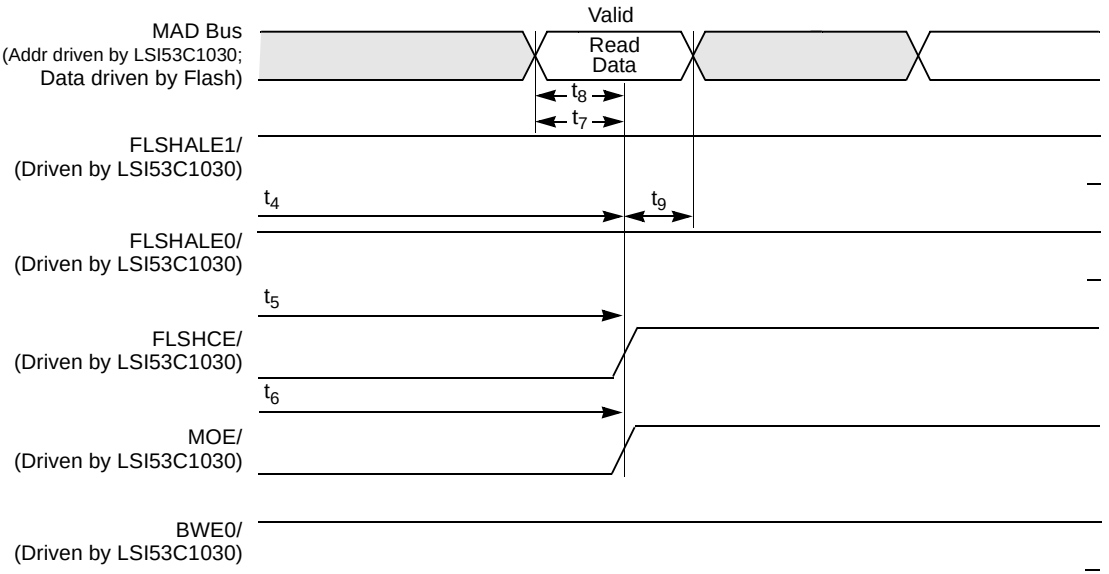


Table 5.19 and Figure 5.11 provide the timing information for Flash ROM write accesses.

**Table 5.19 Flash ROM Write Cycle**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{11}$ | Address setup to FLSHALE/ HIGH | 25 | – | ns |
| $t_{12}$ | Address hold from FLSHALE/ HIGH | 25 | – | ns |
| $t_{13}$ | FLSHALE/ pulse width | 25 | – | ns |
| $t_{20}$ | Data setup to BWE0/ LOW | 40 | – | ns |
| $t_{21}$ | Data hold from BWE0/ HIGH | 30 | – | ns |
| $t_{22}$ | BWE0/ pulse width | 20 | – | ns |
| $t_{23}$ | Address setup to BWE0/ LOW | 75 | – | ns |
| $t_{24}$ | FLSHCE/ LOW to BWE0/ HIGH | 60 | – | ns |
| $t_{25}$ | FLSHCE/ LOW to BWE0/ LOW | 25 | – | ns |
| $t_{26}$ | BWE0/ HIGH to RAMCE/ HIGH | 25 | – | ns |
| $t_{27}$ | FLSHCE/ pulse width | 100 | – | ns |

**Figure 5.11 Flash ROM Write Cycle**

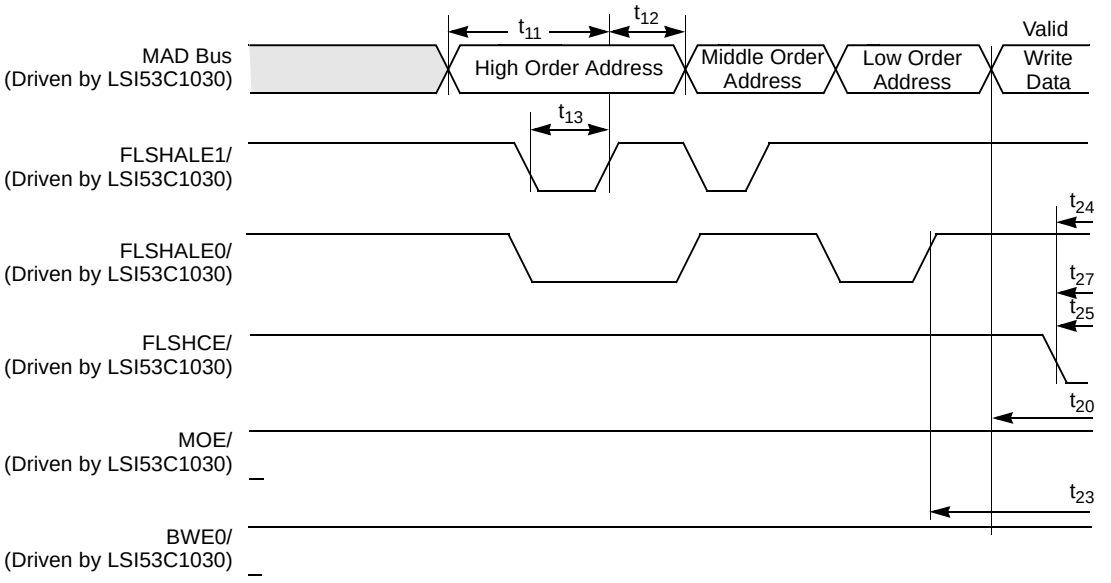
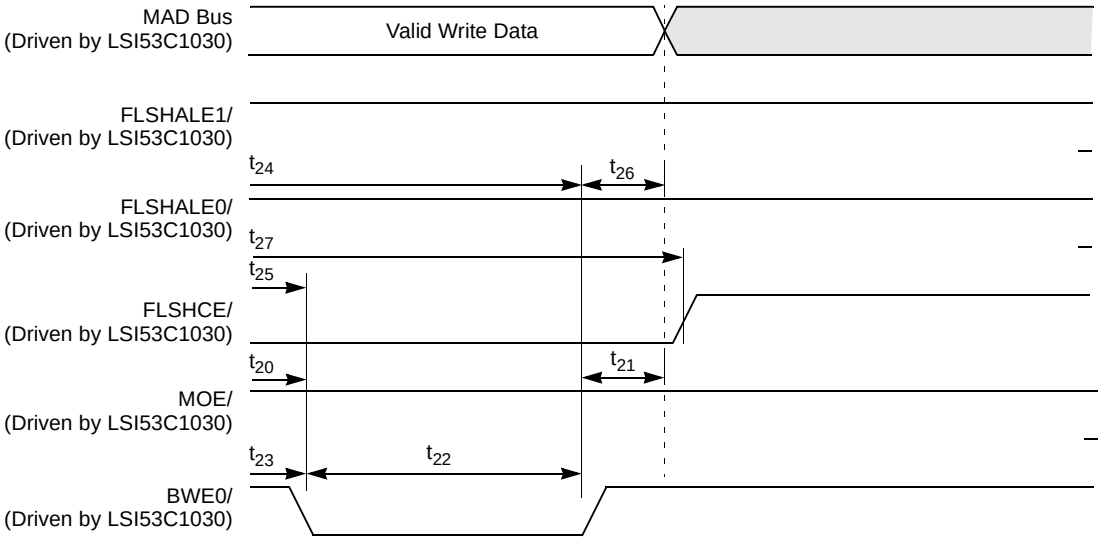



**Figure 5.11 Flash ROM Write Cycle (Cont.)**



## 5.5 Package Drawings

Figure 5.12 illustrates the signal locations on the Ball Grid Array (BGA).

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## Figure 5.12 LSI53C1030 456-Pin BGA Top View

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 VDD_IO | A2 VDD_IO | A3 B_SD12– | A4 B_SD12+ | A5 VSS_IO | A6 VDD_IO | A7 B_SDP1– | A8 B_SD0+ | A9 VSS_IO | A10 VDD_IO | A11 B_RBIAS | A12 B_SD6– | A13 VSS_IO |
| B1 VSS_IO | B2 TRACE PKT1 | B3 TRACECLK | B4 VSSC | B5 B_SD13+ | B6 B_SD14+ | B7 B_SD15+ | B8 B_SD0– | B9 B_SD1+ | B10 B_SD4– | B11 B_SD5– | B12 B_SD6+ | B13 B_VDDBIAS |
| C1 VDDA | C2 TRACE PKT4 | C3 PIPESTAT2 | C4 VSS_IO | C5 TN | C6 B_SD13– | C7 VDD_IO | C8 VSS_IO | C9 B_SD2– | C10 B_SD4+ | C11 VDD_IO | C12 VSS_IO | C13 B_SDP0+ |
| D1 A_SD11+ | D2 VDDC | D3 VDD_IO | D4 TRACE PKT0 | D5 PIPESTAT0 | D6 VDDC | D7 TESTCLKEN | D8 B_SD15– | D9 B_SD1– | D10 B_SD3– | D11 B_SD5+ | D12 B_SDP0– | D13 B_SATN+ |
| E1 VSS_IO | E2 A_ DIFFSENS | E3 TRACE PKT5 | E4 TRACE PKT3 | E5 TRACSYNC | E6 PIPESTAT1 | E7 SCANMODE | E8 B_SD14– | E9 B_SDP1+ | E10 B_SD2+ | E11 B_SD3+ | E12 B_SD7+ | E13 B_SD7– |
| F1 VDD_IO | F2 A_SD11- | F3 SCLK | F4 TRACE PKT7 | F5 TRACE PKT2 | | | | | | | | |
| G1 A_SD10+ | G2 A_SD10– | G3 VSS_IO | G4 VSSC | G5 TRACE PKT6 | | | | | | | | |
| H1 A_SD8- | H2 A_SD8+ | H3 VDD_IO | H4 A_SD9+ | H5 VSSA | | | | | | | | |
| J1 VSS_IO | J2 A_SREQ- | J3 A_SREQ+ | J4 A_SD9- | J5 A_SIO+ | | | | | | | | |
| K1 VDD_IO | K2 A_SSEL+ | K3 A_SCD- | K4 A_SCD+ | K5 A_SIO- | | | | | | | | |
| L1 A_SMSG+ | L2 A_SMSG- | L3 VSS_IO | L4 A_SSEL– | L5 A_SACK+ | | | | | | L11 VSS_IO | L12 VSS_IO | L13 VSS_IO |
| M1 A_SRST– | M2 A_SRST+ | M3 VDD_IO | M4 A_SATN– | M5 A_SACK– | | | | | | M11 VSS_IO | M12 VSS_IO | M13 VSS_IO |
| N1 VSS_IO | N2 VDDC | N3 A_SBSY– | N4 A_SBSY+ | N5 A_SATN+ | | | | | | N11 VSS_IO | N12 VSS_IO | N13 VSS_IO |
| P1 VDD_IO | P2 VSSC | P3 A_SD7+ | P4 A_SDP0– | P5 A_SDP0+ | | | | | | P11 VSS_IO | P12 VSS_IO | P13 VSS_IO |
| R1 A_RBIAS | R2 A_SD5+ | R3 VSS_IO | R4 A_SD7– | R5 A_SD6+ | | | | | | R11 VSS_IO | R12 VSS_IO | R13 VSS_IO |
| T1 A_VDDBIAS | T2 A_SD5– | T3 VDD_IO | T4 A_SD4+ | T5 A_SD6– | | | | | | T11 VSS_IO | T12 VSS_IO | T13 VSS_IO |
| U1 VSS_IO | U2 A_SD4– | U3 A_SD2+ | U4 A_SD3+ | U5 A_SD3– | | | | | | | | |
| V1 VDD_IO | V2 A_SD2– | V3 A_SD0+ | V4 A_SD1– | V5 A_SD1+ | | | | | | | | |
| W1 A_SDP1+ | W2 A_SDP1– | W3 VSS_IO | W4 A_SD0– | W5 ASD15+ | | | | | | | | |
| Y1 A_SD15– | Y2 A_SD14+ | Y3 VDD_IO | Y4 IDDTN | Y5 TMS_ICE | | | | | | | | |
| AA1 VSS_IO | AA2 A_SD14– | AA3 A_SD13+ | AA4 TCK_ICE | AA5 RTCK_ICE | | | | | | | | |
| AB1 VDD_IO | AB2 A_SD13– | AB3 TDI_ICE | AB4 TRST_ICE/ | AB5 VSSC | AB6 TESTACLK | AB7 VSSC | AB8 VSSC | AB9 ALT_INTB/ | AB10 RST/ | AB11 AD28 | AB12 AD24 | AB13 C_BE3/ |
| AC1 A_SD12+ | AC2 CLK MODE_1 | AC3 VSS_IO | AC4 DIS_SCSI_ FSN/ | AC5 IOPD_GNT/ | AC6 TCK_CHIP | AC7 VDDC | AC8 INTA/ | AC9 NC | AC10 PCI5VBIAS | AC11 AD27 | AC12 AD23 | AC13 IDSEL |
| AD1 A_SD12– | AD2 TDO_ICE | AD3 VDDC | AD4 VDD_IO | AD5 TST_RST/ | AD6 TDO_CHIP | AD7 VSS_IO | AD8 VDD_IO | AD9 PCI5VBIAS | AD10 REQ/ | AD11 VSS_IO | AD12 VDD_IO | AD13 AD22 |
| AE1 VSS_IO | AE2 TESTHCLK | AE3 VDDC | AE4 TMS_CHIP | AE5 PVT1 | AE6 PCI5VBIAS | AE7 INTB/ | AE8 GNT/ | AE9 AD31 | AE10 AD29 | AE11 AD26 | AE12 AD25 | AE13 AD21 |
| AF1 VDD_IO | AF2 VSS_IO | AF3 TDI_CHIP | AF4 PVT2 | AF5 VDD_IO | AF6 VSS_IO | AF7 ALT_INTA/ | AF8 AD30 | AF9 VDD_IO | AF10 VSS_IO | AF11 AD20 | AF12 PCI5VBIAS | AF13 VDD_IO |

## Figure 5.12 LSI53C1030 456-Pin BGA Top View (Cont.)

| A14 | A15 | A16 | A17 | A18 | A19 | A20 | A21 | A22 | A23 | A24 | A25 | A26 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VDD_IO | B_SBSY– | B_SRST+ | VSS_IO | VDD_IO | B_SD8– | B_SD9+ | VSS_IO | VDD_IO | B_SD11+ | DIS_PCI_FSN/ | VSS_IO | VDD_IO |
| B14 | B15 | B16 | B17 | B18 | B19 | B20 | B21 | B22 | B23 | B24 | B25 | B26 |
| B_SATN– | B_SBSY+ | B_SMSG– | B_SSEL– | B_SREQ– | B_SD8+ | B_SD10+ | B_SD11– | B_DIFFSENS | ADV/ | MADP0 | MAD13 | VSS_IO |
| C14 | C15 | C16 | C17 | C18 | C19 | C20 | C21 | C22 | C23 | C24 | C25 | C26 |
| VSSC | VDD_IO | VSS_IO | B_SSEL+ | B_SREQ+ | VDD_IO | VSS_IO | VSSC | MADP1 | VDD_IO | MAD10 | HB_LED/ | VSSC |
| D14 | D15 | D16 | D17 | D18 | D19 | D20 | D21 | D22 | D23 | D24 | D25 | D26 |
| B_SACK– | VDDC | B_SMSG+ | B_SCD+ | B_SIO+ | B_SD10– | RAMCE/ | ADSC/ | MAD15 | MAD12 | VSS_IO | MAD2 | MAD7 |
| E14 | E15 | E16 | E17 | E18 | E19 | E20 | E21 | E22 | E23 | E24 | E25 | E26 |
| B_SACK+ | B_SRST– | B_SCD– | B_SIO– | B_SD9– | VDDC | MCLK | MAD14 | MAD11 | MAD8 | BWE1/ | MAD6 | VDD_IO |
| | | | | | | | | F22 | F23 | F24 | F25 | F26 |
| | | | | | | | | MAD9 | MAD1 | MAD4 | VSSC | VSS_IO |
| | | | | | | | | G22 | G23 | G24 | G25 | G26 |
| | | | | | | | | MAD0 | MAD3 | VDD_IO | FLSHCE/ | MOE/ |
| | | | | | | | | H22 | H23 | H24 | H25 | H26 |
| | | | | | | | | MAD5 | BWE0/ | VSS_IO | GPIO3 | SerialDATA |
| | | | | | | | | J22 | J23 | J24 | J25 | J26 |
| | | | | | | | | VDDC | A_LED/ | FLSHALE1/ | SerialCLK | VDD_IO |
| | | | | | | | | K22 | K23 | K24 | K25 | K26 |
| | | | | | | | | FLSHALE0/ | B_LED/ | GPIO2 | GPIO7 | VSS_IO |
| L14 | L15 | L16 | | | | | | L22 | L23 | L24 | L25 | L26 |
| VSS_IO | VSS_IO | VSS_IO | | | | | | VSSC | GPIO6 | VDD_IO | GPIO5 | AD34 |
| M14 | M15 | M16 | | | | | | M22 | M23 | M24 | M25 | M26 |
| VSS_IO | VSS_IO | VSS_IO | | | | | | VDDC | PCI5VBIAS | VSS_IO | GPIO4 | AD35 |
| N14 | N15 | N16 | | | | | | N22 | N23 | N24 | N25 | N26 |
| VSS_IO | VSS_IO | VSS_IO | | | | | | SCANEN | ZCR_EN/ | AD32 | AD33 | VDD_IO |
| P14 | P15 | P16 | | | | | | P22 | P23 | P24 | P25 | P26 |
| VSS_IO | VSS_IO | VSS_IO | | | | | | AD42 | AD41 | AD39 | AD38 | VSS_IO |
| R14 | R15 | R16 | | | | | | R22 | R23 | R24 | R25 | R26 |
| VSS_IO | VSS_IO | VSS_IO | | | | | | AD43 | AD40 | VDD_IO | AD44 | AD36 |
| T14 | T15 | T16 | | | | | | T22 | T23 | T24 | T25 | T26 |
| VSS_IO | VSS_IO | VSS_IO | | | | | | AD47 | AD46 | VSS_IO | AD45 | AD37 |
| | | | | | | | | U22 | U23 | U24 | U25 | U26 |
| | | | | | | | | AD55 | AD49 | AD52 | AD48 | VDD_IO |
| | | | | | | | | V22 | V23 | V24 | V25 | V26 |
| | | | | | | | | AD56 | AD53 | AD54 | AD51 | VSS_IO |
| | | | | | | | | W22 | W23 | W24 | W25 | W26 |
| | | | | | | | | AD63 | AD59 | VDD_IO | PCI5VBIAS | AD50 |
| | | | | | | | | Y22 | Y23 | Y24 | Y25 | Y26 |
| | | | | | | | | PCI5VBIAS | C_BE5/ | VSS_IO | AD58 | AD57 |
| | | | | | | | | AA22 | AA23 | AA24 | AA25 | AA26 |
| | | | | | | | | CLK MODE_0 | C_BE7/ | PAR64 | AD60 | VDD_IO |
| AB14 | AB15 | AB16 | AB17 | AB18 | AB19 | AB20 | AB21 | AB22 | AB23 | AB24 | AB25 | AB26 |
| C_BE2/ | FRAME/ | STOP/ | AD12 | AD11 | AD5 | ACK64/ | VDDA | PCI5VBIAS | VSSC | VSSC | AD62 | VSS_IO |
| AC14 | AC15 | AC16 | AC17 | AC18 | AC19 | AC20 | AC21 | AC22 | AC23 | AC24 | AC25 | AC26 |
| AD16 | AD17 | DEVSEL/ | SERR/ | AD13 | AD8 | AD2 | AD0 | CLK | GPIO0 | VDD_IO | C_BE6/ | AD61 |
| AD14 | AD15 | AD16 | AD17 | AD18 | AD19 | AD20 | AD21 | AD22 | AD23 | AD24 | AD25 | AD26 |
| VSSC | VSS_IO | VDD_IO | AD15 | PCI5VBIAS | VSS_IO | VDD_IO | AD4 | REQ64/ | VSS_IO | VSSA | VDDC | C_BE4/ |
| AE14 | AE15 | AE16 | AE17 | AE18 | AE19 | AE20 | AE21 | AE22 | AE23 | AE24 | AE25 | AE26 |
| AD18 | IRDY/ | TRDY/ | PERR/ | C_BE1/ | AD14 | AD9 | C_BE0/ | AD6 | AD1 | VDDC | GPIO1 | VDD_IO |
| AF14 | AF15 | AF16 | AF17 | AF18 | AF19 | AF20 | AF21 | AF22 | AF23 | AF24 | AF25 | AF26 |
| VSS_IO | VDDC | AD19 | VDD_IO | VSS_IO | PAR | AD10 | VDD_IO | VSS_IO | AD7 | AD3 | VDD_IO | VSS_IO |

Table 5.20 contains the pinout for the LSI53C1030.

**Table 5.20 LSI53C1030 Signal List by Signal Name**

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|---|---|---|---|---|---|---|---|---|---|
| ACK64/ | AB20 | AD45 | T25 | A_SD6- | T5 | B_SD0- | B8 | B_VDDBIAS | B13 |
| AD0 | AC21 | AD46 | T23 | A_SD6+ | R5 | B_SD0+ | A8 | BWE0/ | H23 |
| AD1 | AE23 | AD47 | T22 | A_SD7- | R4 | B_SD1- | D9 | BWE1/ | E24 |
| AD2 | AC20 | AD48 | U25 | A_SD7+ | P3 | B_SD1+ | B9 | C_BE0/ | AE21 |
| AD3 | AF24 | AD49 | U23 | A_SD8- | H1 | B_SD2- | C9 | C_BE1/ | AE18 |
| AD4 | AD21 | AD50 | W26 | A_SD8+ | H2 | B_SD2+ | E10 | C_BE2/ | AB14 |
| AD5 | AB19 | AD51 | V25 | A_SD9- | J4 | B_SD3- | D10 | C_BE3/ | AB13 |
| AD6 | AE22 | AD52 | U24 | A_SD9+ | H4 | B_SD3+ | E11 | C_BE4/ | AD26 |
| AD7 | AF23 | AD53 | V23 | A_SD10- | G2 | B_SD4- | B10 | C_BE5/ | Y23 |
| AD8 | AC19 | AD54 | V24 | A_SD10+ | G1 | B_SD4+ | C10 | C_BE6/ | AC25 |
| AD9 | AE20 | AD55 | U22 | A_SD11- | F2 | B_SD5- | B11 | C_BE7/ | AA23 |
| AD10 | AF20 | AD56 | V22 | A_SD11+ | D1 | B_SD5+ | D11 | CLK | AC22 |
| AD11 | AB18 | AD57 | Y26 | A_SD12- | AD1 | B_SD6- | A12 | CLK | |
| AD12 | AB17 | AD58 | Y25 | A_SD12+ | AC1 | B_SD6+ | B12 | MODE_0 | AA22 |
| AD13 | AC18 | AD59 | W23 | A_SD13- | AB2 | B_SD7- | E13 | CLK | |
| AD14 | AE19 | AD60 | AA25 | A_SD13+ | AA3 | B_SD7+ | E12 | MODE_1 | AC2 |
| AD15 | AD17 | AD61 | AC26 | A_SD14- | AA2 | B_SD8- | A19 | DIS_ | |
| AD16 | AC14 | AD62 | AB25 | A_SD14+ | Y2 | B_SD8+ | B19 | PCI_FSN/ | A24 |
| AD17 | AC15 | AD63 | W22 | A_SD15- | Y1 | B_SD9- | E18 | DIS_ | |
| AD18 | AE14 | A_DIFFSENS | E2 | A_SD15+ | W5 | B_SD9+ | A20 | SCSI_FSN/ | AC4 |
| AD19 | AF16 | ADSC/ | D21 | A_SDP0- | P4 | B_SD10- | D19 | DEVSEL/ | AC16 |
| AD20 | AF11 | ADV/ | B23 | A_SDP0+ | P5 | B_SD10+ | B20 | FLSHALE0/ | K22 |
| AD21 | AE13 | A_LED/ | J23 | A_SDP1- | W2 | B_SD11- | B21 | FLSHALE1/ | J24 |
| AD22 | AD13 | ALT_INTA/ | AF7 | A_SDP1+ | W1 | B_SD11+ | A23 | FLSHCE/ | G25 |
| AD23 | AC12 | ALT_INTB/ | AB9 | A_SIO- | K5 | B_SD12- | A3 | FRAME/ | AB15 |
| AD24 | AB12 | A_RBIAS | R1 | A_SIO+ | J5 | B_SD12+ | A4 | GNT/ | AE8 |
| AD25 | AE12 | A_SACK- | M5 | A_SMSG- | L2 | B_SD13- | C6 | GPIO0 | AC23 |
| AD26 | AE11 | A_SACK+ | L5 | A_SMSG+ | L1 | B_SD13+ | B5 | GPIO1 | AE25 |
| AD27 | AC11 | A_SATN- | M4 | A_SREQ- | J2 | B_SD14- | E8 | GPIO2 | K24 |
| AD28 | AB11 | A_SATN+ | N5 | A_SREQ+ | J3 | B_SD14+ | B6 | GPIO3 | H25 |
| AD29 | AE10 | A_SBSY- | N3 | A_SRST- | M1 | B_SD15- | D8 | GPIO4 | M25 |
| AD30 | AF8 | A_SBSY+ | N4 | A_SRST+ | M2 | B_SD15+ | B7 | GPIO5 | L25 |
| AD31 | AE9 | A_SCD- | K3 | A_SSEL- | L4 | B_SDP0- | D12 | GPIO6 | L23 |
| AD32 | N24 | A_SCD+ | K4 | A_SSEL+ | K2 | B_SDP0+ | C13 | GPIO7 | K25 |
| AD33 | N25 | A_SD0- | W4 | A_VDDBIAS | T1 | B_SDP1- | A7 | HB_LED/ | C25 |
| AD34 | L26 | A_SD0+ | V3 | B_DIFFSENS | B22 | B_SDP1+ | E9 | IDDTN | Y4 |
| AD35 | M26 | A_SD1- | V4 | B_LED/ | K23 | B_SIO- | E17 | IDSEL | AC13 |
| AD36 | R26 | A_SD1+ | V5 | B_RBIAS | A11 | B_SIO+ | D18 | INTA/ | AC8 |
| AD37 | T26 | A_SD2- | V2 | B_SACK- | D14 | B_SMSG- | B16 | INTB/ | AE7 |
| AD38 | P25 | A_SD2+ | U3 | B_SACK+ | E14 | B_SMSG+ | D16 | IOPD_GNT/ | AC5 |
| AD39 | P24 | A_SD3- | U5 | B_SATN- | B14 | B_SREQ- | B18 | IRDY/ | AE15 |
| AD40 | R23 | A_SD3+ | U4 | B_SATN+ | D13 | B_SREQ+ | C18 | MAD0 | G22 |
| AD41 | P23 | A_SD4- | U2 | B_SBSY- | A15 | B_SRST- | E15 | MAD1 | F23 |
| AD42 | P22 | A_SD4+ | T4 | B_SBSY+ | B15 | B_SRST+ | A16 | MAD2 | D25 |
| AD43 | R22 | A_SD5- | T2 | B_SCD- | E16 | B_SSEL- | B17 | MAD3 | G23 |
| AD44 | R25 | A_SD5+ | R2 | B_SCD+ | D17 | B_SSEL+ | C17 | MAD4 | F24 |

**Table 5.20 LSI53C1030 Signal List by Signal Name (Cont.)**

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|---|---|---|---|---|---|---|---|---|---|
| MAD5 | H22 | TCK_ICE | AA4 | VDD_IO | N26 | VSS_IO | B26 | VSS_IO | R15 |
| MAD6 | E25 | TDI_CHIP | AF3 | VDD_IO | P1 | VSS_IO | C4 | VSS_IO | R16 |
| MAD7 | D26 | TDI_ICE | AB3 | VDD_IO | R24 | VSS_IO | C8 | VSS_IO | T11 |
| MAD8 | E23 | TDO_CHIP | AD6 | VDD_IO | T3 | VSS_IO | C12 | VSS_IO | T12 |
| MAD9 | F22 | TDO_ICE | AD2 | VDD_IO | U26 | VSS_IO | C16 | VSS_IO | T13 |
| MAD10 | C24 | TESTCLKEN | D7 | VDD_IO | V1 | VSS_IO | C20 | VSS_IO | T14 |
| MAD11 | E22 | TESTACLK | AB6 | VDD_IO | W24 | VSS_IO | D24 | VSS_IO | T15 |
| MAD12 | D23 | TESTHCLK | AE2 | VDD_IO | Y3 | VSS_IO | E1 | VSS_IO | T16 |
| MAD13 | B25 | TMS_CHIP | AE4 | VDD_IO | AA26 | VSS_IO | F26 | VSS_IO | T24 |
| MAD14 | E21 | TMS_ICE | Y5 | VDD_IO | AB1 | VSS_IO | G3 | VSS_IO | U1 |
| MAD15 | D22 | TN | C5 | VDD_IO | AC24 | VSS_IO | H24 | VSS_IO | V26 |
| MADP0 | B24 | TRACECLK | B3 | VDD_IO | AD4 | VSS_IO | J1 | VSS_IO | W3 |
| MADP1 | C22 | TRACEPKT0 | D4 | VDD_IO | AD8 | VSS_IO | K26 | VSS_IO | Y24 |
| MCLK | E20 | TRACEPKT1 | B2 | VDD_IO | AD12 | VSS_IO | L3 | VSS_IO | AA1 |
| MOE/ | G26 | TRACEPKT2 | F5 | VDD_IO | AD16 | VSS_IO | L11 | VSS_IO | AB26 |
| NC | AC9 | TRACEPKT3 | E4 | VDD_IO | AD20 | VSS_IO | L12 | VSS_IO | AC3 |
| PAR | AF19 | TRACEPKT4 | C2 | VDD_IO | AE26 | VSS_IO | L13 | VSS_IO | AD7 |
| PAR64 | AA24 | TRACEPKT5 | E3 | VDD_IO | AF1 | VSS_IO | L14 | VSS_IO | AD11 |
| PCI5VBIAS | AD9 | TRACEPKT6 | G5 | VDD_IO | AF5 | VSS_IO | L15 | VSS_IO | AD15 |
| PCI5VBIAS | AE6 | TRACEPKT7 | F4 | VDD_IO | AF9 | VSS_IO | L16 | VSS_IO | AD19 |
| PCI5VBIAS | AC10 | TRACESYNC | E5 | VDD_IO | AF13 | VSS_IO | M11 | VSS_IO | AD23 |
| PCI5VBIAS | AF12 | TRDY/ | AE16 | VDD_IO | AF17 | VSS_IO | M12 | VSS_IO | AE1 |
| PCI5VBIAS | AD18 | TRST_ICE/ | AB4 | VDD_IO | AF21 | VSS_IO | M13 | VSS_IO | AF2 |
| PCI5VBIAS | AB22 | TST_RST/ | AD5 | VDD_IO | AF25 | VSS_IO | M14 | VSS_IO | AF6 |
| PCI5VBIAS | Y22 | VDD_IO | A1 | VDDA | C1 | VSS_IO | M15 | VSS_IO | AF10 |
| PCI5VBIAS | W25 | VDD_IO | A2 | VDDA | AB21 | VSS_IO | M16 | VSS_IO | AF14 |
| PCI5VBIAS | M23 | VDD_IO | A6 | VDDC | D2 | VSS_IO | M24 | VSS_IO | AF18 |
| PERR/ | AE17 | VDD_IO | A10 | VDDC | N2 | VSS_IO | N1 | VSS_IO | AF22 |
| PIPESTAT0 | D5 | VDD_IO | A14 | VDDC | AD3 | VSS_IO | N11 | VSS_IO | AF26 |
| PIPESTAT1 | E6 | VDD_IO | A18 | VDDC | AE3 | VSS_IO | N12 | VSSA | H5 |
| PIPESTAT2 | C3 | VDD_IO | A22 | VDDC | AC7 | VSS_IO | N13 | VSSA | AD24 |
| PVT1 | AE5 | VDD_IO | A26 | VDDC | AF15 | VSS_IO | N14 | VSSC | G4 |
| PVT2 | AF4 | VDD_IO | C7 | VDDC | AE24 | VSS_IO | N15 | VSSC | P2 |
| RAMCE/ | D20 | VDD_IO | C11 | VDDC | AD25 | VSS_IO | N16 | VSSC | AB5 |
| REQ/ | AD10 | VDD_IO | C15 | VDDC | M22 | VSS_IO | P11 | VSSC | AB7 |
| REQ64/ | AD22 | VDD_IO | C19 | VDDC | J22 | VSS_IO | P12 | VSSC | AB8 |
| RST/ | AB10 | VDD_IO | C23 | VDDC | E19 | VSS_IO | P13 | VSSC | AD14 |
| RTCK_ICE | AA5 | VDD_IO | D3 | VDDC | D15 | VSS_IO | P14 | VSSC | AB23 |
| SCANEN | N22 | VDD_IO | E26 | VDDC | D6 | VSS_IO | P15 | VSSC | AB24 |
| SCANMODE | E7 | VDD_IO | F1 | VSS_IO | A5 | VSS_IO | P16 | VSSC | L22 |
| SCLK | F3 | VDD_IO | G24 | VSS_IO | A9 | VSS_IO | P26 | VSSC | F25 |
| SerialCLK | J25 | VDD_IO | H3 | VSS_IO | A13 | VSS_IO | R3 | VSSC | C26 |
| SerialDATA | H26 | VDD_IO | J26 | VSS_IO | A17 | VSS_IO | R11 | VSSC | C21 |
| SERR/ | AC17 | VDD_IO | K1 | VSS_IO | A21 | VSS_IO | R12 | VSSC | C14 |
| STOP/ | AB16 | VDD_IO | L24 | VSS_IO | A25 | VSS_IO | R13 | VSSC | B4 |
| TCK_CHIP | AC6 | VDD_IO | M3 | VSS_IO | B1 | VSS_IO | R14 | ZCR_EN/ | N23 |

Table 5.21 contains the pinout for the LSI53C1030.

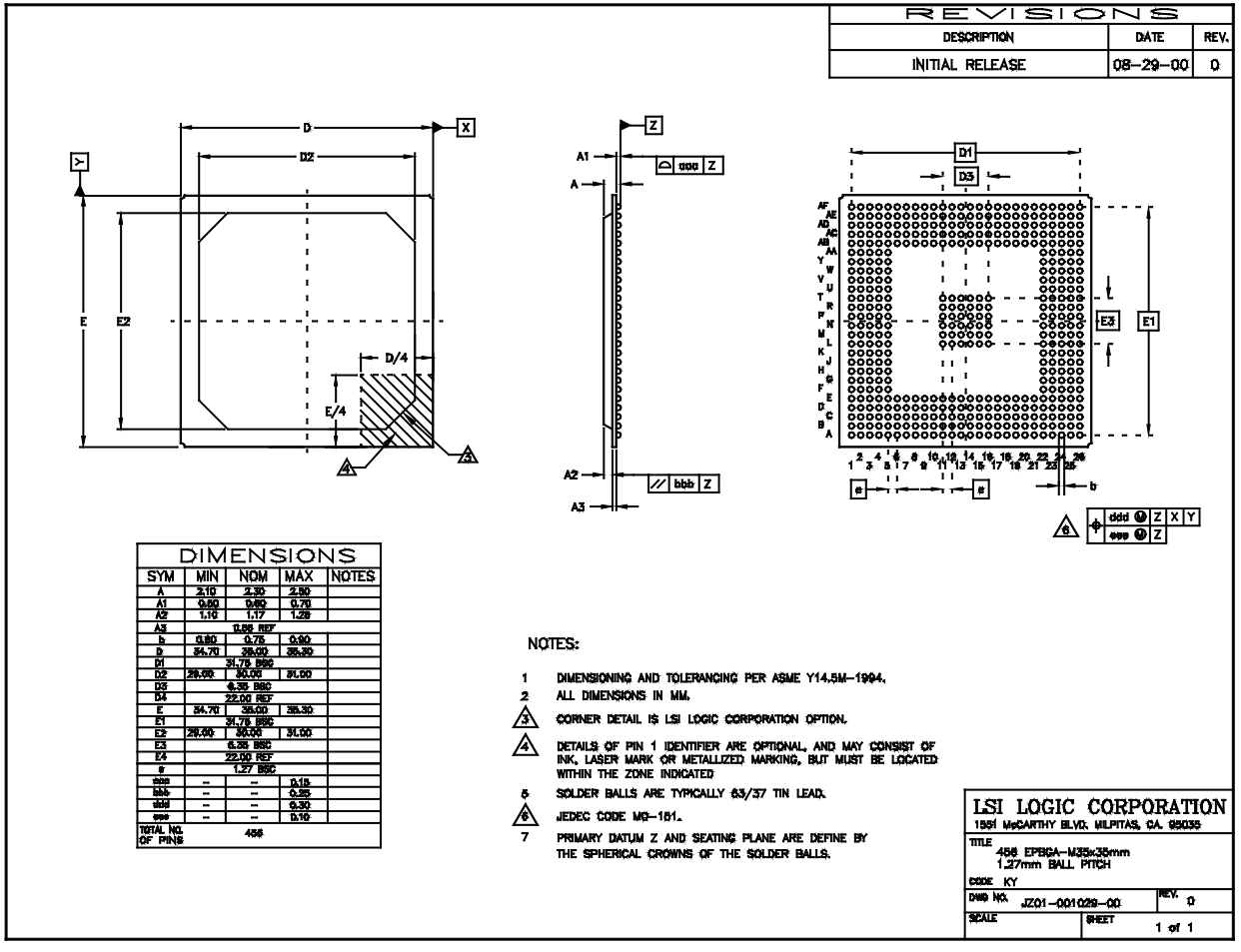
**Table 5.21 LSI53C1030 Signal List by BGA position**

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|---|---|---|---|---|---|---|---|---|---|
| A1 | VDD_IO | B20 | B_SD10+ | D14 | B_SACK- | F24 | MAD4 | L4 | A_SSEL- |
| A2 | VDD_IO | B21 | B_SD11- | D15 | VDDC | F25 | VSSC | L5 | A_SACK+ |
| A3 | B_SD12- | B22 | B_DIFFSENS | D16 | B_SMSG+ | F26 | VSS_IO | L11 | VSS_IO |
| A4 | B_SD12+ | B23 | ADV/ | D17 | B_SCD+ | G1 | A_SD10+ | L12 | VSS_IO |
| A5 | VSS_IO | B24 | MADP0 | D18 | B_SIO+ | G2 | A_SD10- | L13 | VSS_IO |
| A6 | VDD_IO | B25 | MAD13 | D19 | B_SD10- | G3 | VSS_IO | L14 | VSS_IO |
| A7 | B_SDP1- | B26 | VSS_IO | D20 | RAMCE/ | G4 | VSSC | L15 | VSS_IO |
| A8 | B_SD0+ | C1 | VDDA | D21 | ADSC/ | G5 | TRACEPKT6 | L16 | VSS_IO |
| A9 | VSS_IO | C2 | TRACEPKT4 | D22 | MAD15 | G22 | MAD0 | L22 | VSSC |
| A10 | VDD_IO | C3 | PIPESTAT2 | D23 | MAD12 | G23 | MAD3 | L23 | GPIO6 |
| A11 | B_RBIAS | C4 | VSS_IO | D24 | VSS_IO | G24 | VDD_IO | L24 | VDD_IO |
| A12 | B_SD6- | C5 | TN | D25 | MAD2 | G25 | FLSHCE/ | L25 | GPIO5 |
| A13 | VSS_IO | C6 | B_SD13- | D26 | MAD7 | G26 | MOE/ | L26 | AD34 |
| A14 | VDD_IO | C7 | VDD_IO | E1 | VSS_IO | H1 | A_SD8- | M1 | A_SRST- |
| A15 | B_SBSY- | C8 | VSS_IO | E2 | A_DIFFSENS | H2 | A_SD8+ | M2 | A_SRST+ |
| A16 | B_SRST+ | C9 | B_SD2- | E3 | TRACEPKT5 | H3 | VDD_IO | M3 | VDD_IO |
| A17 | VSS_IO | C10 | B_SD4+ | E4 | TRACEPKT3 | H4 | A_SD9+ | M4 | A_SATN- |
| A18 | VDD_IO | C11 | VDD_IO | E5 | TRACESYNC | H5 | VSSA | M5 | A_SACK- |
| A19 | B_SD8- | C12 | VSS_IO | E6 | PIPESTAT1 | H22 | MAD5 | M11 | VSS_IO |
| A20 | B_SD9+ | C13 | B_SDP0+ | E7 | SCANMODE | H23 | BWE0/ | M12 | VSS_IO |
| A21 | VSS_IO | C14 | VSSC | E8 | B_SD14- | H24 | VSS_IO | M13 | VSS_IO |
| A22 | VDD_IO | C15 | VDD_IO | E9 | B_SDP1+ | H25 | GPIO3 | M14 | VSS_IO |
| A23 | B_SD11+ | C16 | VSS_IO | E10 | B_SP2+ | H26 | SerialDATA | M15 | VSS_IO |
| A24 | DIS_ PCI_FSN/ | C17 | B_SSEL+ | E11 | B_SD3+ | J1 | VSS_IO | M16 | VSS_IO |
| | | C18 | B_SREQ+ | E12 | B_SD7+ | J2 | A_SREQ- | M22 | VDDC |
| A25 | VSS_IO | C19 | VDD_IO | E13 | B_SD7- | J3 | A_SREQ+ | M23 | PCI5VBIAS |
| A26 | VDD_IO | C20 | VSS_IO | E14 | B_SACK+ | J4 | A_SD9- | M24 | VSS_IO |
| B1 | VSS_IO | C21 | VSSC | E15 | B_SRST- | J5 | A_SIO+ | M25 | GPIO4 |
| B2 | TRACEPKT1 | C22 | MADP1 | E16 | B_SCD- | J22 | VDDC | M26 | AD35 |
| B3 | TRACECLK | C23 | VDD_IO | E17 | B_SIO- | J23 | A_LED/ | N1 | VSS_IO |
| B4 | VSSC | C24 | MAD10 | E18 | B_SD9- | J24 | FLSHALE1/ | N2 | VDDC |
| B5 | B_SD13+ | C25 | HB_LED/ | E19 | VDDC | J25 | SerialCLK | N3 | A_SBSY- |
| B6 | B_SD14+ | C26 | VSSC | E20 | MCLK | J26 | VDD_IO | N4 | A_SBSY+ |
| B7 | B_SD15+ | D1 | A_SD11+ | E21 | MAD14 | K1 | VDD_IO | N5 | A_SATN+ |
| B8 | B_SD0- | D2 | VDDC | E22 | MAD11 | K2 | A_SSEL+ | N11 | VSS_IO |
| B9 | B_SD1+ | D3 | VDD_IO | E23 | MAD8 | K3 | A_SCD- | N12 | VSS_IO |
| B10 | B_SD4- | D4 | TRACEPKT0 | E24 | BWE1/ | K4 | A_SCD+ | N13 | VSS_IO |
| B11 | B_SD5- | D5 | PIPESTAT0 | E25 | MAD6 | K5 | A_SIO- | N14 | VSS_IO |
| B12 | B_SD6+ | D6 | VDDC | E26 | VDD_IO | K22 | FLSHALE0/ | N15 | VSS_IO |
| B13 | B_VDDBIAS | D7 | TESTCLKEN | F1 | VDD_IO | K23 | B_LED/ | N16 | VSS_IO |
| B14 | B_SATN- | D8 | B_SD15- | F2 | A_SD11- | K24 | GPIO2 | N22 | SCANEN |
| B15 | B_SBSY+ | D9 | B_SD1- | F3 | SCLK | K25 | GPIO7 | N23 | ZCR_EN/ |
| B16 | B_SMSG- | D10 | B_SD3- | F4 | TRACEPKT7 | K26 | VSS_IO | N24 | AD32 |
| B17 | B_SSEL- | D11 | B_SD5+ | F5 | TRACEPKT2 | L1 | A_SMSG+ | N25 | AD33 |
| B18 | B_SREQ- | D12 | B_SDP0- | F22 | MAD9 | L2 | A_SMSG- | N26 | VDD_IO |
| B19 | B_SD8+ | D13 | B_SATN+ | F23 | MAD1 | L3 | VSS_IO | | |

**Table 5.21 LSI53C1030 Signal List by BGA position (Cont.)**

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|---|---|---|---|---|---|---|---|---|---|
| P1 | VDD_IO | T25 | AD45 | AA5 | RTCK_ICE | AC14 | AD16 | AE8 | GNT/ |
| P2 | VSSC | T26 | AD37 | AA22 | CLKMODE_0 | AC15 | AD17 | AE9 | AD31 |
| P3 | A_SD7+ | U1 | VSS_IO | AA23 | C_BE7/ | AC16 | DEVSEL/ | AE10 | AD29 |
| P4 | A_SDP0- | U2 | A_SD4- | AA24 | PAR64 | AC17 | SERR/ | AE11 | AD26 |
| P5 | A_SDP0+ | U3 | A_SD2+ | AA25 | AD60 | AC18 | AD13 | AE12 | AD25 |
| P11 | VSS_IO | U4 | A_SD3+ | AA26 | VDD_IO | AC19 | AD8 | AE13 | AD21 |
| P12 | VSS_IO | U5 | A_SD3- | AB1 | VDD_IO | AC20 | AD2 | AE14 | AD18 |
| P13 | VSS_IO | U22 | AD55 | AB2 | A_SD13- | AC21 | AD0 | AE15 | IRDY/ |
| P14 | VSS_IO | U23 | AD49 | AB3 | TDI_ICE | AC22 | CLK | AE16 | TRDY/ |
| P15 | VSS_IO | U24 | AD52 | AB4 | TRST_ICE/ | AC23 | GPIO0 | AE17 | PERR/ |
| P16 | VSS_IO | U25 | AD48 | AB5 | VSSC | AC24 | VDD_IO | AE18 | C_BE1/ |
| P22 | AD42 | U26 | VDD_IO | AB6 | TESTACLK | AC25 | C_BE6/ | AE19 | AD14 |
| P23 | AD41 | V1 | VDD_IO | AB7 | VSSC | AC26 | AD61 | AE20 | AD9 |
| P24 | AD39 | V2 | A_SD2- | AB8 | VSSC | AD1 | A_SD12- | AE21 | C_BE0/ |
| P25 | AD38 | V3 | A_SD0+ | AB9 | ALT_INTB/ | AD2 | TDO_ICE | AE22 | AD6 |
| P26 | VSS_IO | V4 | A_SD1- | AB10 | RST/ | AD3 | VDDC | AE23 | AD1 |
| R1 | A_RBIAS | V5 | A_SD1+ | AB11 | AD28 | AD4 | VDD_IO | AE24 | VDDC |
| R2 | A_SD5+ | V22 | AD56 | AB12 | AD24 | AD5 | TST_RST/ | AE25 | GPIO1 |
| R3 | VSS_IO | V23 | AD53 | AB13 | C_BE3/ | AD6 | TDO_CHIP | AE26 | VDD_IO |
| R4 | A_SD7- | V24 | AD54 | AB14 | C_BE2/ | AD7 | VSS_IO | AF1 | VDD_IO |
| R5 | A_SD6+ | V25 | AD51 | AB15 | FRAME/ | AD8 | VDD_IO | AF2 | VSS_IO |
| R11 | VSS_IO | V26 | VSS_IO | AB16 | STOP/ | AD9 | PCI5VBIAS | AF3 | TDI_CHIP |
| R12 | VSS_IO | W1 | A_SDP1+ | AB17 | AD12 | AD10 | REQ/ | AF4 | PVT2 |
| R13 | VSS_IO | W2 | A_SDP1- | AB18 | AD11 | AD11 | VSS_IO | AF5 | VDD_IO |
| R14 | VSS_IO | W3 | VSS_IO | AB19 | AD5 | AD12 | VDD_IO | AF6 | VSS_IO |
| R15 | VSS_IO | W4 | A_SD0- | AB20 | ACK64/ | AD13 | AD22 | AF7 | ALT_INTA/ |
| R16 | VSS_IO | W5 | A_SD15+ | AB21 | VDDA | AD14 | VSSC | AF8 | AD30 |
| R22 | AD43 | W22 | AD63 | AB22 | PCI5VBIAS | AD15 | VSS_IO | AF9 | VDD_IO |
| R23 | AD40 | W23 | AD59 | AB23 | VSSC | AD16 | VDD_IO | AF10 | VSS_IO |
| R24 | VDD_IO | W24 | VDD_IO | AB24 | VSSC | AD17 | AD15 | AF11 | AD20 |
| R25 | AD44 | W25 | PCI5VBIAS | AB25 | AD62 | AD18 | PCI5VBIAS | AF12 | PCI5VBIAS |
| R26 | AD36 | W26 | AD50 | AB26 | VSS_IO | AD19 | VSS_IO | AF13 | VDD_IO |
| T1 | A_VDDBIAS | Y1 | A_SD15- | AC1 | A_SD12+ | AD20 | VDD_IO | AF14 | VSS_IO |
| T2 | A_SD5- | Y2 | A_SD14+ | AC2 | CLKMODE_1 | AD21 | AD4 | AF15 | VDDC |
| T3 | VDD_IO | Y3 | VDD_IO | AC3 | VSS_IO | AD22 | REQ64/ | AF16 | AD19 |
| T4 | A_SD4+ | Y4 | IDDTN | AC4 | DIS_ | AD23 | VSS_IO | AF17 | VDD_IO |
| T5 | A_SD6- | Y5 | TMS_ICE | | SCSI_FSN/ | AD24 | VSSA | AF18 | VSS_IO |
| T11 | VSS_IO | Y22 | PCI5VBIAS | AC5 | IOPD_GNT/ | AD25 | VDDC | AF19 | PAR |
| T12 | VSS_IO | Y23 | C_BE5/ | AC6 | TCK_CHIP | AD26 | C_BE4/ | AF20 | AD10 |
| T13 | VSS_IO | Y24 | VSS_IO | AC7 | VDDC | AE1 | VSS_IO | AF21 | VDD_IO |
| T14 | VSS_IO | Y25 | AD58 | AC8 | INTA/ | AE2 | TESTHCLK | AF22 | VSS_IO |
| T15 | VSS_IO | Y26 | AD57 | AC9 | NC | AE3 | VDDC | AF23 | AD7 |
| T16 | VSS_IO | AA1 | VSS_IO | AC10 | PCI5VBIAS | AE4 | TMS_CHIP | AF24 | AD3 |
| T22 | AD47 | AA2 | A_SD14- | AC11 | AD27 | AE5 | PVT1 | AF25 | VDD_IO |
| T23 | AD46 | AA3 | A_SD13+ | AC12 | AD23 | AE6 | PCI5VBIAS | AF26 | VSS_IO |
| T24 | VSS_IO | AA4 | TCK_ICE | AC13 | IDSEL | AE7 | INTB/ | | |

## Figure 5.13 456-Pin EPBGA (KY) Mechanical Drawing




**Important:** **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code KY.**

# Appendix A
# Register Summary

Tables A.1, A.2, and A.3 provide a register summary.

**Table A.1 LSI53C1030 PCI Registers**

| Register Name | Offset[1] | Read/Write | Page |
|---|---|---|---|
| Vendor ID | 0x00–0x01 | Read Only | 4-3 |
| Device ID | 0x02–0x03 | Read Only | 4-3 |
| Command | 0x04–0x05 | Read/Write | 4-3 |
| Status | 0x06–0x07 | Read/Write | 4-5 |
| Revision ID | 0x08 | Read/Write | 4-7 |
| Class Code | 0x09–0x0B | Read Only | 4-7 |
| Cache Line Size | 0x0C | Read/Write | 4-7 |
| Latency Timer | 0x0D | Read/Write | 4-8 |
| Header Type | 0x0E | Read Only | 4-8 |
| Reserved | 0x0F | Reserved | 4-9 |
| I/O Base Address | 0x10–0x13 | Read/Write | 4-9 |
| Memory [0] Low | 0x14–0x17 | Read/Write | 4-10 |
| Memory [0] High | 0x18–0x1B | Read/Write | 4-10 |
| Memory [1] Low | 0x1C–0x1F | Read/Write | 4-11 |
| Memory [1] High | 0x20–0x23 | Read/Write | 4-11 |
| Reserved | 0x24–0x27; 0x28–0x2B | Reserved | 4-12 |
| Subsystem Vendor ID | 0x2C–0x2D | Read Only | 4-12 |
| Subsystem ID | 0x2E–0x2F | Read Only | 4-13 |

**Table A.1 LSI53C1030 PCI Registers (Cont.)**

| Register Name | Offset[1] | Read/Write | Page |
|---|---|---|---|
| Expansion ROM Base Address | 0x30–0x33 | Read/Write | 4-14 |
| Capabilities Pointer | 0x34 | Read Only | 4-15 |
| Reserved | 0x35–0x37; 0x38–0x3B | Reserved | 4-16 |
| Interrupt Line | 0x3C | Read/Write | 4-16 |
| Interrupt Pin | 0x3D | Read Only | 4-16 |
| Minimum Grant | 0x3E | Read Only | 4-17 |
| Maximum Latency | 0x3F | Read Only | 4-17 |
| Power Management Capability ID | — | Read Only | 4-18 |
| Power Management Next Pointer | — | Read Only | 4-18 |
| Power Management Capabilities | — | Read Only | 4-18 |
| Power Management Control/Status | — | Read/Write | 4-19 |
| Power Management Bridge Support Extensions | — | Read Only | 4-20 |
| Power Management Data | — | Read Only | 4-21 |
| MSI Capability ID | — | Read Only | 4-21 |
| MSI Next Pointer | — | Read Only | 4-21 |
| Message Control | — | Read/Write | 4-22 |
| Message Address | — | Read/Write | 4-23 |
| Message Upper Address | — | Read/Write | 4-23 |
| Message Data | — | Read/Write | 4-24 |
| PCI-X Capability ID | — | Read Only | 4-24 |
| PCI-X Next Pointer | — | Read Only | 4-25 |
| PCI-X Command | — | Read/Write | 4-25 |
| PCI-X Status | — | Read/Write | 4-27 |

1. The offset of the PCI extended capabilities registers can vary. Access these registers through the Next Pointer and Capability ID registers.

**Table A.2 LSI53C1030 PCI I/O Space Registers**

| Register Name | Offset | Read/Write | Page |
|---|---|---|---|
| System Doorbell | 0x00 | Read/Write | 4-31 |
| Write Sequence | 0x04 | Read/Write | 4-31 |
| Host Diagnostic | 0x08 | Read/Write | 4-32 |
| Test Base Address | 0x0C | Read/Write | 4-34 |
| Diagnostic Read/Write Data | 0x10 | Read/Write | 4-34 |
| Diagnostic Read/Write Address | 0x14 | Read/Write | 4-35 |
| Reserved | 0x18–0x2F | Reserved | – |
| Host Interrupt Status | 0x30 | Read/Write | 4-36 |
| Host Interrupt Mask | 0x34 | Read/Write | 4-37 |
| Reserved | 0x38–0x3F | Reserved | – |
| Request FIFO | 0x40 | Read/Write | 4-38 |
| Reply FIFO | 0x44 | Read/Write | 4-38 |

**Table A.3 LSI53C1030 PCI I/O Space Registers**

| Register Name | Offset | Read/Write | Page |
|---|---|---|---|
| System Doorbell | 0x00 | Read/Write | 4-31 |
| Write Sequence | 0x04 | Read/Write | 4-31 |
| Host Diagnostic | 0x08 | Read/Write | 4-32 |
| Test Base Address | 0x0C | Read/Write | 4-34 |
| Reserved | 0x10–0x2F | Reserved | – |
| Host Interrupt Status | 0x30 | Read/Write | 4-36 |
| Host Interrupt Mask | 0x34 | Read/Write | 4-37 |
| Reserved | 0x38–0x3F | Reserved | – |
| Request FIFO | 0x40 | Read/Write | 4-38 |
| Reply FIFO | 0x44 | Read/Write | 4-38 |

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## V



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## Z

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