LSI403Z Digital Signal Processor

ZSP™ ARCHITECTURE PERFORMANCE WITH HIGH-END INTEGRATION

OVERVIEW

The LSI403Z is a low power 16-bit fixed-point digital signal processor (DSP) based on the LSI Logic ZSP400 DSP core. The device has been designed for applications requiring high throughput and flexibility coupled with a high speed I/O, such as Voice over Networks CPE/IAD devices and audio applications. The LSI403Z is capable of a maximum clock rate of 150 MHz for 600 MIPS peak performance and sustained effective throughput of 300 DSP MIPS (MACs). The device is also software compatible with all other products in the ZSP architecture, and offers an unrivalled combination of code density, performance and ease of use.

MEMORY

The internal memory structure of the LSI403Z comprises of 16K words of on-chip instruction memory, 16K words of on-chip data memory, 2K words on-chip boot ROM, and on-chip peripherals. Additionally, the boot ROM provides start-up and self-test capabilities. Both synchronous and asynchronous devices are supported including sync-burst SRAM. The external memory is logically segmented into instruction, data, and peripheral spaces.

DMA

The DMA controller of the LSI403Z supports zero-overhead instruction or data transfers to or from the entire 32K words of internal RAM to the memory interface unit, host processor interface, or serial ports. The eight DMA channels are segmented between four "indexed" and four "non-indexed" channels. Indexed channels have the ability to multiplex and de-multiplex data. Indexed channels can also operate in non-indexed mode.

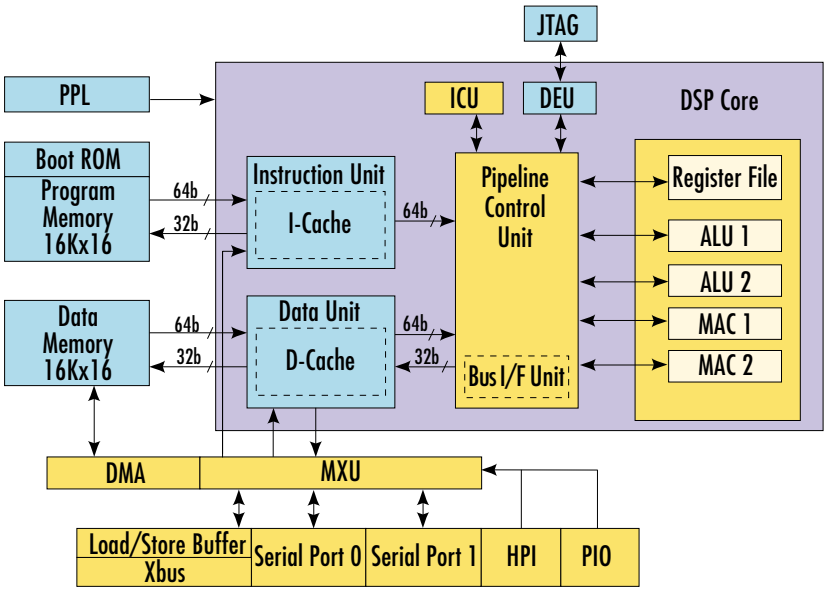

Figure 1. LSI403Z Functional Block Diagram

FEATURES

- 150 MHz operation at 1.8V
- 2 high-speed serial/TDM ports (T1/E1 framer, H.100/H.110 bit stream compatible)
- Low power modes
- 32K words on-chip RAM, 2K words on-chip ROM
- 8-channel DMA controller
- On-board PLL for clock generation
- 32-/16-bit external memory interface
- 2 on-board timers
- IEEE 1149.1-compliant JTAG port for real-time emulation

BENEFITS

- 300 MMAC sustained DSP performance at 150 MHz
- Direct interfacing to standard telecommunications interfaces, reducing system cost
- High data throughput without processor overhead
- Low power per channel
- Flexibility to optimize power consumption
- High data bandwidth to off-chip devices
- RTOS support and increased system integration
- Low overhead on chip debug
- Ideal for Voice over DSL IAD designs

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TIMERS

The LSI403Z has two identical 16-bit on board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit prescaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

TDM SERIAL PORTS

The LSI403Z provides two identical synchronous serial ports that support 8- or 16-bit active or passive transfers, which can be either burst or continuous. It a maximum transfer rate in either active or passive mode of one-half the processor clock rate. Both serial ports provide the programmable feature of a TDM (time division multiplex) mode that is compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals.

HOST PROCESSOR INTERFACE (HPI)

The Host Processor Interface, or HPI, is an asynchronous 8-bit parallel port that is used to interface with off-chip devices. It is compatible with both Motorola and Intel style memory interfaces, and supports word transfers. The maximum transfer rate for the HPI is one-forth of the processor clock frequency.

DEVELOPMENT TOOLS

The LSI403Z is fully supported by both LSI Logic and third party commercial tools. LSI Logic provides a GNU-based compiler, linker and assembler available for Windows and Solaris platforms. The compiler supports C fixed-point data types and employs a variety of C intrinsic functions. Also supported is a full commercial tool chain from GreenHills Software and Corelis JTAG debug tools. The ZSP architecture enables the C compiler to produce code unrivaled in code density and execution speed by any DSP in its class, offering a fast time to market with optimal performance and cost.

An LSI403Z evaluation board, the EB403, is available offering the following features:

- 32-bit PCI interface provides JTAG debug capabilities
- 16-bit A/D converter on board
- Reference board with the ability to handle multiple voice channels
- Programmable Gain Amplifier

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