LSI401Z Digital Signal Processor

Leading-edge Superscalar DSP Technology

Overview

The LSI401Z is a high-performance 16-bit fixed-point digital signal processor (DSP) based on the ZSP™ Architecture. This device has been designed for applications that require high data throughput capacity coupled with high-speed I/O, such as communications infrastructure equipment, and offers enhanced I/O capabilities and on-chip memory. The LSI401Z is capable of a maximum clock rate of 200 MHz for 800 MIPS peak performance and sustained effective throughput of 400 DSP MIPS (MACs).

Memory

The internal memory structure of the LSI401Z comprises 48K words of dual-access RAM, 2K words of boot ROM and 2K words of data space dedicated to memory-mapped registers and external peripherals. Up to 40K words of the dual-access RAM can be used for instruction memory and up to 48K words for data memory. The boot ROM contains several routines, including internal self-test, on-chip debug support code, and boot-loader routines. The Memory Interface Unit (MIU) provides a glueless interface to industry-standard 16-bit asynchronous SRAMs and ROM devices, and/or to user-defined peripherals, and allows expansion of instruction and data space to 128K words.

DMA

The single-channel DMA controller of the LSI401Z can transfer either instructions or data from the internal memory space to or from the MIU, HPI, or either serial port. Zero-overhead data transfers are made from a dedicated area of internal dual-access RAM to these peripherals. The DMA controller has dedicated buses to access a maximum of 8K words of dual-access RAM so that no cycle stealing is required for these data transfers.
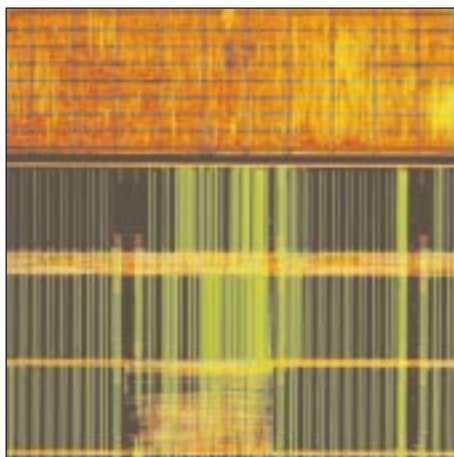
LSI401Z available in 0.25 μm technology.

Features

- 200 MHz operation at 2.5 V (5 ns cycle time)
- On-board PLL for clock generation
- 48K words RAM, 2K words ROM on-chip
- DMA support for fast I/O transfers without cycle stealing
- 16-bit external memory interface
- Two on-board timers
- Two high-speed synchronous serial ports
- 16-bit host processor interface
- Four-pin programmable I/O port
- IEEE 1149.1-compliant JTAG port for real-time emulation and system download
- 208 MBGA package

Benefits

- 400 MMAC sustained DSP performance
- Flexibility to optimize power consumption
- Reduced system memory cost
- High data throughput without processor overhead
- High data bandwidth to off-chip devices
- RTOS support and increased system integration
- High-speed link to I/O data streams
- Simple interfacing to industry-standard micros
- Flexibility for direct control of off-chip devices
- Low overhead on chip debug
- Very high processing density per unit area

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Timers

The LSI401Z has two identical 16-bit on-board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit pre-scaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

Synchronous Serial Ports

The device provides two identical synchronous serial ports that support 8- or 16-bit active or passive transfers. Transfers can be either burst or continuous, depending on whether data transfer is intermittent or in a continuous bit stream. The maximum transfer rate in active mode is 100 Mbps given a 200 MHz processor clock frequency. In passive mode, the maximum transfer rate is 200 Mbps.

Host Processor Interface (HPI)

The Host Processor Interface, or HPI, is an asynchronous 16-bit parallel port that is compatible with both Motorola and Intel style interfaces, and supports word (16-bit) transfers. The maximum transfer rate for the HPI is half of the processor clock frequency (100M words per second given a processor operating frequency of 200 MHz).

Development Tools

The ZSP Processor family is fully supported by a GNU-based compiler, linker and assembler, available for Windows 95/98/NT and Solaris 2 platforms. The ZSP Architecture enables the C compiler to produce code unrivaled in code density and execution speed by any DSP in its class, offering fast time to market with optimal performance and cost. An integrated debug environment is available for PC platforms.

An LSI401Z development platform is available, offering the following features:

- FLASH EPROM
- RS232C and JTAG-based host communication and code download
- 128K words asynchronous program/data memory
- Dual audio codecs