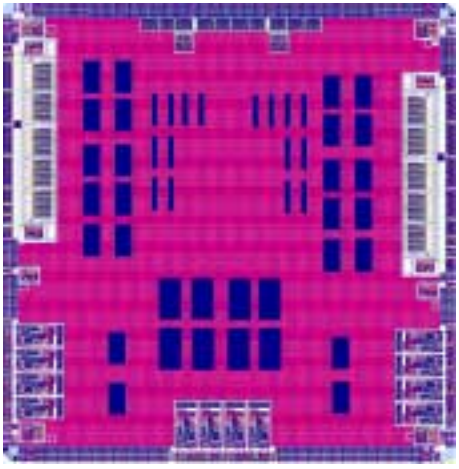
RapidChip™ L79301 StreamSlice™ Configurable 10 Gbit/s Platform

Advance Datasheet

The StreamSlice L79301 (Figure 1) is the first platform of the LSI Logic RapidChip configurable-logic family. It greatly reduces the NRE and development costs usually associated with cell-based logic, while maintaining a significant cost advantage over FPGAs. The L79301 provides the diffused cores needed for high-speed networking applications along with a large amount of customer-configurable logic. There are 12 GigaBlaze® channels operating at 1.0625 Gbit/s to 3.1875 Gbit/s each, 40 HyperPHY channels operating at 622 Mbits/s to 832 Mbits/s each, and an 80-bit DDR interface. The device also contains 2.2 Mbits of embedded memory and 3 million gates of customer-configurable logic.

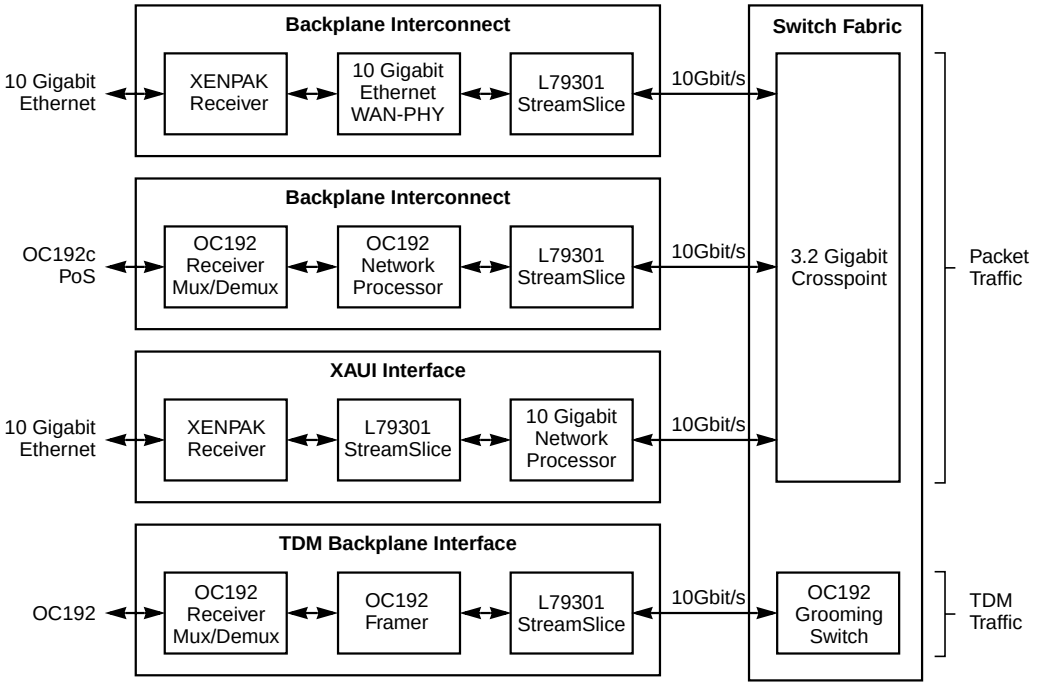
LSI Logic Corporation provides RapidReady™ CoreWare® and IP blocks that combine the diffused-embedded cores with the configurable logic to address a number of high-performance and standards-based applications. These include the10 Gbit Ethernet XGXS, SPI4.2 interface, DDR-SDRAM controller, and others. In addition, customers can add their own IP for differentiation. The combination of diffused and soft IP, along with LSI Logic sophisticated RapidChip methodology makes it easy to generate a set of metal layers implementing a customer's unique system on a chip.

Figure 1 L79301 StreamSlice Configurable Platform



The StreamSlice platform provides a basis for a wide range of differentiated designs. As shown in Figure 2, StreamSlice can be configured for specific roles on different linecards within the same system. These applications are suitable to any high-throughput data communication system (Router, Switch, or Aggregation System).

Figure 2 Typical L79301 StreamSlice Applications



StreamSlice Features

- ASIC performance
- Quick turnaround to market
- Three million gates of configurable logic. Configuration is in five layers of metal
- 12 Ultra-high speed GigaBlaze SERDES serial interfaces
  - Data rate: 1.0625 Gbit/s to 3.1875 Gbit/s each
  - Point to point full duplex

  - Programmable internal impedance for matching to external devices
  - XAUI, Gigabit Ethernet, and Fibre Channel compliant
- 40 HyperPHY high-speed interfaces
  - 622-Mbits/s to 832 Mbits/s each
  - Full duplex operation
  - Typical 85 mW per channel @ 622 Mbits/s
  - Receives data reliably even with long sequences of data without transitions
  - Supports SPI4 Phase 2
- 80-Bit DDR SDRAM interface
  - High-performance 333 Mbits/s per pin
  - Delay-time settings in increments of 20 ps
  - Internal scan
  - Supports point to point and Multi-drop configurations
- 6 PLLs
  - Four @ 100 MHz to 500 MHz
  - Two @ 600 MHz to 1250 MHz
- 2.2 Mbit Diffused SRAM
- 333 user configurable I/Os
- 0.18-micron process: 1.8 V
- 1509-pin FPBGA FlipChip™

Overview

The L79301 consists of three million usable gates of configurable logic embedded with a set of diffused cores. The cores are

- 12 GigaBlaze high-speed serial channels operating between 1.0625 Gbits/s and 3.1875 Gbits/s
- 40 HyperPHY channels operating at 622-Mbits/s to 832-Mbits/s
- an 80-bit DDR interface

- dual-port SRAM
- single-port SRAM
- 6 PLLs

The cores are not configurable.

Customizable Logic Fabric

The Transistor Fabric provides the basis for the implementation of the user's logic. An R-Cell is the basic unit within the Transistor Fabric; it is made up of specially sized "N" and "P" type transistors for maximum flexibility and performance. R-Cells are diffused in a regular pattern throughout the slice and can implement memory as well as logic structures efficiently. They are configured in up to five layers of metal to create the full range of logic functions available within the RapidChip logic cell library. The library contains over 400 cells, with a range of drive strengths. R-Cells can also be configured efficiently as small memory blocks, further adding flexibility to a designer's memory implementation. Transistors within the Fabric are activated only when they are part of the implementation of a function used in the design, ensuring the most power-efficient solution.

The L79301 contains 3 million gates of user-configurable logic. The maximum frequency for user logic is 166 MHz.

Configurable I/Os

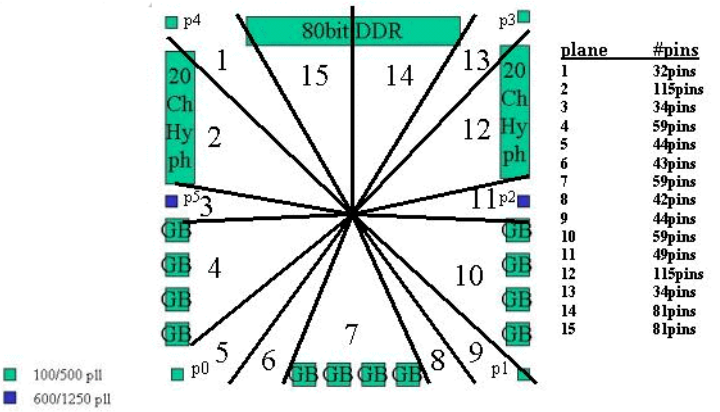
The L79301 provides designers with access to a broad range of user-configurable I/O types. Configured by patterning of metal interconnect, the I/O buffers are compact yet address the majority of industry-standard applications without overheads associated with reprogrammability.

Through optimization of package power domains and slice-specific VDD/VSS placements, the configuration I/O resources enable designers to assign buffers with fine granularity. The I/O power plane grouping are partitioned to a set a banks as illustrated in Figure 3. All I/Os within a bank share the same VDD. Table 1 lists the available I/O bus types and drive strengths for I/Os

Table 1 I/O Configuration List

I/O Signaling Standard	Type	VDD	Drive Strength
(CMOS) LVTTL	Bidirectional	3.3 V	12 mA
	Bidirectional	3.3 V	8 mA
	Bidirectional	3.3 V	4 mA
	Bidirectional	3.3 V	2 mA
	Bidirectional	2.5 V	12 mA
	Bidirectional	2.5 V	8 mA
	Bidirectional	2.5 V	4 mA
	Bidirectional	2.5 V	2 mA
	Bidirectional	1.8 V	12 mA
	Bidirectional	1.8 V	8 mA
	Bidirectional	1.8 V	4 mA
	Bidirectional	1.8 V	2 mA
	Bidirectional Differential	2.5 V	50 Ω
SSTL-2	Bidirectional	2.5 V	Class I
	Bidirectional	2.5 V	Class II
LVDS	Differential Output	2.5 V	4 mA
	Differential Input	2.5 V	
HSTL- Single Ended	Bidirectional	1.5 V	Class I (8 mA)
	Bidirectional	1.5 V	Class II (16 mA)
	Bidirectional	1.5 V	Class III (24 mA)
LVPECL	Input	3.3 V	
PCI-66	Bidirectional	3.3 V	

Figure 3 Power Plane Groupings



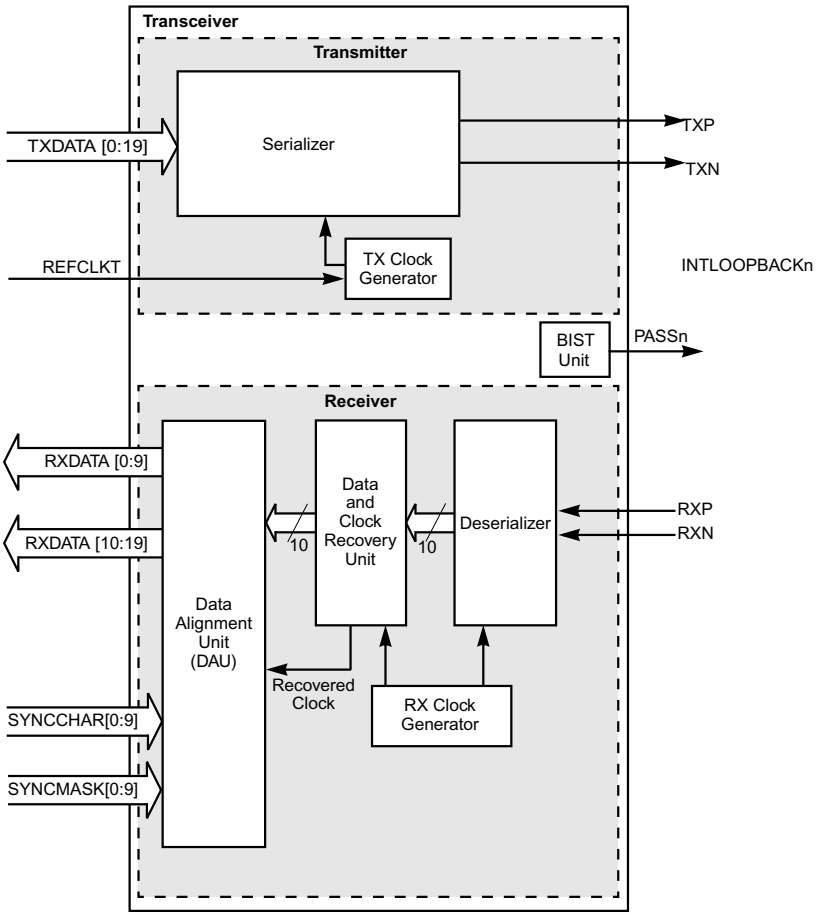
plane	#pins
1	32pins
2	115pins
3	34pins
4	59pins
5	44pins
6	43pins
7	59pins
8	42pins
9	44pins
10	59pins
11	49pins
12	115pins
13	34pins
14	81pins
15	81pins

GigaBlaze

The GigaBlaze SERDES transceivers provide point-to-point serial communications links that operate between 1.0625 Gbits/s and 3.1875 Gbits/s. There are 12 GigaBlaze channels. Each channel transfers data between a 20-bit bus that is internal to the device and a differential serial pair I/O. The clock rate is 1/20 the serial data rate. Thus for 3.125 Gbits/s, the clock frequency is 156.25 MHz. Receiver clock recovery and synchronization are included. Testability and debugging capability are provided by BIST and various loop backs.

The serial I/O is composed of a transmit differential pair and a serial differential pair. The transmit signal ranges from 1 V p/p to 2.4 V p/p. Also, the device can be programmed to add up to 38% pre-emphasis to the signal. In typical applications, the receive I/O pair is AC coupled. Both the transmit and receive I/Os have programmable internal terminations to match the signal traces. Figure 4 is a block diagram of a typical GigaBlaze Transceiver core.

Figure 4 Typical GigaBlaze Core



Because the transmitter and receiver operate independently, the GigaBlaze SERDES transceiver can send and receive data simultaneously. Also, the transmitter and receiver can operate at different data transfer rates. It transmits data at a rate controlled by the Reference Clock (REFCLKT). The transmitter accepts 20-bit parallel data (TXDATA[19:0] clocked in on REFCLKT. It serializes and transmits the data at 20 times the REFCLKT frequency. The serial bit stream is transmitted in non-return-to-zero (NRZ) format on the differential pair (TXP, TXN).

The receive buffer accepts a 1.0625 to 3.1875 Gbit/s serial bit stream from the differential pair (RXP, RXN). It deserializes the bit stream, and recovers the embedded clock (RBC) and the parallel data. The recovered parallel data is output on the 20-bit RXDATA bus at the RBC frequency which is 1/20 the serial data rate. The receiver can optionally align RXDATA to a selectable synchronization pattern. Control inputs to the receiver can select the synchronization pattern. The complementary recovered clock outputs (RBC[0:1]) can be used by other logic to clock the output on the RXDATA bus.

To facilitate testing and system bring-up, the GigaBlaze SERDES transceiver includes

- two internal serial loopback paths from TXP/TXN to RXP/RXN
- an internal serial reverse loopback path from RXP/RXN to TXP/TXN
- an internal parallel wrap back from the transmitter's input parallel data to the receiver's data alignment unit (DAU)
- full scan to achieve high fault coverage in the transceiver's digital section
- a BIST unit that tests digital and analog sections

Through the internal loopback/wrap back or an external link, the BIST unit can transmit test patterns, compare them with received patterns, and alert external logic if there is a mismatch. With standards-compliant GigaBlaze SERDES transceivers, designers also benefit from the LSI Logic CoreWare library of link layer functions. The combination provides a low-risk route to enabling fully compliant 10 GigaBit Ethernet, Fibre Channel, and other applications.

The key features of the GigaBlaze SERDES transceiver are

- serial transfer rates up to 3.1875 Gbits/s with a bit error rate less than 10^{-12}
- standards support for Fibre Channel, Gigabit Ethernet, and XAUI
- full-duplex operation: the transmitter and receiver can work at different data rates
- internal serial loopback, digital parallel wrap back, BIST, and full scan to facilitate testing

- Adjustable differential output swing for driving coaxial and twinaxial cables, or a fibre optic transmitter
- Low-swing differential input sensitivity
- Support for standard serial line impedances of 50Ω and 75Ω (100Ω and 150Ω differential) with internal termination

GigaBlaze provides the physical layer for standard high-speed communications protocols such as Fibre Channel, Infiniband, Gigabit Ethernet, and 10 Gigabit Ethernet.

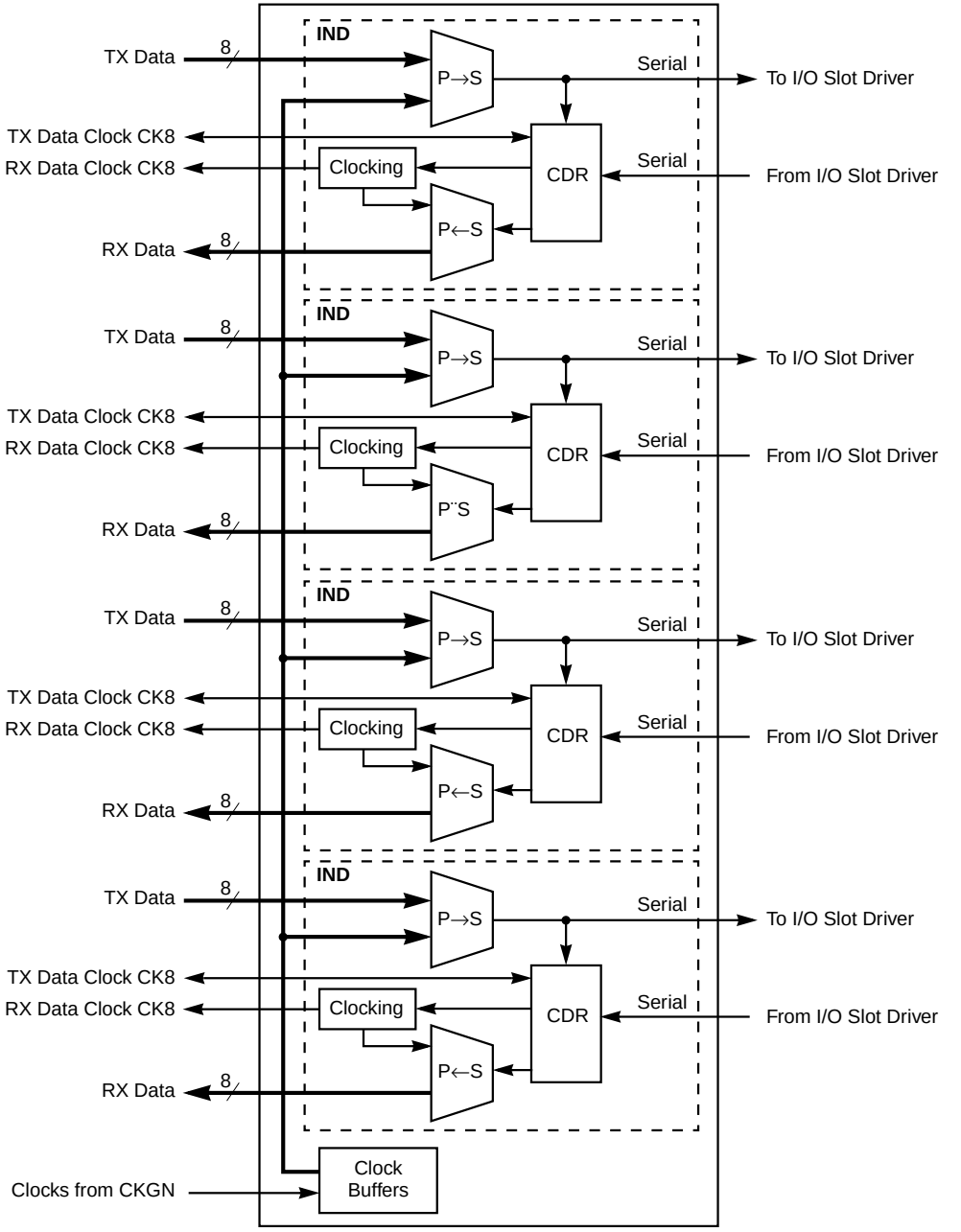
For more information on the G12 GigaBlaze (CW000504), please refer to the *GigaBlaze G12 Revision 2.x Core Design Manual.*

HyperPHY

HyperPHY channels provide point to point communications links that operate between 622-Mbits/s and 832-Mbits/s. There are two banks of 20 HyperPHY channels. Each channel transfers data between an 8-bit bus that is internal to the device and a differential serial pair I/O. Clock recovery and synchronization are included. The HyperPHY channels are connected to the I/O via LVDS buffers.

Each bank has five CW108005_ind4 cores and one cw108005_ckgen core. The cw108005_ind4 core is composed of four HyperPHY channels. The cw108005_ckgn core accepts clocks from a high-speed PLL, and creates buffered and aligned clocks for use by the IND4 cores. Figure 5 illustrates a HyperPHY hookup.

Figure 5 HyperPHY IND4 Block Diagram



The HyperPHY banks can be used to implement SPI4 Phase 2.

The key features of the HyperPHY cores are

- supports OC-12/STM-4 data rate
- supports SPI4 Phase 2 standard
- receives serial data at rates from 622 Mbits/s to 832 Mbits/s and de-multiplexes to an 8-bit word with associated clock
- multiplexes an 8-bit word with associated clock and transmits serial data at rates from 622 Mbits/s to 832 Mbits/s
- typical 85 mW per full duplex channel at 622 Mbps including LVDS I/Os
- at-speed built-in-self-test of full transmit and receive/clock recovery functions
- able to receive data reliably even with long sequences of data without transitions
- LVDS buffers
- 1.8 V supply

For more information on the G12® Standard HyperPHY (*CW108005)* please refer to the *G12-p CW108002 HyperPHY CMOS Independent Channel Transceiver Design Manual*

DDR

There is one 80-bit DDR interface block. It consists of configurable I/O buffers, ten 8-bit datapath hardmacs, and two master delay hardmacs. The I/Os are suitable for both single-point and multipoint applications. The datapath hardmacs provide data, clock, and control signals. The master delay hardmacs are optimized to meet the critical timing requirements of the early and late clocks and thus to detect early and late data.

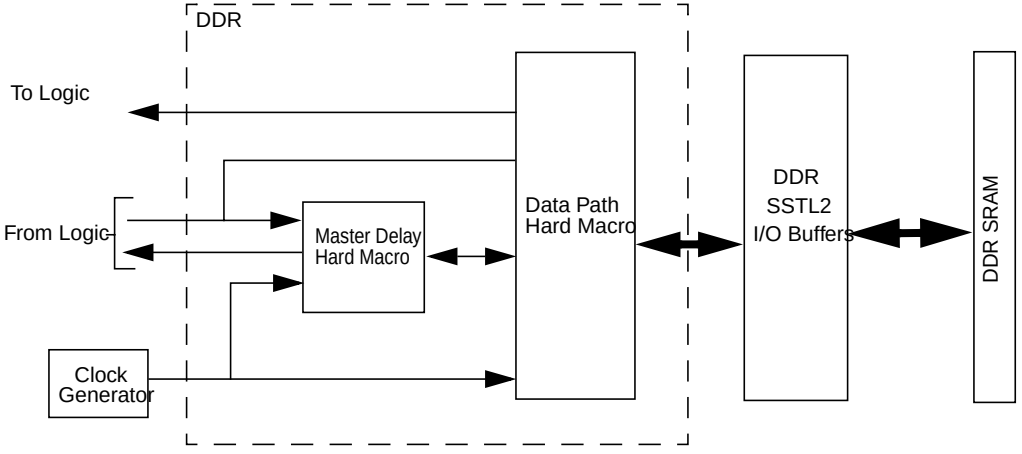
In designs using the DDR interface, the corresponding configurable I/Os operate in the SSTL2 mode. Otherwise, they are available as general-purpose I/Os and can be configured onto any of the available modes. Figure 6 shows the DDR Core hardmacros.

The key features of the DDR PHY resources are

- 80-bit wide DDR PHY data path
- 166 MHz operation for data transfer rates up to 333 Mbits/s
- internal scan
- memory controller interfaces for 4-, 8-, 16-, and 32-bit DDR SDRAM/FCRAM configurations
- burst lengths of 2, 4, and 8
- self-test
- programmable delay of data strobe for read operations
- Digital Delay Locked Loop (DDLL) to maintain constant programmable delay over PVT
- 2X clock architecture to ensure 90-degree phase shift for DQS during write cycle

For more information on the G12 DDR (CW000701), please refer to the *G12 DDR Core Design Manual*.

Figure 6 Typical DDR Core Hardmacros



Diffused Memories

The L79301 has several banks of diffused SRAM. Although these are in diffused configurations, the tool GENMEN allows the user to reconfigure the memory to meet their requirements. In addition, GENMEM can configure R Cells to act as memory cells if additional memory is required. Table 2 lists the memory banks.

Table 2 Memory Banks

Mem.	Size	Ports	# Banks
rr2kx72_1rw	2K X 72	1 R/W Port	8
rr256x36_1r1w	256 X 36	1 R Port / 1 W Port	16
rr1kX36_1r1w	1K X 36	1 R Port / 1 W Port	24

PLL Resources

The L79301 contains six fully integrated, wide-range PLLs: two high-range PLLs and four standard PLLs. The output frequency range of the standard PLLs is 100 MHz to 500 MHz and the high range PLL's output frequency range is 600 MHz to 1250 MHz. The external reference clock for each PLL can be either single-ended or differential and has dedicated impedance-controlled traces assigned within the slice's package.

Programmable charge pump settings allow stable operation and acceptable bandwidths to be achieved for frequency multiplication as high as M = 32 (standard PLL) or M = 64 (high-range PLL). Both PLL types employ a differential VCO powered by an integrated self-referenced voltage regulator for reduced susceptibility to supply noise. They are powered through a 1.8 V supply voltage.

For more information on the G12 PLL (pll12pipw100500), please refer to the *G12 Cell-Based ASIC Products-I/Os, Memories, and Special Cells Databook*

Test

An IEEE 1149.1 JTAG interface is provided on the StreamSlice platform allowing manufacturing test, boundary scan and access to Built In System Test (BIST) routines. An interface is provided to allow user register customization to enable access to internal register space to allow for register initialization, design verification and debug.

Specifications

Recommended Operating Conditions

Table 3 gives the recommended operating conditions for the L79301

Table 3 Recommended Operating Conditions[1]

Symbol	Parameter	Minimum	Typical.	Maximum	Unit
V_{DD}	DC Supply Voltage[2]	1.62	1.80	1.89	V
V_{DDGB}	GigaBlaze Supply Voltage	1.62	1.80	1.89	V
V_{DDHP}	HyperPHY Supply Voltage	1.62	1.80	1.89	V
V_{DD15}	1.5 V I/O Supply Voltage	1.42	1.50	1.58	V
V_{DD18}	1.8 V I/O Supply Voltage	1.68	1.80	1.89	V
V_{DD25}	2.5 V I/O Supply Voltage	2.37	2.5	2.63	V
V_{DD33}	3.3 V I/O Supply Voltage	3.13	3.3	3.46	V

1. For normal device operation, adhere to the limits in this table. Device functionality to stated DC and AC operation are not guaranteed if conditions exceed recommended operating conditions.

2. Core Supply Voltage (1.80 V Nominal)

DC Electrical Characteristics

TBD

AC Electrical Characteristics

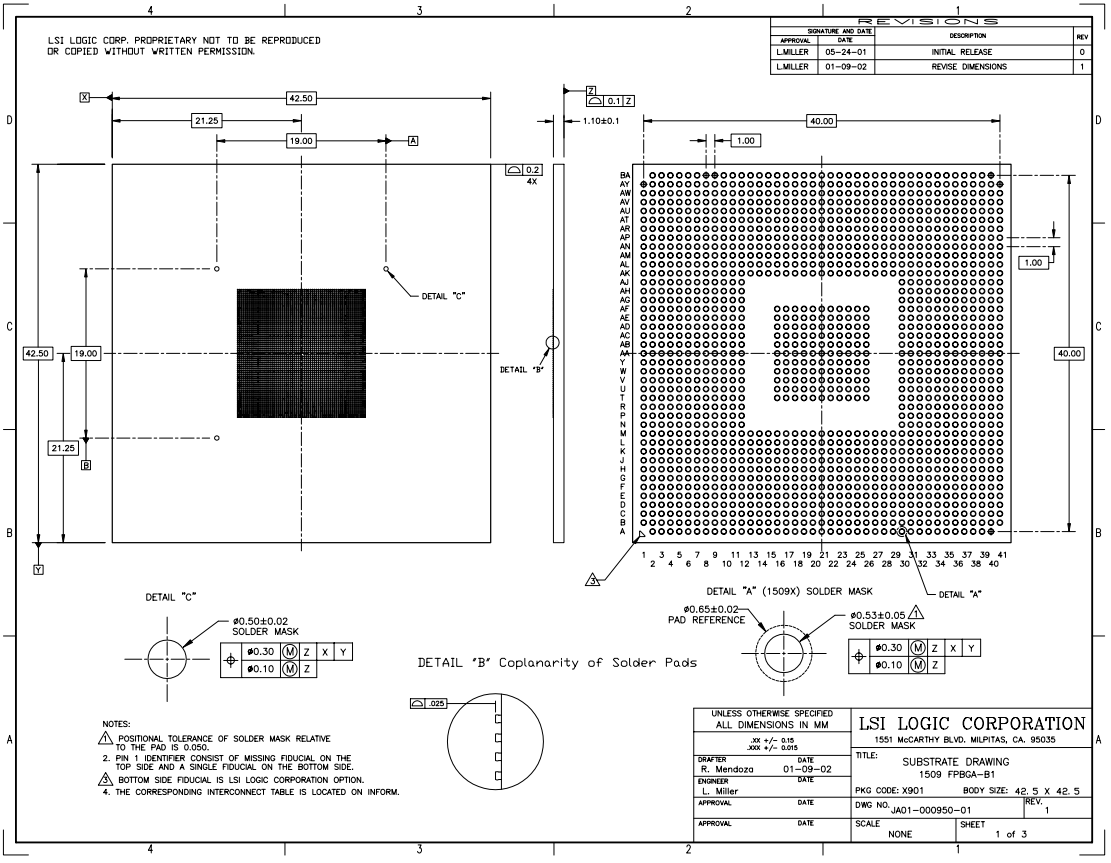
Table 4 TBD

Pin List and Package Information

Table 5 lists the L79301 pins and Figure 7 is a mechanical drawing of the package.

Table 5 L69301 StreamSlice Platform Pin List (TBD)

Figure 7 1509-pin FPBGA



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code X901.**

Related Documents

G12®-p CW108002 HyperPHY® CMOS Independent Channel Receiver Design Manual

GigaBlaze G12 Core Rev. 2.x Design Manual

DDR Core (CW000701_2_0) Design Manual

G12 Cell-Based ASIC Products-I/Os, Memories, and Special Cells Databook

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