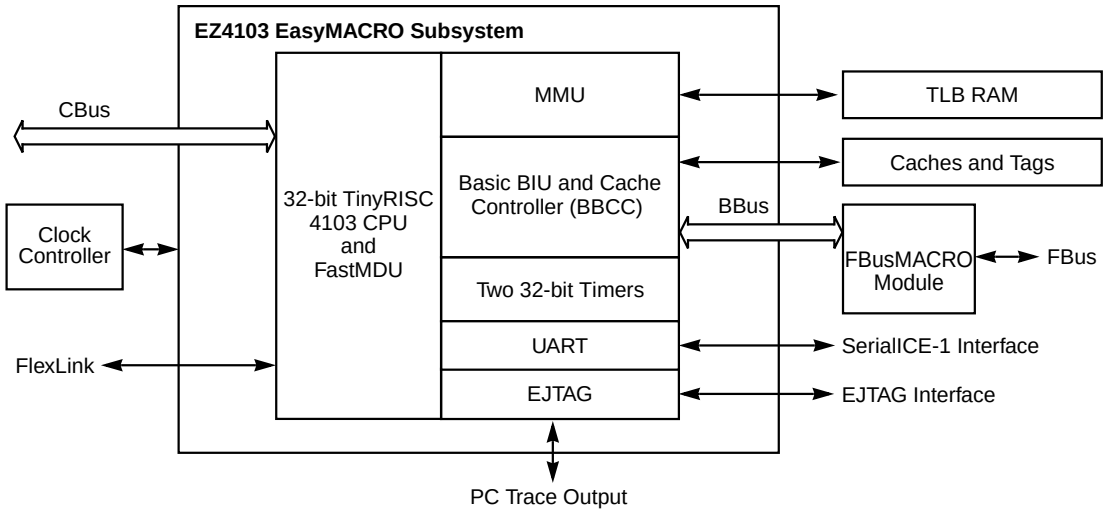
TinyRISC® EZ4103 EasyMACRO Microprocessor

Preliminary Datasheet

The TinyRISC® EZ4103 EasyMACRO subsystem is a compact, high-performance, 32-bit MIPS microprocessor subsystem implemented in the LSI Logic G12™-p technology. The EZ4103 CPU implements the MIPS II instruction set and MIPS16 Application Specific Extensions. The EZ4103 combines the TinyRISC CPU with the most commonly used blocks (such as a bus controller, MMU, and EJTAG) to simplify system-on-a-chip design and reduce time to market. A bus controller module (FBusMACRO) and RAMs are also available from LSI Logic to help speed your CoreWare® design.

The EZ4103 is especially suited for cost-sensitive, low-power embedded applications. The TinyRISC CPU performs code compression and accepts both 16-bit and 32-bit instructions. Figure 1 shows the EZ4103 and how it interfaces with system logic in a typical design.

Figure 1 EZ4103 in a Typical System



Powered by 1.8 V, the EZ4103 has a 120 MHz (worst-case conditions) clock speed with a performance of 120 MIPS peak and 96 MIPS sustained. The EZ4103 uses G12-p technology and implements a full-scan methodology to achieve very high fault coverage.

EZ4103 Overview and Features

Components

- MIPS R3000 CPU, executing MIPS I, MIPS II, and MIPS16 instructions
- EJTAG Interface and Controller
  - Nonintrusive debug
  - Real-time PC trace
  - Breakpoints
- FastMDU
  - 5 cycle 32-bit to 64-bit multiply and accumulate
  - 34/35 cycle divide
- Basic BIU and Cache Controller (BBCC) with four write back buffers included
- Two 32-bit Timers
- MMU supports a 64-entry TLB RAM
- ICEport included for backward compatibility with SerialICE™-1 debugger
- Caches:
  - 1 to 32 Kbytes of direct-mapped or set-associative I-Cache
  - 1 to 32 Kbytes of direct-mapped D-Cache

Features

- All configuration through EasyMACRO interfaces, no external logic needed
- Clock speed is 120 MHz at 1.8 V (120 MIPS peak and estimated 96 MIPS sustained)
- 16-bit and 32-bit code can be mixed arbitrarily with full support on a subroutine basis
- Models available: performance and software development, Verilog, and gate level, timing-accurate models. Support for VHDL models through Model Technology's Model*Sim* simulator
- Compatible with the Microsoft Windows CE operating system
- Compatible with the full range of MIPS, third-party software development, and system verification environment tools
- Implements full-scan methodology to achieve very high design fault coverage

Technology

- LSI Logic G12-p Technology with 0.13 µ L_{eff} (0.18 µ L_{drawn})
- 1.8 V operation

Functional Description

The TR4103 CPU performs all arithmetic, logical, shift, and address calculations. The CPU supports EJTAG debug and is closely coupled with the FastMDU. The FastMDU calculates all multiply and divide operations for the EZ4103 and provides 5 cycle 32 x 32 = 64 bit multiply and accumulate operations, 34/35 cycle divide, saturated math, and overflow indication.

The Basic Bus Interface Unit and Cache Controller (BBCC) provides an internal bus interface and connects the CPU to the caches. Four Write Buffers are integrated with the BBCC in the EZ4103. The BBus connects the BBCC, the SerialICE-1 and EJTAG units, and the two internal timers with logic implemented inside the EZ4103.

The Memory Management Unit (MMU) translates virtual addresses from the CPU to physical addresses and uses an external 64-entry Translation Look-Aside Buffer (TLB) RAM.

The CPU controls the two internal 32-bit Timers. Each timer can count down from a preloaded value, roll over or stop at zero, generate an interrupt on zero, or act as a BBus watchdog.

The EJTAG Interface provides an on-chip debug scheme with breakpoint and PC Trace capability in an EJTAG compatible design. The EJTAG debugger provides real-time PC trace and breakpoint capabilities.

A SerialICE-1 Interface (UART) is also included in the EasyMACRO subsystem to promote backward compatibility with an existing TinyRISC design.

The CBus Interface passes data to and from the CPU. This interface connects the CPU to the MMU, the BBCC, and up to three optional coprocessors and on-chip memory implemented outside the EasyMACRO subsystem.

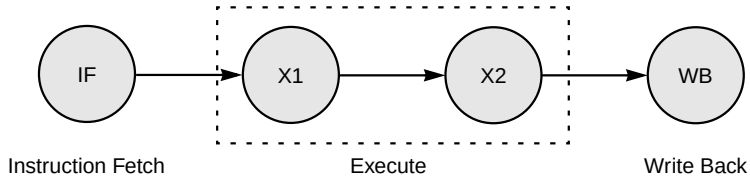
The FlexLink Interface allows the logic designer to insert specialized arithmetic instructions into the microprocessor EasyMACRO subsystem. The FlexLink interface can handle single-cycle and multi-cycle operations.

The optional 32-bit FBusMACRO module controls the FBus, which is a dedicated, multimaster bus that connects outside devices with the EZ4103 internal components. The optional FBusMACRO module allows seamless EZ4103 connection to a variety of devices, including EPROM, RAM, DRAM, SDRAM, and general purpose I/O pins. The FBus also supports burst read (one cycle) and write, built-in arbitration for an external FBus master, and snooping of external write accesses to memory. In the EZ4103, the FBusMACRO interfaces mainly with the BBCC module.

Pipeline Architecture

The EZ4103 implements a three-stage pipeline (Fetch, Execute, and Write Back) that uses a single adder for the ALU, the data address, and the instruction address. Sharing a single adder, as well as eliminating pipeline registers and bypass logic, dramatically reduces the circuitry required to implement the EasyMACRO microprocessor. The EZ4103 does not require a load delay slot. Figure 2 shows the microprocessor CPU three-stage pipeline.

Figure 2 EZ4103 Instruction Pipeline



The execution of a single EZ4103 instruction consists of the following three pipeline stages:

1. Instruction Fetch – The EZ4103 fetches the instruction (IF). If necessary, the core decompresses a 16-bit instruction into a 32-bit instruction.
2. Execute – The EZ4103 executes all ALU instructions, resolves conditional branches, and calculates Load and Store addresses (X1). The EasyMACRO microprocessor subsystem transfers Load and Store data from external memory or cache (performs memory accesses) and performs Move To/From Coprocessor operations in a second Execute (Stall) Cycle (X2).

3. Write Back – The EZ4103 writes the results into the Register File (WB).

EZ4103 Design Support

The EZ4103 EasyMACRO subsystem has all the necessary tools to develop a system on a chip, including:

- Architectural Simulator
- Coverification
- EJTAG interface/on-chip debugger
- LR4103 Microprocessor Chip and BDMR4103 Evaluation Kit for evaluation and prototyping
- System Verification Environment
- Third-party Toolchain Support

The EZ4103 supports the LSI Logic EJTAG interface, which enables software development and hardware design debugging from a remote host. EJTAG uses the EZ4103 EJTAG pins to provide a debug solution with breakpoint capability and real-time trace of the program counter. A SerialICE-1 ICEport has also been added to the EZ4103 for backward compatibility with any existing TinyRISC designs.

The CoreWare program consists of three main elements:

1. A library of cores
2. A design development and simulation package
3. Expert applications support

The CoreWare library contains a wide range of complex cores based on accepted and emerging industry standards from high-speed interconnect and digital video to DSP and MIPS microprocessors. LSI Logic provides a complete framework for device and system development and simulation. LSI Logic has advanced ASIC technologies that consistently produce Right-First-Time™ silicon. The LSI Logic in-house experts provide design support from system architecture definition through chip layout and test vector generation.

Instruction Set Summary

Table 1 summarizes the 32-bit instruction set for the EZ4103. All instructions are MIPS I except those marked with a footnote. Tables 2 and 3 list the TinyRISC-specific CP0 and the Multiply/Divide instructions. Tables 4 and 5 list the MMU and the unimplemented MIPS II instructions. Table 6 provides a summary of the EZ4103 MIPS16 instruction set.

Table 1 EZ4103 Instruction Set Summary (32 bits)

Instruction	Description	Instruction	Description
Load/Store Instructions			
LB	Load Byte	SB	Store Byte
LBU	Load Byte Unsigned	SH	Store Halfword
LH	Load Halfword	SW	Store Word
LHU	Load Halfword Unsigned	SWL	Store Word Left
LW	Load Word	SWR	Store Word Right
LWL	Load Word Left	SYNC	Synchronize Shared Memory
LWR	Load Word Right		
Immediate Arithmetic Instructions			
ADDI	Add Immediate	ORI	OR Immediate
ADDIU	Add Immediate Unsigned	SLTI	Set on Less Than Immediate
ANDI	AND Immediate	SLTIU	Set on Less Than Immediate Unsigned
LUI	Load Upper Immediate	XORI	Exclusive OR Immediate
Three-Operand, Register-Type Arithmetic Instructions			
ADD	Add	SLT	Set on Less Than
ADDU	Add Unsigned	SLTU	Set on Less Than Unsigned
AND	Logical AND	SUB	Subtract
NOR	Logical NOR	SUBU	Subtract Unsigned
OR	Logical OR	XOR	Exclusive Logical OR

(Sheet 1 of 3)

Table 1 EZ4103 Instruction Set Summary (32 bits) (Cont.)

Instruction	Description	Instruction	Description
Jump and Branch Instructions			
BCzF	Branch on Coprocessor z False (also listed under Coprocessor Instructions)	BLTZAL	Branch on Less Than Zero and Link
BCzT	Branch on Coprocessor z True (also listed under Coprocessor Instructions)	BNE	Branch on Not Equal
BEQ	Branch on Equal	J	Jump
BGEZ	Branch on Greater Than or Equal to Zero	JAL	Jump and Link
BGEZAL	Branch on Greater Than or Equal to Zero and Link	JALR	Jump and Link Register
BGTZ	Branch on Greater Than Zero	JALX	Jump and Link Exchange
BLEZ	Branch on Less Than or Equal to Zero	JR	Jump Register
BLTZ	Branch on Less Than Zero		
Branch Likely Instructions			
BCzFL[1]	Branch on Coprocessor z False Likely	BGTZL[1]	Branch on Greater Than Zero Likely
BCzTL[1]	Branch on Coprocessor z True Likely	BLEZL[1]	Branch on Less Than or Equal to Zero Likely
BEQL[1]	Branch on Equal Likely	BLTZALL[1]	Branch on Less Than Zero and Link Likely
BGEZALL[1]	Branch on Greater Than or Equal to Zero and Link Likely	BLTZL[1]	Branch on Less Than Zero Likely
BGEZL[1]	Branch on Greater Than or Equal to Zero Likely	BNEL[1]	Branch on Not Equal Likely
Trap Instructions			
TEQ[1]	Trap if Equal	TLT[1]	Trap if Less Than
TEQI[1]	Trap if Equal Immediate	TLTI[1]	Trap if Less Than Immediate
TGE[1]	Trap if Greater Than or Equal	TLTIU[1]	Trap if Less Than Immediate Unsigned

(Sheet 2 of 3)

Table 1 EZ4103 Instruction Set Summary (32 bits) (Cont.)

Instruction	Description	Instruction	Description
Trap Instructions (Cont.)			
TGEI[1]	Trap if Greater Than or Equal Immediate	TLTU[1]	Trap if Less Than Unsigned
TGEIU[1]	Trap if Greater Than or Equal Immediate Unsigned	TNE[1]	Trap if Not Equal
TGEU[1]	Trap if Greater Than or Equal Unsigned	TNEI[1]	Trap If Not Equal Immediate
Coprocessor Instructions			
BCzF	Branch on Coprocessor z False (also listed under Jump and Branch Instructions)	LWCz	Load Word to Coprocessor z ($z \neq 0$)
BCzT	Branch on Coprocessor z True (also listed under Jump and Branch Instructions)	MTCz	Move To Coprocessor z
COPz	Coprocessor Operation	MFCz	Move From Coprocessor z
CTCz	Move Control to Coprocessor z	SWCz	Store Word from Coprocessor z ($z \neq 0$)
CFCz	Move Control from Coprocessor z		
Shift Instructions			
SLL	Shift Left Logical	SRAV	Shift Right Arithmetic Variable
SLLV	Shift Left Logical Variable	SRL	Shift Right Logical
SRA	Shift Right Arithmetic	SRLV	Shift Right Logical Variable
Special Control Instructions			
BREAK	Breakpoint	SYSCALL	System Call
EJTAG Debug Instructions			
SDBBP	Software Debug Breakpoint	DERET	Debug Exception Return
(Sheet 3 of 3)			

1. MIPS II instructions.

Table 2 EZ4103-Specific System Control Processor (CP0) Instructions (32 bits)

Instruction	Description	Instruction	Description
MFC0	Move from CP0	RFE	Restore from Exception
MTC0	Move to CP0	WAITI	Wait for Interrupt

Table 3 Multiply/Divide Instructions (32 bits)

Instruction	Description	Instruction	Description
MUL	Three-Operand Multiply	DIV	Divide
MULT	Multiply	DIVU	Divide Unsigned
MULTU	Multiply Unsigned	MFHI	Move From HI
MADD	Multiply Add	MFLO	Move From LO
MADDU	Multiply Add Unsigned	MTHI	Move To HI
MSUB	Multiply Subtract	MTLO	Move To LO
MSUBU	Multiply Subtract Unsigned		

Table 4 MMU TLB Instructions (32 bits)

Instruction	Description	Instruction	Description
TLBR	Read Indexed TLB Entry	TLBWI	Write Indexed TLB Entry
TLBWR	Write Random TLB Entry	TLBP	Probe TLB For Matching Entry

Table 5 Unimplemented MIPS II Instructions

Instruction	Description	Instruction	Description
COP1	All floating point instructions	ERET	Exception Return
LL	Load Linked Word	LDCz	Load Doubleword to Coprocessor
SC	Store Conditional Word	SDCz	Store Doubleword to Coprocessor

Table 6 EZ4103 Instruction Set Summary (MIPS16)

Instruction	Description	Instruction	Description
Load/Store Instructions			
LB	Load Byte	LW	Load Word
LBU	Load Byte Unsigned	SB	Store Byte
LH	Load Halfword	SH	Store Halfword
LHU	Load Halfword Unsigned	SW	Store Word
Arithmetic Instructions: ALU Immediate			
LI	Load Immediate	SLTIU	Set on Less Than Immediate Unsigned
ADDIU	Add Immediate Unsigned	CMPI	Compare Immediate
SLTI	Set on Less Than Immediate		
Arithmetic Instructions: Two/Three Operand, Register Type			
ADDU	Add Unsigned	AND	AND
SUBU	Subtract Unsigned	OR	OR
SLT	Set on Less Than	XOR	Exclusive OR
SLTU	Set on Less Than Unsigned	NOT	Not
CMP	Compare	MOVE	Move
NEG	Negate		
Multiply/Divide Instructions			
MULT	Multiply	DIVU	Divide Unsigned
MULTU	Multiply Unsigned	MFHI	Move From HI
DIV	Divide	MFLO	Move From LO
Jump and Branch Instructions			
JAL	Jump and Link	BNEZ	Branch on Not Equal to Zero
JALX	Jump and Link Exchange	BTEQZ	Branch on T Equal to Zero
JR	Jump Register	BTNEZ	Branch on T Not Equal to Zero
JALR	Jump and Link Register	B	Branch Unconditional

(Sheet 1 of 2)

Table 6 EZ4103 Instruction Set Summary (MIPS16) (Cont.)

Instruction	Description	Instruction	Description
Jump and Branch Instructions (Cont.)			
BEQZ	Branch on Equal to Zero		
Shift Instructions			
SLL	Shift Left Logical	SLLV	Shift Left Logical Variable
SRL	Shift Right Logical	SRLV	Shift Right Logical Variable
SRA	Shift Right Arithmetic	SRAV	Shift Right Arithmetic Variable
Special Instructions			
EXTEND	Extend	BREAK	Breakpoint
EJTAG Debug Instructions			
SDBBP	Software Debug Breakpoint[1]		
(Sheet 2 of 2)			

1. This instruction is unique to the EZ4103.

Signal Descriptions

Table 7 defines all the signals that interface with the EZ4103 EasyMACRO microprocessor subsystem. In the table, the signals are divided into the following categories:

- CPU
- FastMDU
- FlexLink Interface
- CBus Interface
- MMU Interface and Setup
- BBCC
- BBus Interface
- Timer
- SerialICE-1 Port
- Clock and Reset
- Scan Test
- EJTAG

Mnemonics for signals that are active LOW end with an ‘N’, and mnemonics for signals that are active HIGH end with a ‘P’.

Table 7 EZ4102 EasyMACRO Module Signals

Signal	I/O	Description
CPU		
D_CDEBUGMP	Output	Debug mode indicator
G_BIG_ENDIANP	Input	CPU Big endian select
G_CWAITIP	Output	CPU Wait Indicator
G_LOPRP[3:0]	Input	CPU low REV nibble of CP0 PRID register (hardwire)
(Sheet 1 of 10)		

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
FastMDU		
G_AMOFP	Output	FastMDU
G_BCMP	Input	FastMDU, multiply-accumulate instruction, TinyRISC backward compatibility mode
G_SATMP	Input	FastMDU saturated math mode select
FlexLink Interface		
F_CIR_BOTP[5:0]	Output	Instruction register bottom six bits
F_CIR_TOPP[5:0]	Output	Instruction register top six bits
F_CKILLXP	Output	Kill instruction in X1 stage
F_CPIPE_RUNN	Output	Indicates that next cycle is a CPU run cycle without an X2 stage
F_CRSP[31:0]	Output	Source register (rs) bus
F_CRTP[31:0]	Output	Source register (rt) bus
F_CRUN_INN	Output	CPU run enable
F_CRX_VALIDN	Output	Register buses valid
F_SELP	Input	FlexLink select
F_STALLP	Input	FlexLink stall request
F_XBUSP[31:0]	Input	FlexLink result bus
CBus Interface		
C_ADDR_ERRORP	Output	Memory address error
C_ADDR_OUTP[31:1]	Output	CBus virtual instruction/data address
C_BBEP	Input	BIU bus error
C_BBEP_ACKP	Output	CPU BIU bus error acknowledge
C_BYTEP[3:0]	Output	Byte enable signals
(Sheet 2 of 10)		

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
CBus Interface (Cont.)		
C_CBUS_STEALN	Output	Indicates a CBus steal from the BBCC
C_COPCONDP[3:0]	Input	CPU coprocessor condition bits
C_COP_DRIVEP	Output	Indicates that the coprocessor is driving the data bus
C_COPEXISTP[3:1]	Input	Indicates coprocessor existence
C_COPP[1:0]	Output	Coprocessor number
C_DATAP[31:0]	Output	CBus data bus
C_DRDYP	Output	CBus data ready on data bus
C_EXT_CDATAP[31:0]	input	CBus input from external modules
C_EXT_DRDYP	Input	External CBus data ready on data bus
C_EXT_IRDYP	Input	External CBus instruction ready
C_EXT_OEP	Output	External CBus output enable
C_EXT_RUN_ENABLEP	Input	CBus run enable signal, deasserting C_EXT_RUN_ENABLEP causes the CPU to stall
C_EXT_SELP	Input	External CBus select signal
C_INTGRP	Output	CPU interrupt grant
C_INTP[5:0]	Input	CPU interrupt direct
C_IP_DN	Output	Indicates that instruction/data is available on the CBus
C_IRDYP	Output	CBus instruction ready
C_KILLMEMP	Output	CPU kill memory transaction
C_KILLWP	Output	CBus kill instruction in WB stage
C_KILLXP	Output	CBus kill instruction in X1 stage
C_MADDR_OUTP[31:0]	Output	Physical address output from MMU
C_MADDR_VALIDP	Output	Indicates that physical address is valid
C_MEM_FETCHP	Output	CPU memory fetch request
(Sheet 3 of 10)		

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
CBus Interface (Cont.)		
C_MNOCACHEP	Output	MMU prevents current page data from storage in cache
C_MODE16P	Output	CPU in MIPS16 mode
C_RUNN	Output	Indicates that the next cycle is a run cycle
C_STOREP	Output	CPU store to memory request
MMU Interface and Setup		
G_MMUENP	Input	MMU enable configuration bit
M_CAMINP[25:0]	Input	TLB CAM array data
M_CAMOUTP[25:0]	Output	TLB CAM array data
M_GBITOUTP	Output	TLB group mask (global) bit
M_MATCHINP[5:0]	Input	TLB encoded match address
M_RAMINP[23:0]	Input	TLB RAM array data
M_RAMOUTP[23:0]	Output	TLB RAM array data
M_TLBCLKP	Output	TLB gated CLK (runs only during MMU stall cycles)
M_TLBINDP[5:0]	Output	TLB address
M_TLBMISSP	Input	TLB miss indicator
M_TLBMTCHP	Output	TLB match enable
M_TLBRDP	Output	TLB read enable
M_TLBWRTP	Output	TLB write enable
BBCC - System Configuration Register and Cache Setup		
G_CACHE_CONFIGP[2:0]	Input	Controls to configure cache/tag size
G_MREQP	Input	BBus modified request
G_SCONFIG1P[31:0]	Output	BBCC System Configuration register (SCR1)
G_SCONFIG2P[31:0]	Output	BBCC System Configuration register (SCR2)
(Sheet 4 of 10)		

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
BBCC - System Configuration Register and Cache Setup (Cont.)		
G_SCONFIG3P[31:0]	Output	BBCC System Configuration register (SCR3)
G_SCR2_RESETP[11:0]	Input	Copies into G_SCONFIG2P[11:0] during system reset
G_SCR2_STICKYP[3:0]	Input	Copies into G_SCONFIG2P[15:12], and value is sticky until reset by either system reset or CPU write zero
G_SCR3_READP[31:0]	Input	Read-only bits for G_SCONFIG3P[31:0]
BBCC - Cache and Tag		
R_I1DCDATAP[31:0]	Input	Data from I-Cache Set 1 Data RAM
R_I1DCLKP	Output	Clock for I-Cache Set 1 Data RAM
R_I1DWEP	Output	Write enable for I-Cache Set 1 Data RAM
R_I1TCDATAP[25:0]	Input	Data from I-Cache Set 1 Tag RAM
R_I1TCLKP	Output	Clock for I-Cache Set 1 Tag RAM
R_I1TWEP[4:0]	Output	Write enable for I-Cache Set 1 Tag RAM
R_IDDCDATAP[31:0]	Input	Data from I-Cache Set 0/D-Cache Data RAM
R_IDDCLKP	Output	Clock for I-Cache Set 0/D-Cache Data RAM
R_IDDWEP[3:0]	Output	Write enable for I-Cache Set 0/D-Cache Data RAM
R_IDTCDATAP[26:0]	Input	Data from I-Cache Set 0/D-Cache Tag RAM
R_IDTCLKP	Output	Clock for I-Cache Set 0/D-Cache Tag RAM
R_IDTWEP[5:0]	Output	Write enable for I-Cache Set 0/D-Cache Tag RAM
R_INDEXP[14:2]	Output	Address for I-Cache Set 0/D-Cache and I-Cache Set 1 Data RAMs
R_IP_DN	Output	MSB address bit for I-Cache Set 0/D-Cache Data and Tag RAM
R_LOCKP	Output	Lock bits for I-Cache Set 0/D-Cache Tag RAM
R_TAGP[21:0]	Output	Address Tag for I-Cache Set 0/D-Cache and I-Cache Set 1 Tag RAM

(Sheet 5 of 10)

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
BBCC - Cache and Tag (Cont.)		
R_VALIDP[3:0]	Output	Valid bits for I-Cache Set 0/D-Cache and I-Cache Set 1 Tag RAM
BBCC - OCM Related		
C_OCMCLKP	Output	On-chip memory clock
C_OCMEXISTP	Input	On-chip memory exists
C_OCMOEP	Output	On-chip memory output enable
C_OCMSELP	Input	On-chip memory select signal
C_OCMWEP	Output	On-chip memory write enable
BBus Interface		
B_CONTADDRN	Output	BBus continuous address indicator
B_FBREQN	Input	BBus request to master from FBus module
B_WRAPP	Output	BBus address wrap-around indicator
B_XBADDRP[31:2]	Output	Output address bus to all BBus devices
B_XBBLKREQN	Output	Block fetch request to external BBus device (only from BBCC)
B_XBBYTEN[3:0]	Output	Byte enable bits to all BBus devices
B_XBDATAP[31:0]	Output	Output data bus to all BBus devices
B_XBERRORN	Output	BBus error signal to all BBus devices (bundled)
B_XBIP_DN	Output	Instruction/data indicator to all BBus devices
B_XBNOSELN	Output	Indicates hardware test mode (B_ZCACHE_SELP) and no address selected to all BBus devices
B_XBRDYN	Output	Ready signal (transaction complete) to all BBus devices
B_XBSNOOPWAITP	Output	Wait for snoop to finish signal to all BBus devices
B_XBSTARTN	Output	Transaction start signal to all BBus devices
B_XBTXN	Output	Transaction active signal to all BBus devices

(Sheet 6 of 10)

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
BBus Interface (Cont.)		
B_XBWBURST_GNTN	Output	Write burst grant to external BBus device (only from BBCC)
B_XBWRN	Output	Read/write indicator to all BBus devices
B_XFBGNTN	Output	BBus grant to FBus module (FBM)
B_XZBGNTN	Output	BBus grant to external BBus device
B_ZBADDRP[31:2]	Input	Input address bus from external BBus device
B_ZBBLKGNTN	Input	Block fetch grant from external BBus device (only to BBCC)
B_ZBBYTEN[3:0]	Input	Byte enable bits from external BBus device
B_ZBDATAP[31:0]	Input	Input data bus from external BBus device
B_ZBDSNOOPP	Input	BBus data snoop signal
B_ZBERRORN	Input	BBus error signal from external BBus device
B_ZBIP_DN	Input	Indicates arriving instruction/data from external BBus device
B_ZBISNOOPP	Input	BBus instruction snoop signal
B_ZBRDYN	Input	Ready signal (transaction complete) from external BBus device
B_ZBREQN	Input	BBus request from external BBus device
B_ZBSTARTN	Input	Transaction start signal from external BBus device
B_ZBTXN	Input	Transaction active signal from external BBus device
B_ZBWBURST_REQN	Input	Write burst request from external BBus device (only to BBCC)
B_ZBWRN	Input	Indicates a read/write from external BBus device
B_ZCACHE_SELP	Input	Indicates hardware test mode. Signal is supplied by hardware test master (from external BBus device).
B_ZISETP	Input	Hardware cache test select between I-Cache Set 0 and Set 1. B_ZISETP is supplied by hardware test master (from external BBus device).
(Sheet 7 of 10)		

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
BBus Interface (Cont.)		
B_ZTAGTESTN	Input	Hardware cache test select between Tag and Data cache. B_ZTAGTESTN is supplied by hardware test master (from external BBus device).
G_MRRP	Input	Modified Round Robin internal-bus algorithm selector
Timer		
T_0OUTN	Output	Timer 0 output
T_1OUTN	Output	Timer 1 output
SerialICE-1 Port		
I_ICECLKP	Input	External clock, must run at 16x the serial bit rate
I_ICERXP	Input	Serial receive data
I_ICETXP	Output	Serial transmit data
I_RXRDYP	Output	Asserts when a byte is received
Clock and Reset		
G_PCLKP	Input	System clock
G_RESETN	Input	Synchronous system reset input
Scan Test		
G_SCAN_ENABLEP	Input	Scan chain enable
G_SCAN_INP	Input	Scan chain input
G_SCAN_MODEP	Input	Scan test logic enable
G_SCAN_OUTP	Output	Scan chain output
G_SCAN_RAMWEP	Input	Scan mode RAM write control
(Sheet 8 of 10)		

Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
EJTAG - Device Identification Register		
D_IPART_NUMBERP[13:0]	Input	Part number in Device Identification register
D_IDEVICE_REVP[1:0]	Input	Device revision code in Device Identification register
D_ILOCATIONP[3:0]	Input	LSI Logic geographic location code in Device Identification register
EJTAG - Implementation Register		
D_FORCEBRTP	Input	Controls PC trace setup
D_IASIDSIZEP[1:0]	Input	ASID size in Implementation register
D_ICHP[3:0]	Input	Obsolete Ch field in Implementation register
D_ICPLXBRKP	Input	Complex Break Support in Implementation register
D_IDCACHECP	Input	Data cache coherency in Implementation register
D_IICACHECP	Input	Instruction cache coherency in Implementation register
D_IIMPL3126P[5:0]	Input	Reserved
D_INODATABRKP	Input	Data address break in Implementation register
D_INODMAP	Input	No JTAG DMA support in Implementation register
D_INOINSTBRKP	Input	Instruction break in Implementation register
D_INOPCTRACEP	Input	No PC trace support in Implementation register
D_INOPROCBRKP	Input	Processor bus break in Implementation register
D_IPCSTWP[2:0]	Input	PCST width and DCLK division factor in Implementation register
D_IPROFSUPP[1:0]	Input	Profiling support in Implementation register
D_ISDBBPCODEP	Input	SDBBP uses Special2 (or version 1.3) opcode
D_ITPCWP[2:0]	Input	TPC width in Implementation register
D_SIMPIMPLP[9:0]	Input	Simple break configuration
D_TRACEMETHP	Input	Controls internal PC trace setup

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Table 7 EZ4102 EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
EJTAG - JTAG Setup		
D_JTAGALSOP	Input	Normal JTAG interface attached
D_JTAGIRBITSP[1:0]	Input	Number of bits in JTAG instruction register
D_JTAGTDOP	Input	Test Data Output from normal JTAG module
EJTAG - Probe		
D_TCK	Input	JTAG clock
D_TDI_DINT	Input	JTAG data in
D_TDO_DRIVEN	Output	JTAG drive indication for TDO
D_TDO_TPC	Output	JTAG data out
D_TMS	Input	JTAG mode select
D_TRST	Input	Active-LOW JTAG reset
EJTAG - PC Trace		
D_CLKP	Output	Divided processor clock
D_PCST1P[2:0]	Output	PC trace status information set 1
D_PCST2P[2:0]	Output	PC trace status information set 2
D_PCST3P[2:0]	Output	PC trace status information set 3
D_PCST4P[2:0]	Output	PC trace status information set 4
D_TPCP[8:2]	Output	PC and ASID bits
EJTAG - Miscellaneous Control		
D_PCLKWAKEUP	Output	Indicates wake-up of the PCLKP clock generator when either a JTAG break or a CPU soft reset occurs
D_PERRSTN	Output	Reset signal for peripheral from the EJTAG Control Register
D_PSLEEPN	Input	Run indication for CPU clock, generated by clock module

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EZ4103 Nomenclature

As with any new product, the EZ4103 nomenclature has changed since the previous TR4101 design. Table 8 lists the supporting products for the TR4101 and EZ4103 designs.

Table 8 TinyRISC Family Nomenclature

TinyRISC Design	Core	EasyMACRO	Evaluation Chip	Reference Chip	Evaluation Board
4101	TR4101 (CW001000)	–	EV4101 (L9C0099)	–	BDMR4101
4102	–	EZ4102 (CW001005)	–	LR4102 (L9A0212)	BDMR4102
4103	–	EZ4103 (CW001015)	–	LR4103 (L9A0238)	BDMR4103

Notes

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