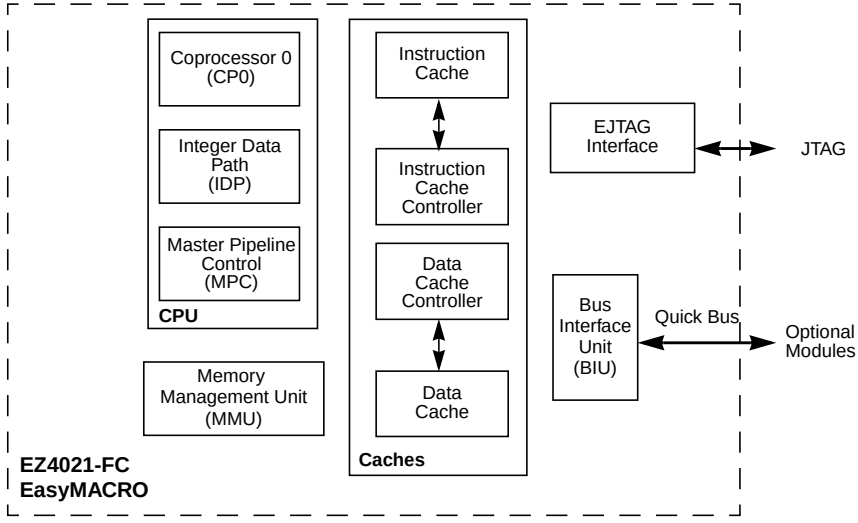
MiniRISC® EZ4021-FC EasyMACRO Microprocessor

Preliminary Datasheet

The MiniRISC EZ4021-FC Microprocessor EasyMACRO is a compact, high-performance, 64-bit microprocessor subsystem implemented in G12™ CMOS technology. The EZ4021-FC uses the LSI Logic CoreWare® system-on-a-chip methodology and executes the MIPS III instruction set. It is ideal for high-performance, cost-sensitive embedded processor applications. As shown in Figure 1, the EZ4021-FC includes the following components:

- CPU includes system coprocessor, an integer data path with multiply divide unit, and a master pipeline controller
- Instruction and data caches
- Memory Management Unit (MMU)
- Bus Interface Unit (BIU)
- Quick Bus interface
- EJTAG Interface module

Figure 1 EZ4021-FC Microprocessor EasyMACRO Block Diagram



Features

- High-performance RISC CPU
  - Single issue, five-stage pipeline
  - 250 native MIPS, 275 Dhrystone MIPS at 250 MHz
  - 250 MHz operation at WCABS (Tj = 125 °C, VDD = 1.71V, WC process)
  - Both big- and little-endian support for load and store operations
  - R4000 standard 32-bit timer/counter
  - MIPS CPU standard interrupt exceptions (one NMI, one timer, five hardware, two software)
- Integrated multiply and divide unit
  - High-performance eight bit/cycle multiplier
    - ◊ 32-bit signed/unsigned multiply in five CPU clock cycles
    - ◊ 64-bit signed/unsigned multiply in nine CPU clock cycles
  - Compact one bit/cycle divider
    - ◊ 32-bit signed/unsigned divide in 34 CPU clock cycles
    - ◊ 64-bit signed/unsigned divide in 66 CPU clock cycles
- Windows CE compatible MMU with 32 dual-entry page translations
- Integrated instruction and data caches
  - Harvard architecture
  - 16 Kbyte 2-way set-associative instruction and data caches
    - ◊ LRU algorithm for replacement
    - ◊ Line level lock for instruction RAM and scratchpad memory
    - ◊ Data cache has write-through or write back update policy, programmable on a page basis
- MIPS III Instruction Set Architecture
  - MIPS III ISA supporting 64-bit integer operations
  - Thirty-two 64-bit general-purpose registers
  - R4000-style status register and exception processing
  - Wait for Interrupt (WAITI) instruction for power saving
  - Supports SPECIAL2 Multiply-Accumulate extensions
- Advanced Debug Support
  - MIPS EJTAG version 1.5.3
  - Instruction and data breakpoints
  - Program Counter (PC) trace
  - Processor singlestep and software debug breakpoints

Features continued

- Technology
  - 2.6 mW/MHz power consumption (includes caches)
  - 12 mm^2 core size
  - 1.8 V Core VDD
  - LSI Logic G12 CMOS technology (0.18 µ L-drawn, 0.15 µ L-effective)

Functional Description

The EZ4021-FC CPU performs all arithmetic, logical, shift, and address calculations. The CPU includes:

- Data path and control

  Contains a 64-bit integer data path module with a 32 x 64-bit register file and an instruction decoder/data path control module.

- Integrated Multiply/Divide Unit (MDU)

  Supports the MIPS accumulate operations (MADD, MADDU, MSUB, and MSUBU) and the three-operand multiply (MUL). The MDU includes an eight-bits-per-cycle multiply capability and a one-bit-per-cycle divide capability.

- System control coprocessor (CP0)

  Provides exception processing support using the MIPS R4000 exception model and processor state control that includes three operating modes—kernel, user, supervisor.

The EZ4021-FC interface supports a new high-performance, on-chip bus known as the Quick Bus. The Quick Bus is a split-transaction bus that allows the overlap of memory requests (fetch/load/store) and data returns. A Quick Bus design operating at 125 MHz can achieve a peak bandwidth of 1.0 Gbytes per second.

The Bus Interface Unit (BIU) passes address/data between the CPU and the Quick Bus and arbitrates CPU-to-Quick Bus access. It provides a 64-bit incoming datapath from the Quick Bus to the CPU and a 64-bit path for outgoing data. Depending on the customer design, outgoing Quick Bus data can go to a variety destinations outside the EZ4021-FC.

The EZ4021-FC has separate instruction and data caches (I-Cache and D-Cache). Each cache is organized as a two-way set associative 16 Kbyte cache with a fixed cache block (line) size of 8 words (32-bytes). The caches are virtually indexed and physically tagged.

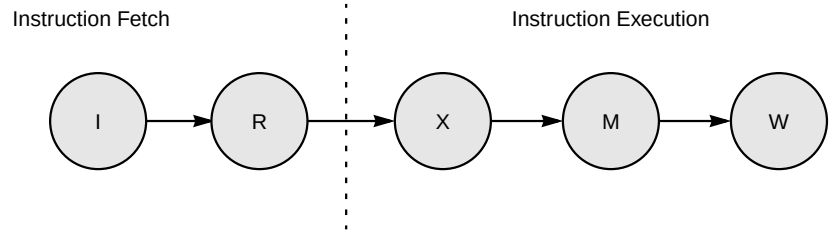
The memory management unit (MMU) performs virtual-to-physical address translation using a 32-entry joint translation lookaside buffer (TLB). The MMU supports a variety of page sizes from 4 Kbytes to 1 Mbyte.

The EZ4021-FC includes a Joint Test Action Group (JTAG) interface and supports Enhanced JTAG (EJTAG) functions. EJTAG is a debug feature of MIPS-based processors. You can use EJTAG to debug stand-alone processors as well as 32-bit or 64-bit processors that are embedded in a system like the EZ4021-FC.

Pipeline Architecture

The EZ4021-FC five-stage instruction pipeline is illustrated in Figure 2.

Figure 2 EZ4021-FC Instruction Pipeline



Instruction fetch occurs during the first two pipeline stages and instruction execution during the last three stages. After a stage accepts an instruction from the previous stage, it must hold the instruction for re-execution in case the pipeline stalls. The function of each pipeline stage is summarized below.

Instruction Fetch (I) – The EZ4021-FC fetches the instruction during this first stage.

Register Read (R) – In the R stage, the CPU reads any required operands from the Register File while decoding the instruction.

Execute (X) – Computational and logical instructions execute during the X stage. The CPU resolves conditional branches during this stage, and does the address calculations for load and store instructions.

Memory Access (M) – In this stage, the CPU accesses the cache for load and store instructions. Data returns to the register bypass logic at the end of the M stage.

Write Back (W) – The CPU writes results into the Register File in the W stage.

Application Examples

The EZ4021-FC is designed for mid- to high-end applications, including set top boxes and image-processing engines, networking switches/routers, and consumer products requiring 64-bit performance.

CoreWare Program

The CoreWare program consists of three main elements:

1. A library of cores
2. A design development and simulation package
3. Expert applications support

The CoreWare library contains a wide range of complex cores based on accepted and emerging industry standards from high-speed interconnect and digital video to DSP and MIPS microprocessors. LSI Logic provides a complete framework for device and system development and simulation. LSI Logic has advanced ASIC technologies that consistently produce Right-First-Time™ silicon. The LSI Logic in-house experts provide design support from system architecture definition through chip layout and test vector generation.

Instruction Set Summary

Table 1 summarizes the EZ4021-FC instruction set. All instructions are MIPS I except those marked otherwise.

Table 1 EZ4021-FC Instruction Set Summary

Instruction	Description	Instruction	Description
Normal CPU Load/Store Instructions			
LB	Load Byte	LWU	Load Word Unsigned - MIPS III
LBU	Load Byte Unsigned	SB	Store Byte
LD	Load Doubleword - MIPS III	SD	Store Doubleword - MIPS III
LH	Load Halfword	SH	Store Halfword
LHU	Load Halfword Unsigned	SW	Store Word
LW	Load Word		
Unaligned CPU Load/Store Instructions			
LDL	Load Doubleword Left - MIPS III	SDL	Store Doubleword Left - MIPS III
LDR	Load Doubleword Right - MIPS III	SDR	Store Doubleword Right - MIPS III
LWL	Load Word Left	SWL	Store Word Left
LWR	Load Word Right	SWR	Store Word Right
Atomic Update CPU Load/Store Instructions			
LL	Load Linked Word - MIPS II	SC	Store Conditional Word - MIPS II
LLD	Load Linked Doubleword - MIPS III	SCD	Store Conditional Doubleword - MIPS III
Coprocessor Load/Store Instructions			
LDCz	Load Doubleword to Coprocessor - MIPS II	SDCz	Store Doubleword from Coprocessor - MIPS II
LWCz	Load Word to Coprocessor	SWCz	Store Word from Coprocessor

(Sheet 1 of 5)

Table 1 EZ4021-FC Instruction Set Summary (Cont.)

Instruction	Description	Instruction	Description
ALU Instructions with Immediate Operand			
ADDI	Add Immediate	LUI	Load Upper Immediate
ADDIU	Add Immediate Unsigned	ORI	OR Immediate
DADDI	Doubleword Add Immediate - MIPS III	SLTI	Set on Less Than Immediate
DADDIU	Doubleword Add Immediate Unsigned - MIPS III	SLTIU	Set on Less Than Immediate Unsigned
ANDI	AND Immediate	XORI	Exclusive OR Immediate
Three-Operand ALU Instructions			
ADD	Add	NOR	Logical NOR
ADDU	Add Unsigned	OR	Logical OR
AND	Logical AND	SLT	Set on Less Than
DADD	Doubleword Add - MIPS III	SLTU	Set on Less Than Unsigned
DADDU	Doubleword Add Unsigned - MIPS III	SUB	Subtract
DSUB	Doubleword Subtract - MIPS III	SUBU	Subtract Unsigned
DSUBU	Doubleword Subtract Unsigned - MIPS III	XOR	Exclusive Logical OR
Shift Instructions			
DSLL	Doubleword Shift Left Logical - MIPS III	DSRAV	Doubleword Shift Right Arithmetic Variable - MIPS III
DSLL32	Doubleword Shift Left Logical Plus 32 - MIPS III	SLL	Shift Left Logical
DSRA	Doubleword Shift Right Arithmetic	SLLV	Shift Left Logical Variable
DSRA32	Doubleword Shift Right Arithmetic Plus 32 - MIPS III	SRA	Shift Right Arithmetic
DSRL	Doubleword Shift Right Logical	SRAV	Shift Right Arithmetic Variable

(Sheet 2 of 5)

Table 1 EZ4021-FC Instruction Set Summary (Cont.)

Instruction	Description	Instruction	Description
Shift Instructions (Cont.)			
DSRL32	Doubleword Shift Right Logical Plus 32 - MIPS III	SRL	Shift Right Logical
DSLLV	Doubleword Shift Left Logical Variable - MIPS III	SRLV	Shift Right Logical Variable
DSRLV	Doubleword Shift Right Logical Variable - MIPS III		
Multiply/Divide Instructions			
DDIV	Doubleword Divide - MIPS III	MFHI	Move From HI
DDIVU	Doubleword Divide Unsigned - MIPS III	MFLO	Move From LO
DIV	Divide	MTHI	Move To HI
DIVU	Divide Unsigned	MTLO	Move To LO
DMULT	Doubleword Multiply - MIPS III	MULT	Multiply
DMULTU	Doubleword Multiply Unsigned - MIPS III	MULTU	Multiply Unsigned
Jump Instructions			
J	Jump	JALR	Jump and Link Register
JAL	Jump and Link	JR	Jump Register
PC-Relative Conditional Branch Instructions			
BEQ	Branch on Equal	BLEZ	Branch on Less Than or Equal to Zero
BGEZ	Branch on Greater Than or Equal to Zero	BLTZ	Branch on Less Than Zero
BGEZAL	Branch on Greater Than or Equal to Zero and Link	BLTZAL	Branch on Less Than Zero and Link
BGTZ	Branch on Greater Than Zero	BNE	Branch on Not Equal

(Sheet 3 of 5)

Table 1 EZ4021-FC Instruction Set Summary (Cont.)

Instruction	Description	Instruction	Description
PC-Relative Conditional Branch Likely Instructions			
BEQL	Branch on Equal Likely - MIPS II	BLEZL	Branch on Less Than or Equal to Zero Likely - MIPS II
BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely - MIPS II	BLTZALL	Branch on Less Than Zero and Link Likely - MIPS II
BGEZL	Branch on Greater Than or Equal to Zero Likely - MIPS II	BLTZL	Branch on Less Than Zero Likely - MIPS II
BGTZL	Branch on Greater Than Zero Likely - MIPS II	BNEL	Branch on Not Equal Likely - MIPS II
Breakpoint and System Call Instructions			
BREAK	Breakpoint	SYSCALL	System Call
Trap-on-Condition Instructions			
TEQ	Trap if Equal - MIPS II	TLT	Trap if Less Than - MIPS II
TEQI	Trap if Equal Immediate - MIPS II	TLTI	Trap if Less Than Immediate - MIPS II
TGE	Trap if Greater Than or Equal - MIPS II	TLTIU	Trap if Less Than Immediate Unsigned - MIPS II
TGEI	Trap if Greater Than or Equal Immediate - MIPS II	TLTU	Trap if Less Than Unsigned - MIPS II
TGEIU	Trap if Greater Than or Equal Immediate Unsigned - MIPS II	TNE	Trap if Not Equal - MIPS II
TGEU	Trap if Greater Than or Equal Unsigned - MIPS II	TNEI	Trap If Not Equal Immediate - MIPS II
Serialization Instructions			
SYNC	Synchronize Shared Memory - MIPS II		

(Sheet 4 of 5)

Table 1 EZ4021-FC Instruction Set Summary (Cont.)

Instruction	Description	Instruction	Description
Coprocessor Data Movement and Conditional Branch Instructions			
BCzF	Branch on Coprocessor z False	DMFCz	Doubleword Move from Coprocessor
BCzT	Branch on Coprocessor z True	DMTCz	Doubleword Move to Coprocessor
CFCz	Move Control from Coprocessor z	MFCz	Move From Coprocessor z
COPz	Coprocessor Operation	MTCz	Move To Coprocessor z
CTCz	Move Control to Coprocessor z		
System Control Coprocessor (CPO) Instructions			
ERET	Exception Return	TLBR	Read Indexed TLB Entry
MFC0	Move from CP0	TLBWI	Write Indexed TLB Entry
MTC0	Move to CP0	TLBWR	Write Random TLB Entry
TLBP	Probe TLB For Matching Entry		
Cache Maintenance Instruction			
CACHE	Cache Maintenance		
General 32-Bit Instruction Extensions			
MADD	Multiply Add	MSUB	Multiply Subtract
MADDU	Multiply Add Unsigned	MSUBU	Multiply Subtract Unsigned
MUL	Multiply	SDBBP	Software Debug Breakpoint
CP0 Instruction Extensions			
DERET	Debug Exception Return		
WAITI	Wait for Interrupt		

(Sheet 5 of 5)

Signal Descriptions

Table 2 defines all the signals that interface with the EZ4021-FC. In the table, the signals are divided into the following categories:

- Quick Bus Interface
- Interrupt, Clock, and Reset
- EJTAG and PC Trace
- Global Test Mode
- RAM BIST
- Miscellaneous

Mnemonics for signals that are active LOW end with an ‘N’, and mnemonics for signals that are active HIGH end with a ‘P’.

Table 2 EZ4021-FC EasyMACRO Module Signals

Signal	I/O	Description
Quick Bus Interface		
BC_D_QB_BREQP	Output	Bus Request for Data Access
BC_E_QB_BREQP	Output	Bus Request for EJTAG DMA
BC_I_QB_BREQP	Output	Bus Request for Instruction Fetch
BC_QB_ADDRP[31:3]	Output	Address
BC_QB_BURSTREQP	Output	Burst Request
BC_QB_BYTEP[7:0]	Output	Byte Enable Signals
BC_QB_CMDLOCKP	Output	Command Lock
BC_QB_RDACKP	Output	Read Data Acknowledge
BC_QB_READP	Output	Read Request
BC_QB_WRDATAP[63:0]	Output	Write Data
(Sheet 1 of 6)		

Table 2 EZ4021-FC EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
Quick Bus Interface (Cont.)		
BC_QB_WRITEP	Output	Write Request
QB_ADDRP[31:3]	Input	Address (snooping)
QB_BADADDRP	Input	Bad Address Error
QB_BOFFP	Input	Back Off (snooping)
QB_BURSTACKP	Input	Burst Request Acknowledge
QB_CMDRDYP	Input	Command Ready
QB_GRANT_BC_DP	Input	Data Access Command Bus Grant
QB_GRANT_BC_EP	Input	EJTAG DMA Command Bus Grant
QB_GRANT_BC_IP	Input	Instruction Fetch Command Bus Grant
QB_RDDATAP[63:0]	Input	Read Data
QB_RDERRP	Input	Read Data Error
QB_RDRDY_BC_DP	Input	Read Data Ready for Data Read
QB_RDRDY_BC_EP	Input	Read Data Ready for EJTAG Read
QB_RDRDY_BC_IP	Input	Read Data Ready for Instruction Fetch
QB_SLRDY_BC_DP	Input	Slave Ready for Data Access
QB_SLRDY_BC_EP	Input	Slave Ready for EJTAG DMA
QB_SLRDY_BC_IP	Input	Slave Ready for Instruction Fetch
QB_WRITEP	Input	Snoop Request (snooping)
Interrupt, Clock, and Reset		
CG_RESETP	Input	Clock Generator Reset
EZ_SCLK_GATEP	Output	System/Secondary Clock Gate
INTP[4:0]	Input	External Hardware Interrupts
NMIP	Input	Nonmaskable Interrupt
(Sheet 2 of 6)		

Table 2 EZ4021-FC EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
Interrupt, Clock, and Reset (Cont.)		
PCLKP	Input	Primary CPU Clock
RESETP	Input	System Cold Reset
SCLKP_DIVP[1:0]	Input	SCLKP Divide Ratio
EJTAG and PC Trace Signals		
DJ_TCKP	Input	EJTAG Test Clock
DJ_TDIP_DINTN	Input	Test Data Input/Debug Interrupt
DJ_TDOP_TPCP	Output	Test Data Output/Target PC Output
DJ_TMSP	Input	Test Mode Select
DJ_TRSTN	Input	Test Reset
DCLKP	Output	EJTAG PC Trace Clock
DT_PCST1[2:0]	Output	PC Trace Status Information 1
DT_PCST2[2:0]	Output	PC Trace Status Information 2
DT_TPCPLP[6:0]	Output	TPC Plus
DJ_JTAGALSOP	Input	Parallel JTAG Present
DJ_JTAGTDOP	Input	Parallel JTAG TDO
DJ_TDO_DRIVEN	Output	TDO Output Enable
DJ_PURETDO_DRN	Output	Pure TDO Output Enable
DJ_PURETDOP	Output	Pure TDO
DT_TPC1P	Output	Bit 1 of the TPC (TPC[1])
BC_DMP	Output	Debug Mode
DJ_DBGBRKP	Input	Debug Break
DJ_PERRSTN	Output	Peripheral Reset
DJ_DBRKDEMUXP	Output	Disable DTIP_DINTN Break

(Sheet 3 of 6)

Table 2 EZ4021-FC EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
EJTAG and PC Trace Signals (Cont.)		
DJ_EJTAGIRBITS[1:0]	Input	EIR Extension Width
DJ_PON[19:0]	Input	Part Number
DT_PCTEN	Input	PC Trace Enable
MMU_CNTALWYSP	Input	MMU Increment Count Reg in Debug Mode
Global Test Mode Signals		
GSCAN_ENABLEP	Input	Core Scan Enable
GSCAN_IN1P	Input	Core Scan Chain 1 Input
GSCAN_IN2P	Input	Core Scan Chain 2 Input
GSCAN_IN3P	Input	Core Scan Chain 3 Input
GSCAN_IN4P	Input	Core Scan Chain 4 Input
GSCAN_IN5P	Input	Core Scan Chain 5 Input
GSCAN_IN6P	Input	Core Scan Chain 6 Input
GSCAN_MODEP	Input	Global Test Mode
GSCAN_OUT1P	Output	Core Scan Chain 1 Output
GSCAN_OUT2P	Output	Core Scan Chain 2 Output
GSCAN_OUT3P	Output	Core Scan Chain 3 Output
GSCAN_OUT4P	Output	Core Scan Chain 4 Output
GSCAN_OUT5P	Output	Core Scan Chain 5 Output
GSCAN_OUT6P	Output	Core Scan Chain 6 Output
GSCAN_RAMCLKP	Input	Scan Test RAM Clock and BIST Clock
RAM BIST Signals		
BIST_DIAG_EN	Input	BIST Diag Enable
BIST_HOLD	Input	BIST Hold Command

(Sheet 4 of 6)

Table 2 EZ4021-FC EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
RAM BIST Signals (Cont.)		
BIST_SETUP[1:0]	Input	BIST Setup
BIST_SHIFT	Input	BIST Shift Command
BIST_SI	Input	BIST Shift Data In
BIST_SO	Output	BIST Shift Data Out
MBIST_DONE	Output	BIST Test Completion
MBIST_EN	Input	BIST Controller Enable
MBIST_GO	Output	BIST Test Failure Indication
TCK	Input	BIST TAP Controller Clock
TCK_MODE	Input	BIST TCK Mode
Miscellaneous Signals		
BIG_ENDIANP	Input	Big Endian Mode
CACHE_TESTP	Input	Cache Test Mode
COP_CP0COND	Input	CP0 Branch Condition
CPU_EC_WAITI	Output	Wait for Interrupt
DCACHE_ENABLEP	Input	Data Cache Enable
DHQ_SCR1[31:0]	Output	System Configuration Register
ICACHE_ENABLEP	Input	Instruction Cache Enable
LOADSCHED_ENABLEP	Input	Load Scheduling Enable
MMU_ENABLEP	Input	MMU Enable
PREFETCH_ENABLEP	Input	Instruction Prefetch Enable
PRID_REV[3:0]	Input	Processor Revision Identifier
PSTALLP	Output	EZ4021-FC Global Stall
SNOOP_ENABLEP	Input	Data Cache Snoop Enable

(Sheet 5 of 6)

Table 2 EZ4021-FC EasyMACRO Module Signals (Cont.)

Signal	I/O	Description
Miscellaneous Signals (Cont.)		
READPRI_ENABLEP	Input	Read Priority Enable
VCED_ENABLEP	Input	Virtual Coherency Exception Data Enable
WRITEBUF_ENABLEP	Input	Write Buffer Enable
(Sheet 6 of 6)		

Notes

Notes

Notes

Sales Offices and Design Resource Centers

LSI Logic Corporation
Corporate Headquarters
Tel: 408.433.8000
Fax: 408.433.8989

NORTH AMERICA

California
Irvine
♦ Tel: 949.809.4600
Fax: 949.809.4444

Pleasanton Design Center
Tel: 925.730.8800
Fax: 925.730.8700

San Diego
Tel: 858.467.6981
Fax: 858.496.0548

Silicon Valley
♦ Tel: 408.433.8000
Fax: 408.954.3353

Wireless Design Center
Tel: 858.350.5560
Fax: 858.350.0171

Colorado
Boulder
♦ Tel: 303.447.3800
Fax: 303.541.0641

Colorado Springs
Tel: 719.533.7000
Fax: 719.533.7020

Fort Collins
Tel: 970.223.5100
Fax: 970.206.5549

Florida
Boca Raton
Tel: 561.989.3236
Fax: 561.989.3237

Georgia
Alpharetta
Tel: 770.753.6146
Fax: 770.753.6147

Illinois
Oakbrook Terrace
Tel: 630.954.2234
Fax: 630.954.2235

Kentucky
Bowling Green
Tel: 270.793.0010
Fax: 270.793.0040

Maryland
Bethesda
Tel: 301.897.5800
Fax: 301.897.8389

Massachusetts
Waltham
♦ Tel: 781.890.0180
Fax: 781.890.6158

Burlington - Mint Technology
Tel: 781.685.3800
Fax: 781.685.3801

Minnesota
Minneapolis
♦ Tel: 612.921.8300
Fax: 612.921.8399

New Jersey
Red Bank
Tel: 732.933.2656
Fax: 732.933.2643

Cherry Hill - Mint Technology
Tel: 856.489.5530
Fax: 856.489.5531

New York
Fairport
Tel: 716.218.0020
Fax: 716.218.9010

North Carolina
Raleigh
Tel: 919.785.4520
Fax: 919.783.8909

Oregon
Beaverton
Tel: 503.645.0589
Fax: 503.645.6612

Texas
Austin
Tel: 512.388.7294
Fax: 512.388.4171

Plano
♦ Tel: 972.244.5000
Fax: 972.244.5001

Houston
Tel: 281.379.7800
Fax: 281.379.7818

Canada
Ontario
Ottawa
♦ Tel: 613.592.1263
Fax: 613.592.3253

INTERNATIONAL

France
Paris
LSI Logic S.A.
Immeuble Europa
♦ Tel: 33.1.34.63.13.13
Fax: 33.1.34.63.13.19

Germany
Munich
LSI Logic GmbH
♦ Tel: 49.89.4.58.33.0
Fax: 49.89.4.58.33.108

Stuttgart
♦ Tel: 49.711.13.96.90
Fax: 49.711.86.61.428

Italy
Milan
LSI Logic S.P.A.
♦ Tel: 39.039.687371
Fax: 39.039.6057867

Japan
Tokyo
LSI Logic K.K.
♦ Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

Osaka
♦ Tel: 81.6.947.5281
Fax: 81.6.947.5287

Korea
Seoul
LSI Logic Corporation of Korea Ltd
Tel: 82.2.528.3400
Fax: 82.2.528.2250

The Netherlands
Eindhoven
LSI Logic Europe Ltd
Tel: 31.40.265.3580
Fax: 31.40.296.2109

Singapore
Singapore
LSI Logic Pte Ltd
Tel: 65.334.9061
Fax: 65.334.4749

Sweden
Stockholm
LSI Logic AB
♦ Tel: 46.8.444.15.00
Fax: 46.8.750.66.47

Taiwan
Taipei
LSI Logic Asia, Inc.
Taiwan Branch
Tel: 886.2.2718.7828
Fax: 886.2.2718.8869

United Kingdom
Bracknell
LSI Logic Europe Ltd
♦ Tel: 44.1344.426544
Fax: 44.1344.481039

♦ Sales Offices with Design Resource Centers

To receive product literature, visit us at http://www.lsilogic.com

ISO 9000 Certified

Printed on Recycled Paper

BM
Printed in USA
Doc. No. DB08-000138-00