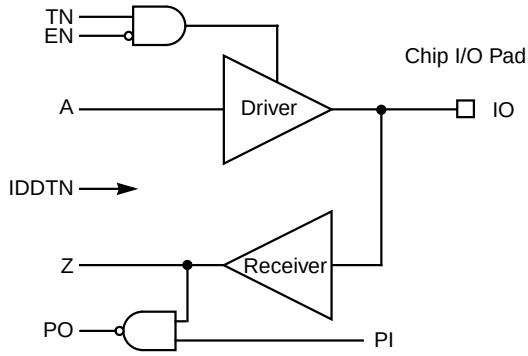
G12™-p bd4f5fs60ls33 4 mA, 60 MHz, 5-Volt Tolerant, Fail-Safe I/O Buffer

Datasheet

The bd4f5fs60ls33 bidirectional buffer cell (Figure 1) provides up to 60 MHz off-chip input/output (I/O) signaling for application-specific integrated circuit (ASIC) chips implemented in the LSI Logic G12™-p 0.13 µm process technology. One application of the bd4f5fs60ls33 buffer is as a clock driver.

Figure 1 bd4f5fs60ls33 Block Diagram



Features and Benefits

- 60 MHz, 3.3 V I/O operation
- 5-Volt tolerant
- Fail-safe at high voltages
- Feedthrough protection
- 20 µA maximum leakage current
- Minimum 4 mA current drive into a 40 pF load at 60 MHz
- 1.8 V internal signaling for reduced power consumption
- Uses one standard I/O slot

General Description

The bd4f5fs60ls33 bidirectional I/O buffer contains a totem-pole type driver, a receiver, and test circuitry. Included level translation circuitry enables the driver to receive 1.8 V level signals from the ASIC circuitry

and produce 3.3 V level output at the I/O pad. Similarly, the receiver receives off-chip input at 3.3 volts and translates it to 1.8 volts for the internal ASIC application. Built-in NAND-tree logic gates and IDDTN control for IDDQ leakage testing enable use of the standard LSI Logic test methodology.

The buffer is 5-volt tolerant. Although the off-chip I/O signaling normally operates at 3.3 V, external circuitry may cause higher voltages, typically upwards of 5 V, to appear at the chip I/O pad. Circuit and process techniques ensure that such DC or transient voltages do not damage the buffer circuitry.

In the absence of a V_{DD} supply, the buffer is fail-safe and protected against voltage feedthrough. With high voltage applied to the chip I/O pad, the buffer can survive without degradation for up to ten years. Furthermore, with a low, maximum 20 µA leakage current, the high voltage can not power up the ASIC through voltage feedthrough.

The following sections describe the `bd4f5fs60ls33` buffer, which adheres to the general specifications in Table 1.

Table 1 General Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.97	3.3	3.63	V
T_j	Junction temperature		0	–	125	˚C
ESD	Electrostatic discharge, human body model (HBM)	MIL-STD-883C, Method 3015.7 100 pF @1.5 KΩ	2000	–	–	V
	Electrostatic discharge, charged device model (CDM)	ESD DS5.3.1-1996	500	–	–	V

The final section, “System Design Guidelines”, provides layout guidelines to ensure good signal integrity for applications using the noise-sensitive, high-speed cells.

Signal Descriptions

Table 2 describes the `bd4f5fs60ls33` connections.

Table 2 bd4f5fs60ls33 Connections

Signal	Direction	Description
A	IN	Data input to driver from ASIC circuitry
EN	IN	0 = Normal mode 1 = Disable driver
IDDTN	IN	0 = Power down entire cell[1] 1 = Normal mode
PI	IN	NAND-tree parametric test input
TN	IN	0 = Disable driver 1 = Normal mode
IO	IN/OUT	Input/output pad
PO	OUT	NAND-tree parametric test output
Z	OUT	Receiver buffer output to ASIC circuitry

1. Used for production IDDQ leakage test

Driver

The following sections describe the driver side of the I/O buffer.

Truth Table

Table 3 describes the bd4f5fs60ls33 driver behavior.

Table 3 Driver Truth Table

IDDTN	A	TN	EN	IO
0[1]	X[2]	X	X	High Impedance
1	X	X	1	High Impedance
1	X	0	X	High Impedance
1	0	1	0	0
1	1	1	0	1

1. Factory IDDQ test setting
2. Don’t care state, X = 0 or 1

Driver Specifications

DC Characteristics

Table 4 describes the bd4f5fs60ls33 driver DC characteristics.

Table 4 Driver DC Characteristics[1]

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output, LOW	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	Output, HIGH	I_{OH} = –4 mA V_{DD} = 3.135 V	2.4	–	–	V
I_{OL}	Sink current	V_{OL} = 0.4 V maximum	4	–	–	mA
I_{OH}	Source current	V_{OH} = 2.4 V minimum	–	–	–4	mA
I_{OZ}	3-Stated leakage current	$0 \le V_{PAD} \le 5.5$ V, V_{DD} = 3.3 V ±10%	–	–	20	µA
I_{LU}	Latchup current	-2 V < V_{PAD} < +8 V	–	–	±100	mA

1. Values apply over all voltage, temperature, and process conditions.

Driver Slew Rate

In the rise/fall test, the driver drives a signal across a 40 pF load capacitor (Figure 2). Table 5 shows the observed slew rate across the load capacitor measured from 0.6 V to 2.2 V.

Figure 2 Rise/Fall Test Circuit

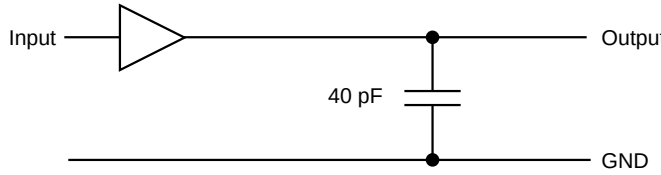


Table 5 Driver Rise/Fall Slew Rate

Min.	Typ.	Max.	Unit
500	880	1500	mV/ns

Receiver

The following sections describe the receiver side of the I/O buffer.

Truth Table

Table 6 describes the bd4f5fs60ls33 receiver behavior.

Table 6 Receiver Truth Table

Inputs			Outputs	
IDDTN	**IO**	**PI**	**Z**	**PO**
0[1]	High Impedance	1	1	0
1	0	0	0	1
1	1	0	1	1
1	1	1	1	0

1. Factory IDDQ test setting

Receiver Specifications

Table 7 describes the bd4f5fs60ls33 receiver DC characteristics.

Table 7 Receiver DC Characteristics[1]

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IL}	Threshold, HIGH-to-LOW		1.0	–	1.50	V
V_{IH}	Threshold, LOW-to-HIGH		1.50	–	2.0	V
V_{TH}–V_{TL}	Hysteresis		320	–	–	mV
I_{LU}	Latch-up current	$-2\ V < V_{PAD} < +8\ V$	–	–	±100	mA

1. Values apply over all voltage, temperature, and process conditions

System Design Guidelines

To ensure good system-level operation, LSI Logic provides the following guidelines for placing the bd4f5fs60ls33 in the ASIC and for supplying power.

Placement

The bd4f5fs60ls33 cell requires placement on the I/O ring (Table 8) using one I/O slot.

Table 8 bd4f5fs60ls33 Dimensions on the I/O Ring

Width Along the I/O Ring	Length into the Chip
45.36 µm	371.01 µm

For correct placement of the bd4f5fs60ls33 cell, adhere to the following guidelines:

- A bd4f5fs60ls33 cell may adjoin another bd4f5fs60ls33 cell or a d4f5fsls33, bd4puf5fsls33, or bd4puodf5fsls33 cell.
- Separate the bd4f5fs60ls33 cell from any other type of I/O function by at least one I/O slot to avoid N-channel to P-channel design rule violations. If possible, use a VDD or VSS pad for the separation.
- Because its length exceeds the length of other standard I/O functions, the bd4f5fs60ls33 cell may not use a corner I/O slot.

Power

For best system-level performance, adhere to the following power guidelines:

- Use one power/ground pad pair for every four I/O cells.
- Place an I/O cell no more than four slots away from a power pad and no more than four slots away from a ground pad.

Notes

Sales Offices and Design Resource Centers

LSI Logic Corporation
Corporate Headquarters
Tel: 408.433.8000
Fax: 408.433.8989

NORTH AMERICA

California
Irvine
♦ Tel: 949.809.4600
Fax: 949.809.4444

Pleasanton Design Center
Tel: 925.730.8800
Fax: 925.730.8700

San Diego
Tel: 858.467.6981
Fax: 858.496.0548

Silicon Valley
♦ Tel: 408.433.8000
Fax: 408.954.3353

Wireless Design Center
Tel: 858.350.5560
Fax: 858.350.0171

Colorado
Boulder
♦ Tel: 303.447.3800
Fax: 303.541.0641

Colorado Springs
Tel: 719.533.7000
Fax: 719.533.7020

Fort Collins
Tel: 970.223.5100
Fax: 970.206.5549

Florida
Boca Raton
Tel: 561.989.3236
Fax: 561.989.3237

Georgia
Alpharetta
Tel: 770.753.6146
Fax: 770.753.6147

Illinois
Oakbrook Terrace
Tel: 630.954.2234
Fax: 630.954.2235

Kentucky
Bowling Green
Tel: 270.793.0010
Fax: 270.793.0040

Maryland
Bethesda
Tel: 301.897.5800
Fax: 301.897.8389

Massachusetts
Waltham
♦ Tel: 781.890.0180
Fax: 781.890.6158

Burlington - Mint Technology
Tel: 781.685.3800
Fax: 781.685.3801

Minnesota
Minneapolis
♦ Tel: 612.921.8300
Fax: 612.921.8399

New Jersey
Red Bank
Tel: 732.933.2656
Fax: 732.933.2643

Cherry Hill - Mint Technology
Tel: 856.489.5530
Fax: 856.489.5531

New York
Fairport
Tel: 716.218.0020
Fax: 716.218.9010

North Carolina
Raleigh
Tel: 919.785.4520
Fax: 919.783.8909

Oregon
Beaverton
Tel: 503.645.0589
Fax: 503.645.6612

Texas
Austin
Tel: 512.388.7294
Fax: 512.388.4171

Plano
♦ Tel: 972.244.5000
Fax: 972.244.5001

Houston
Tel: 281.379.7800
Fax: 281.379.7818

Canada
Ontario
Ottawa
♦ Tel: 613.592.1263
Fax: 613.592.3253

INTERNATIONAL

France
Paris
LSI Logic S.A.
Immeuble Europa
♦ Tel: 33.1.34.63.13.13
Fax: 33.1.34.63.13.19

Germany
Munich
LSI Logic GmbH
♦ Tel: 49.89.4.58.33.0
Fax: 49.89.4.58.33.108

Stuttgart
♦ Tel: 49.711.13.96.90
Fax: 49.711.86.61.428

Italy
Milan
LSI Logic S.P.A.
♦ Tel: 39.039.687371
Fax: 39.039.6057867

Japan
Tokyo
LSI Logic K.K.
♦ Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

Osaka
♦ Tel: 81.6.947.5281
Fax: 81.6.947.5287

Korea
Seoul
LSI Logic Corporation of Korea Ltd
Tel: 82.2.528.3400
Fax: 82.2.528.2250

The Netherlands
Eindhoven
LSI Logic Europe Ltd
Tel: 31.40.265.3580
Fax: 31.40.296.2109

Singapore
Singapore
LSI Logic Pte Ltd
Tel: 65.334.9061
Fax: 65.334.4749

Sweden
Stockholm
LSI Logic AB
♦ Tel: 46.8.444.15.00
Fax: 46.8.750.66.47

Taiwan
Taipei
LSI Logic Asia, Inc.
Taiwan Branch
Tel: 886.2.2718.7828
Fax: 886.2.2718.8869

United Kingdom
Bracknell
LSI Logic Europe Ltd
♦ Tel: 44.1344.426544
Fax: 44.1344.481039

♦ Sales Offices with Design Resource Centers

To receive product literature, visit us at http://www.lsilogic.com

ISO 9000 Certified

AC
Printed in USA
Order No. I15044
Doc. No. DB08-000160-00