

# LSI403US Digital Signal Processor

## Ultra-Sleek Package (7mm x 7mm)

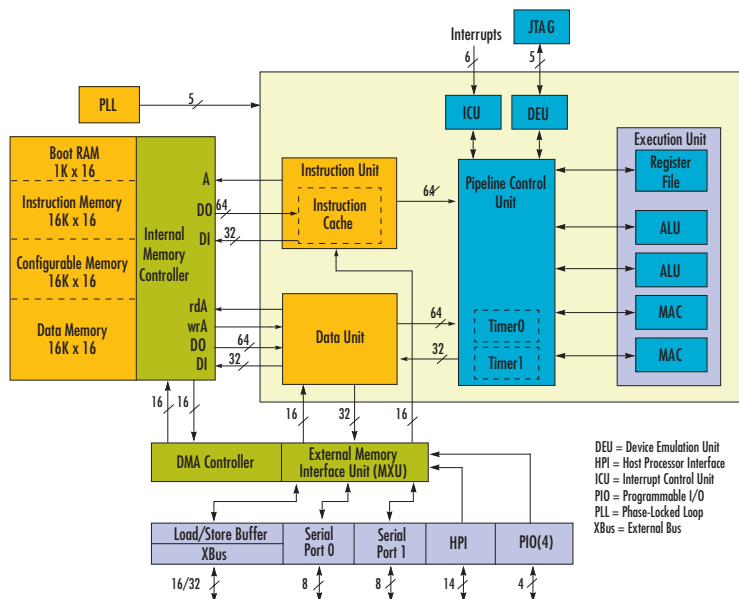


Figure 1.  
LSI403US  
Functional Block  
Diagram

### OVERVIEW

The LSI403US is an extremely low power 16-bit fixed-point digital signal processor (DSP) based on the LSI Logic ZSP400 DSP core, running less than 250 $\mu$ W per DSP MIPS (MMAC). The device is packaged in an Ultra-sleek 144-pin LPGA package which is 7mm x 7mm in size. LSI403US is designed for consumer handheld applications such as VoWiFi and Audio. The LSI403US is capable of a maximum clock rate of 150 MHz for 600 MIPS peak performance and sustained effective throughput of 300 DSP MIPS (MMACs). The device is also software compatible with all other products in the ZSP architecture, and offers an unrivaled combination of code density, performance and ease of use.

### MEMORY

The internal memory structure of the LSI403US comprises of 16K words of instruction memory, 16K words of data memory, 16K words of configurable memory for instruction or data, 1K words of memory for bootloading and interrupt support and peripherals.

### DMA

The DMA controller of the LSI403US supports zero-overhead instruction or data transfers to or from the entire 48K words of internal RAM to the memory interface unit, host processor interface, or a serial port. The eight DMA channels are segmented between four "indexed" and four "non-indexed" channels. Indexed channels have the ability to buffer data from either of the serial TDM interfaces, and non-indexed channels perform sequential accesses to or from internal memory. All DMA channels feature an auto-reload capability to restart transfers with no processor overhead.

### FEATURES

- 150 MHz operation at 1.2V
- 2 high-speed serial/TDM ports (T1/E1 framer, H.100/H.110 bit stream compatible)
- Low power dissipation (50mW typical at 150 MHz)
- Sleep power mode consumes <20mW/MHz
- 48K words on-chip RAM
- 8-channel DMA controller
- On-board PLL for clock generation
- 2 on-board timers
- 8-bit host processor interface with hardware byte pack/unpack
- IEEE 1149.1-compliant JTAG port for in-system debug
- 144 LPGA Package (7mm x 7mm)
- Available in 120 or 150 MHz versions

### BENEFITS

- 300 MMAC sustained DSP performance at 150 MHz
- Direct interfacing to standard telecommunications interfaces, reducing system cost
- Low power per voice or audio channel
- Suitable for very low power applications
- High data throughput without processor overhead
- Flexibility to optimize power consumption
- High data bandwidth to off-chip devices
- Simple interfacing to industry-standard micros
- Low overhead on chip debug
- Ideal for low-cost VoIP designs

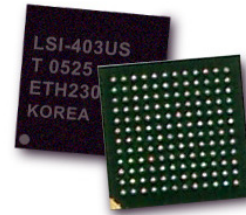
# LSI403US: Digital Signal Processor - Ultra-Sleek Package (7mm x 7mm)

## TIMERS

The LSI403US has two identical 16-bit on board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit prescaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

## TDM SERIAL PORTS

The LSI403US provides two identical synchronous serial ports that support 8- or 16-bit active or passive transfers, which can be either burst or continuous, with a maximum clock speed of one-half the processor clock. Both serial ports support m- and A-law hardware companding and provide the programmable feature of a TDM (time division multiplex) mode that is compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals.



## HOST PROCESSOR INTERFACE (HPI)

The Host Processor Interface, or HPI, is an asynchronous 8-bit parallel port that is used to interface with off-chip devices. It is compatible with both Motorola and Intel style memory interfaces, and supports word transfers. The maximum transfer rate for the HPI is one-third of the processor clock frequency. The HPI includes hardware support to pack/unpack bytes to/from 16-bit words, removing the overhead of this task from the ZSP400 core.

For more information and sales office locations, please visit the LSI Logic web sites at:

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