WT65F5
(FLASH MEMORY Type)
USB Micro Controller

REV. 0.99j

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GENERAL DESCRIPTION

The WT65F5 is highly integrated Micro controller with Universal Serial Bus (USB) interface. It contains an 8051 based CPU core, 64K bytes Flash memory, 2304 bytes (2K+256 bytes) RAM, USB transceiver, Serial bus Interface Engine (SIE), System Interface Logic (SIL) and transmit / receive FIFOs. The USB function supports low/full-speed data rate (1.5M & 12M bps), suspend / resume mode, control / interrupt/ bulk transfer and is fully compliant with the USB specification version 1.1.

FEATURES

- Built-in 8051 8-bit CPU
- 64K bytes flash memory, 2304 bytes SRAM
- PLL build in and can be disabled to use external crystal oscillator frequency
- Complete USB Specification V.1.1 compatibility:
  - Supports low/ Full-speed (1.5M/ 12Mbps) data rate transfer
  - Three 8-byte transmit FIFOs and two 8-byte receive FIFO
  - Support endpoint0 for control IN/OUT, endpoint1 for INT IN or Bulk IN, endpoint2 for INT IN or Bulk IN, and endpoint 3 for INT OUT or Bulk OUT
  - Support Suspend / Resume operation
  - Supports USB remote wakeup
- Power-saving idle and powerdown modes
  - Level detect interrupt mode for the automatic powerdown mode exit
- Built-in power-on reset and low-voltage reset
- Built-in 3.3V regulator for USB transceiver
- One full duplex serial port
- Three 16-bit timer/counter
- Eight-Source, two level interrupt capability.

Package information

Package Type	Part Number
LQFP 48	WT65F5-LQ48
SOP 28	WT65F5-S28

PIN ASSIGNMENT and DESCRIPTION

Table 1. WT65F5 Pins Description

Pin No.				Pin Name	I/O	Description
Die	48		28			
1	1			P20/ A8	I/O	Port 2: function is the same as that of the standard 8052; or A8 address signal of uP. Pull-up internal
2	2			P21/ A9	I/O	Port 2: function is the same as that of the standard 8052; or A9 address signal of uP. Pull-up internal
3	3			P22/ A10	I/O	Port 2: function is the same as that of the standard 8052; or A10 address signal of uP. Pull-up internal
4	4			P23/ A11	I/O	Port 2: function is the same as that of the standard 8052; or A11 address signal of uP. Pull-up internal
5	5			P24/ A12	I/O	Port 2: function is the same as that of the standard 8052; or A12 address signal of uP. Pull-up internal
6	6			P25/ A13	I/O	Port 2: function is the same as that of the standard 8052; or A13 address signal of uP. Pull-up internal
7	7			P26/ A14	I/O	Port 2: function is the same as that of the standard 8052; or A14 address signal of uP. Pull-up internal
8	8			P27/ A15	I/O	Port 2: function is the same as that of the standard 8052; or A15 address signal of uP. Pull-up internal
9	9		5	RST	I	Reset: A high on this pin for two machine cycles while the ocillator is runing resets the device. Pull Low internal
10				P41	I/O	Port 4: bit addressible. Pull-up internal
11	10		6	P10/ T2	I/O	Port 1: function is the same as that of the standard 8052; or T2: Timer 2 external input. Pull-up internal
12	11		7	P11/ T2EX	I/O	Port 3: function is the same as that of the standard 8052; or T2EX: Timer 2 Cature/ Reload triggert. Pull-up internal
13	12		8	P12	I/O	Port 1: function is the same as that of the standard 8052; Pull-up internal. When low, EXT0_INT flag is set to high.
14				GND	P	Ground

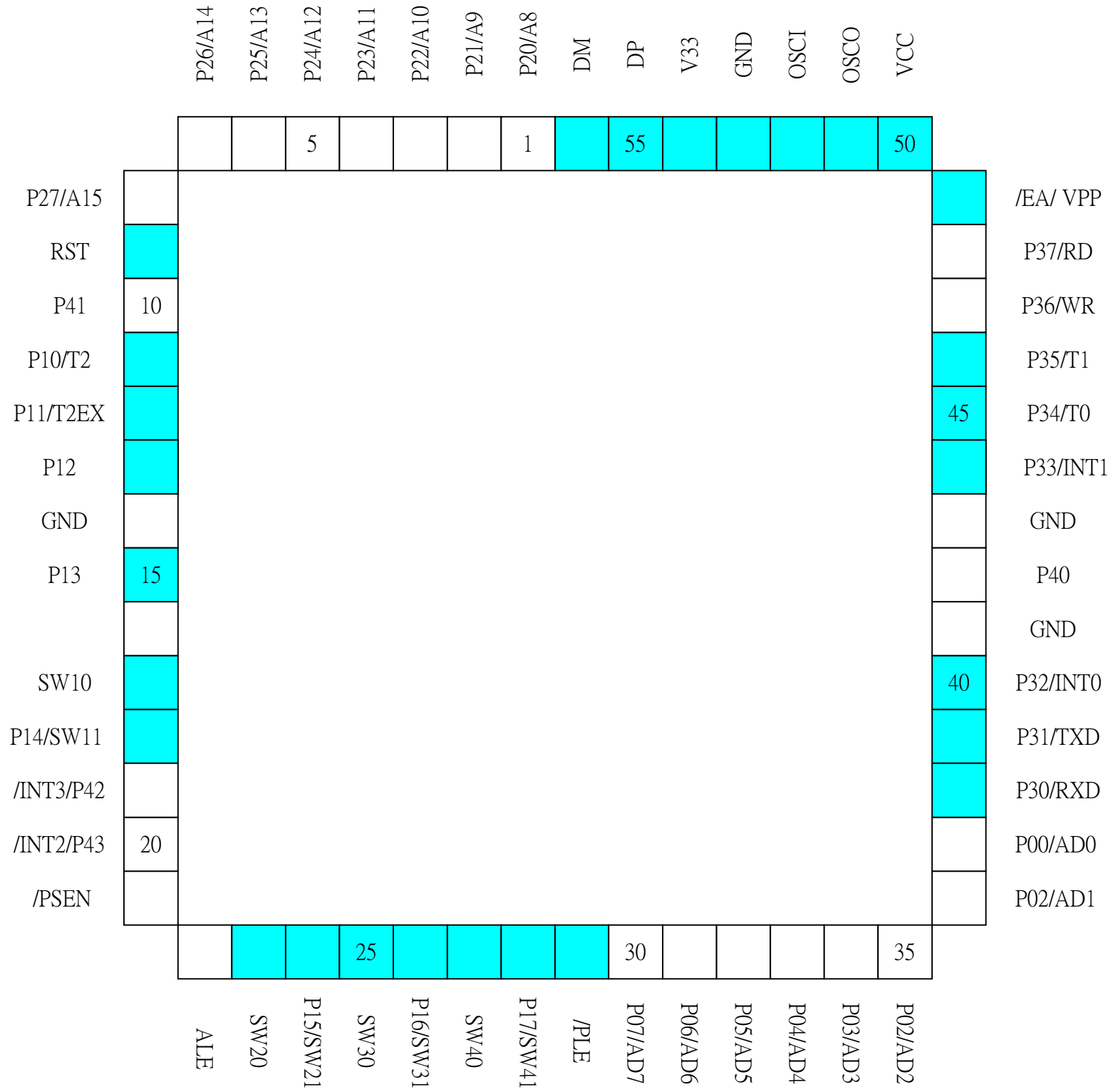
15	13		9	P13	I/O	Port 1: function is the same as that of the standard 8052; Pull-up internal. When low, EXT0_INT flag is set to high.
16				N.C.		
17	14		10	SW10	I/O	SW10 of analog switch (Transmission Gate)
18	15		11	P14/ SW11	I/O	Port 1: function is the same as that of the standard 8052; or SW11 of analog switch (Transmission Gate) Pull-up internal. When low, EXT0_INT flag is set to high.
19	16			/INT3/ P42	I	External Interrupt3: An extra interrupt input source. Or Port 4: bit addressible. Pull High internal.
20	17			/INT2/ P43	I	External Interrupt2: An extra interrupt input source. Or Port 4. Pull High internal.
21				/PSEN	O	Program Store Enable, Active low. Pull-up internal. /PSEN enables the external ROM data in the Port0 address/ data bus during fetchand MOVC operation.
22	18			ALE	O	Address Latch Enable: Active High, ALE is used to enable the address latch that seperates the address from the data on port 0. Pull-up internal.
23	19		12	SW20	I/O	SW20 of analog switch (Transmission Gate)
24	20		13	P15/ SW21	I/O	Port 1: function is the same as that of the standard 8052; SW21 of analog switch (Transmission Gate) ; Pull-up internal. When low, EXT1_INT is set to high.
25	21		14	SW30	I/O	SW30 of analog switch (Transmission Gate)
26	22		15	P16/ SW31	I/O	Port 1: function is the same as that of the standard 8052; SW21 of analog switch (Transmission Gate); Pull-up internal. When low, EXT1_INT is set to high.
27			16	SW40	I/O	SW40 of analog switch (Transmission Gate)
28	23		17	P17/ SW41	I/O	Port 1: function is the same as that of the standard 8052; SW21 of analog switch (Transmission Gate); Pull-up internal. When low, EXT1_INT is set to high.
29	24		18	/PLE	I	Internal PLLx8 Enable for 6MHz Crystal Oscilator, Low Active. Internal PLLx8 be disabled and the Clock (except CPU clock) is same as the Crystal frequency when /PLE is High.

30	25			P07/ AD7	I/O	Port 0: function is the same as that of the standard 8052; or A7/D7 Address/Data Bus of uP. Pull- Low internal
31	26			P06/ AD6	I/O	Port 0: function is the same as that of the standard 8052; or A6/ D6 Address/Data Bus of uP. Pull- Low internal
32	27			P05/ AD5	I/O	Port 0: function is the same as that of the standard 8052; or A5/D5 Address/Data Bus of uP. Pull- Low internal
33	28			P04/ AD4	I/O	Port 0: function is the same as that of the standard 8052; or A4/D4 Address/Data Bus of uP. Pull- Low internal
34	29			P03/ AD3	I/O	Port 0: function is the same as that of the standard 8052; or A3/D7 Address/Data Bus of uP. Pull- Low internal
35	30			P02/ AD2	I/O	Port 0: function is the same as that of the standard 8052; or A2/D2 Address/Data Bus of uP. Pull- Low internal
36	31			P01/ AD1	I/O	Port 0: function is the same as that of the standard 8052; or A1/D1 Address/Data Bus of uP. Pull- Low internal
37	32			P00/ AD0	I/O	Port 0: function is the same as that of the standard 8052; or A0/D0 Address/Data Bus of uP. Pull- Low internal
38	33		19	P30/ RXD	I/O	Port 3: function is the same as that of the standard 8052; or RXD for UART. Pull-up internal
39	34		20	P31/ TXD	I/O	Port 3: function is the same as that of the standard 8052; or RXD for UART. Pull-up internal
40	35		21	P32/ /INT0	I/O	Port 3: function is the same as that of the standard 8052; or External Interrupt INT0. Pull-up internal
41				GND	P	Ground
42				P40	I/O	Port 4: bit addressible. Pull High internal.
43				GND	P	Ground
44	36		22	P33/ /INT1	I/O	Port 3: function is the same as that of the standard 8052; or External Interrupt INT0. Pull-up internal
45	37		23	P34/ T0	I/O	Port 3: function is the same as that of the standard 8052; or Timer 0 external input. Pull-up internal

46	38		24	P35/ T1	I/O	Port 3: function is the same as that of the standard 8052; or Timer 0 external input. Pull-up internal
47	39			P36/ /WR	I/O	Port 3: function is the same as that of the standard 8052; or Write signal of uP. Pull-up internal
48	40			P37/ /RD	I/O	Port 3: function is the same as that of the standard 8052; or Read signal of uP. Pull-up internal
49	41		25	EA	I	Internal PLLx6 Enable for 6MHz Crystal Oscilator, Low Active. Internal PLLx6 be disabled and the Clock (except CPU clock) is same as the Crystal frequency when EA is High.
50	42		26	VCC	P	Power Input
51	43		27	OSCO	O	Crystal output
52	44		28	OSCI	I	Crystal input, can be driven by an extrnal clock
53	45		1	GND	P	Ground
54	46		2	V33	O	3.3 Voltage output
55	47		3	DP	I/O	USB D+ signal.
56	48		4	DM	I/O	USB D- signal.

2.1 Pin Configuration

Die Pin Arrangment



3 Functional Description

The WT65F5 is highly integrated Micro controller with Universal Serial Bus (USB) interface. It contains an 8051 based CPU core, 64K bytes Flash memory, 2304 bytes (2K+256 bytes) RAM, USB transceiver, Serial bus Interface Engine (SIE), System Interface Logic (SIL) and transmit / receive FIFOs. The USB function supports low/full-speed data rate (1.5M & 12M bps), suspend / resume mode, control / interrupt/ bulk transfer and is fully compliant with the USB specification version 1.1.

Operations of the USB interface and special function are controlled through the use of external function registers (XFRs) , special function registers (SFRs), SIE, SIL, FIFOs and 8051 microcontroller that are described in the following sections. Figure 1 shows the main functional blocks of the WT65F5 USB module and how they interface with the 8051 CPU.

3.1 WT65F5 Address Space Mapping

The WT65F5 has five address spaces : a program memory space, an internal data memory space, a special function register space, an external function register space, and a register file. Table 2 shows the addressing mapping of the WT65F5.

Table 2. Addressing mapping

Memory Type	Size	Location	Data Addressing
Flash/ROM Code	64K bytes	0000H-FFFFH	Indirect using MOVC instruction
Extra external RAM	(2048+256)-32 Bytes	0020H—08FFH	Indirect using MOVX instruction
External Function Register	32 bytes	00H-1FH	Indirect using MOVX instruction
Internal Data	128 bytes	00H-7FH	Direct, Indirect
	128 bytes	80H-FFH	Indirect
SFRs	128 bytes	80H-FFH	Direct
Register File (1)	8 bytes	R0-R7	Register

Note:

Direct: Direct Byte Addressing

Indirect: Indirect Byte Addressing

(1): Please refer to 8052 data sheet for bit definition of each SFR.

3.2 WT65F5 SFR & XFR Address Space

The special function registers (SFRs) reside in this optimized 8052 microcontroller core. SFR address mapping lists the location of all the WT65F5 SFRs. Please refer to the 8052 data sheet for bit definition of each SFR.

The external function registers (XFRs) reside inside the XFR module. The instructions, MOVX @Rr, A and MOVX A, @Rr can be used for data movement between the XFRs and accumulator of the 8052 at the address 0000H—00FFH. When the instruction, MOVX @Rr, A or MOVX A, @Rr, is executed, the address contained in R0 or R1 registers is latched by ALE signal and then the direction of data movement between the XFRs and the 8052 can be controlled by the signals $\overline{WR}$ or $\overline{RD}$ subsequently generated by the 8052. The high byte address is tied to 00H at MOVX @Rr, A and MOVX A, @Rr instruction cycle.

Another instructions MOVX DPTR, A and MOVX A, DPTR can be used for data movement between the XFRs and accumulator of the 8052 at the address 0000H—08FFH.

The external function registers(XFR) is accessed by 8052 by MOVX instruction. Table XFR address mapping lists the location of all the WT65F5 XFR.

Table 3. WT65F5 Special Function Register (SFR) address mapping

Data Address	Register Name	Description
80H	P0	Port 0
81H	SP	Stack Point
82H	DPL	Data Point Low
83H	DPH	Data Point High
87H	PCON	Power Control Register
88H	TCON	Timer Control Register
89H	TMOD	Timer Mode Register
8AH	TL0	Timer 0 Low Order
8BH	TL1	Timer 1 Low Order
8CH	TH0	Timer 0 High Order
8DH	TH1	Timer 1 High Order
8EH	AUXR	Auxiliary, Bit1:EN_XMEM Bit0:AO
90H	P1	Port 1
98H	SCON	Serial Control
99H	SBUF	Serial Buffer
A0H	P2	Port 2

A8H	IE	Interrupt Enable Register
B0H	P3	Port 3
B8H	IP	Interrupt Priority Register
C0H	XICON	External interrupt control
C8H	T2CON	Timer 2 control
CAH	RCAP2L	T2 Capture Low
CBH	RCAP2H	T2 Capture High
CCH	TL2	T2 reg. High
CDH	TH2	T2 reg. Low
D0H	PSW	Program Status Word
D8H	P4	Port 4
E0H	ACC	Accumulator
F0H	B	B Register

**The SFR is functional compatible to W78E58 but FE is redesided to PCON bit 5.

Table 4. External Function Register (XFR) address mapping

Data Address	**Register Name**	**Description**
00H	FADDR	Function Address Register
01H	USBI	USB Interrupt Register
02H	USBIE	USB Interrupt Enable Register
03H	SIEI	SIE Interface Register
04H	------	Reserved for testing
05H	EPINDEX	Endpoint Index Register
06H	EPCON	Endpoint Dataflow Control Register
07H	WDTRST	Watch Dog Timer Register
08H	TXDAT	Transmit FIFO Data Register
09H	TXCON	Transmit FIFO Control Register
0AH	TXFLG	Transmit FIFO Flag Register
0BH	TXCNT	Transmit FIFO Byte Count Register
0CH	TXSTAT	Endpoint Transmit Status Register
11H	USBFI	USB Function Interrupt regiater
12H	USBFIE	USB Function Interrupt Enable Register
18H	RXDAT	Receive FIFO Data Register
19H	RXCON	Receive FIFO Control Register
1AH	RXFLG	Receive FIFO Flag Register
1BH	RXCNT	Receive FIFO Byte Count Register

1CH	RXSTAT	Endpoint Receive Status Register
1DH	CLKCON	CPU clock rate selection Register
1EH	SWCON	Analoge Switch Control Register
1FH	USBCON	USB L/F, RD+, RD- Control Register

3.3 Clock Unit

Two different external clock frequencies can be applied to WT65F5, they are 6MHz and non-6MHz. WT65F5 contains a PLLx8 circuit which can multiply the external 6MHz crystal oscillator to be the 48MHz clock for USB Functions and a PLLx6 circuit which multiplies from the external clock oscillator for CPU function. When PLLx8 is disabled (i.e., by inactivating /PLE) and PLLx6 (i.e., by inactivating /EA) is disabled, an external clock or an on-chip oscillator with crystal (or ceramic resonator) can be applied directly as the clock source.

There are four different internal clock speed to be applied to WT65F5 USB functions, 1.5MHz, 6MHz, 12MHz, and 48MHz. For USB full speed mode, 12MHz and 48MHz are used. For USB low speed mode, 1,5MHz and 6MHz are used. There is one internal clock speed (external clock x 6) for WT65F5 CPU core. This CPU clock can be generated from PLLx6. The clock clk_dx is used for FIFO and SIL.

The Clock Table shows clk_sie, usb_clk and clk_dx generation. The Clkcon usage table shows clk_cpu generation.

Table 5. Clock Table

	PLLx8	**PLLx6**	**clk_osc**	**clk_sie**	**usb_clk**	**clk_dx**
USB Full	On	On	6M	48M	12M	12M
		Off				
	Off	On	48M			
		Off				
USB Low	On	On	6M	6M	1.5M	12M
		Off		6M	1.5M	12M
	Off	On		6M	1.5M	18M
		Off		6M	1.5M	6M
non-USB	NC	On	6M	NC	NC	18M
		Off	Any			clk_osc%2

Note :

1. clk_dx must be >= usb_clk
2. clk_dx must be >= clk_cpu%3
3. Set or Clear USB function through XFR:USBCON.USBDE & SPLF register

Table 6. XFR:Clkcon usage

XFR:CLKCON	clk_cpu
00	PLLx6 or clk_osc
01	PLLx6%2 or clk_osc%2
10	PLLx8%2 or clk_osc%2
11	PLLx8%4 or clk_osc%4

3.4 Reset

The reset can be initiated by low voltage reset, or an USB-initiated reset or a high level of signal on the RESET pin. The low voltage reset can be controlled by the XFR:USBCON.LVRSEL1 & LVRSEL2 to enable the POR_RST and LVR2 modules. The POR_RST generates internal reset pulse while VCC < 3.5V. The LVR2 generates internal reset pulse while VCC < 2.1V.

3.5 Powerdown

Table 7. SFR:PCON structure

SFR:PCON-Power control(87H)

SMOD	-	-	-	-	-	PD	IDL

SMOD: Double baud rate bit. When set to '1', the baud rate is double when the serial port is being used in either modes 1,2,3

PD: Power down mode bit.

IDL: Idle mode bit.

Powerdown is set from 8052 CPU by setting PCON.1. Powerdown can be applied to USB function in the ISR of interrupt caused by active SUSPEND signal. The Suspend signal that sets PCON.1 is the last executed instruction prior to entering powerdown mode. Once in the powerdown mode, the pwrdwn signal is active and the oscillator is stopped. The contents of the on-chip RAM, the Special Function Registers and USB External Function Registers are saved. Hardware reset and activation of any enabled interrupt is the ways of exiting the powerdown mode. Powerdown mode should be used for USB suspend operation.

The WT65F5 can initiate resume signaling to the USB host through remote wakeup register **XFR:SIEI.WAKEUP** of the USB function while it is in powerdown mode. While in powerdown mode, remote wakeup has to be initiated through assertion of an enabled **USBFIE**. In the ISR for the interrupt activated by active **USBFI** signal, or an enabled USB resume interrupt signal **(RESUME**). Upon completion of the ISR, program execution continues with the instruction immediately following the instruction that activated the powerdown.

3.6 Interrupt INT0, INT1, INT2, INT3

INT0:

INT0 is activated by Port P32 when XFR:USBFIE=”xxxxxx00”, otherwise activated by USBFI. USBFIE.EXT0_INT is level triggered by Port P12, P13 and P14. USBFIE.EXT1_INT is level triggered by Port P15, P16 and P17.

INT1:

INT1 is activated by Port P33when XFR:USBIE=”x0000000”, otherwise activated by USBI.

INT2 & INT3:

INT2 and INT3 are similar ti those of external interrupt INT0 and INT1 in the standard 80C52. INT2 is activated by Port P43; INT3 is activated by Port P42. The function of these interrupts are determined by SFR:XICON register. The XICON register is bit-addressable but is not a standard register in the standard 80c52. To set/clear bits in the XICON register, one can use the “SETB(/CLR) bit” instruction. For example, “SET 02CH”

Table 8. SFR:XICON structure

SFR:XICON-external interrupt control(C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Table 9. 8052 Interrupt source

Eight-source interrupt information

Interrupt source	Vector address	Polling sequence within priority level	Enable required settings	Interrupt type Edge/Level
INT0	03H	0(ighest)	IE.0	TCON.0
Timer	0BH	1	IE.1	-

INT1	13H	2	IE.2	TCON.2
Timer1	1BH	3	IE.3	-
UART	23H	4	IE.4	-
Timer2	2BH	5	IE.5	-
INT2	33H	6	XICON.2	XICON.0
INT3	3BH	7(lowest)	XICON.6	XICON.3

3.7 Port 0,1,2,3,4

Table 10. SFR:AUXR structure

SFR:AUXR-Auxiliary register(8EH)

-	-	-	-	-	-	EN_XMEM	AO

EN_XMEM : Enable external memory access

AO: Turn off ALE output

P0:

If SFR:AUXR.EN_XMEM='1', external data memory is enabled and Port 0 output low byte address and data when at MOVX cycle; otherwise, Port 0 output SFR register value only.

P1:

P1 operates as 8052 Port P1 when SWCON is disabled. At 'Switch' function, P1(7:4) should not output '0' to corresponding enabled SWx1.

P2:

If SFR:AUXR.EN_XMEM='1', external data memory is enabled and Port 2 output high byte address when at MOVX cycle; otherwise, Port 2 output SFR register value only.

P3:

P3 operates as 8052 Port 3 except P32 and P33. See INT0 and INT1 for details.

P4:

P4 operates as 4-bit I/O Ports. It can be used as general I/O pins or external interrupt input sources INT2 by P4.3 and INT3 by P42.

3.8 FIFO Block

The WT65F5 supports four endpoints. Endpoint 0 contains 8 bytes FIFO each for transmit and receiv. The endpoint1, endpoint2 and endpoint3 are generic endpoints can be programmable to be an interrupt/ bulk and IN/OUT transfer, each endpoints has an 8 bytes FIFO. The EPINDEX register selects the endpoint for any given data transaction.

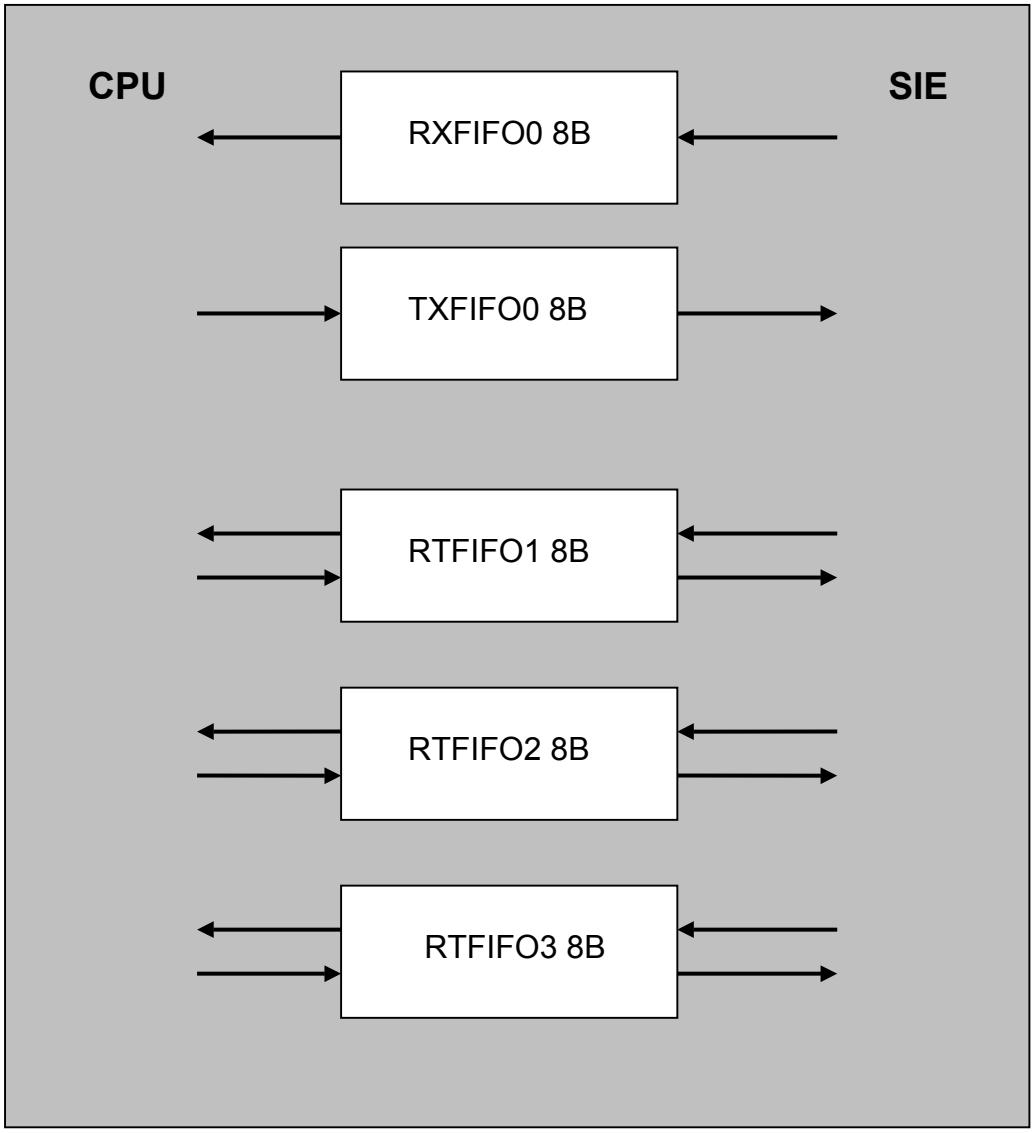


Figure 1. FIFO Block Diagram

3.9 SIL Block

The SIL operates in conjunction with the 8052 CPU to provide the capabilities of controlling the operation of the FIFOs, monitoring the status of the data transactions, transferring event control to the 8052 CPU through interrupt requests

at the appropriate moment, initiating resume signaling to USB bus while the WT65F5 is in powerdown mode . Operation of the SIL is controlled through the use of external function registers. The SIL module is referred to WT655601A and modified for Full speed function.

XFR:EPCON.RXSTL is used to stall the receive endpoint. Clear this bit when the host has intervened through commands sent down endpoint 0 or clear by hardware when a SETUP token received. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and RXSETUP is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP token by a control endpoint. TXSTL operates as the same way.

XFR:EPCON.NR_EN is used to ignore invalid IN/OUT transaction. When firmware complete Status Transaction, set this bit to '1' to ignore following IN/OUT packet. This function prevent Endpoint 0 to response NAK, ACK or STALL to unsupported IN/OUT transaction.

3.10 Analog Transmission Switches and Ports

The SW1, SW2, SW3 and SW4 are enable by XFR:SWCON.

When SW1_E is '1', SWPAD enable transmission gate to switch on.

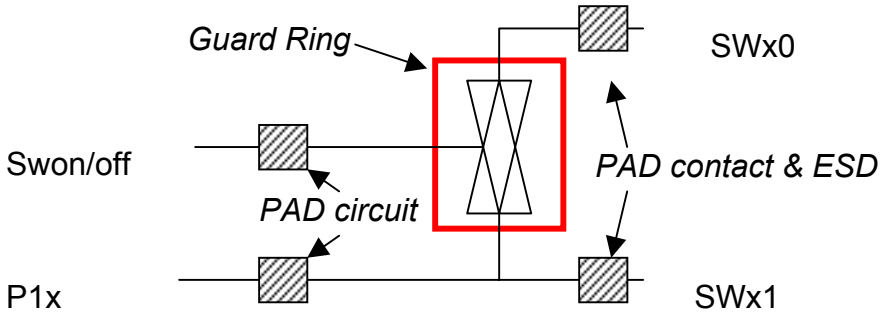


Figure 2. SWPAD Block Diagram

- P1x is in input mode as Switch is on
- P1x can be in input or output mode as switch is off.

3.11 V33 Regulator

3.3V regulator with EN pin is controlled by XFR:USBCON.V33EN

3.12 Low voltage reset

Set XFR:USBCON.LVRSEL1 and USBCON.LVRSEL2 to enable LVR1 or LVR2. The initial value of LVRSEL1 and LVRSEL2 is '0'.

1. LVR1 : Low voltage reset for VDD=5V
2. LVR2 : Low voltage reset with EN pin for VDD = 2.4V

3.13 USB Transceiver

Set XFR:USBCON to control transceiver. Bit USBDE and V33EN must be '1' to enable tarnsceiver function. Set DMR/ DPR to pull up D+/ D-. The initial values of USBCON are USBDE='1' and V33EN='1', others are all '0'. The speed of USB is low speed. The D+/D- are both not pull-up.

4.USB XFR lists

FADDR Address: 00H
Reset State: 0000 0000B

Function Address Register. This XFR holds the address for the USB function. During bus enumeration, it is written with a unique value assigned by the host.

Table 11. Function Address Register

7	0
---	A6:0

Bit Number	Bit Mnemonic	Function
7	---	Reserved: Write zero to this bit.
6:0	A6:0	7-bit Programmable Function Address: This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only.

USBI Address: 01H
Reset State: x000 0000B

USB Interrupt Register. Contains keyboard, PS/2 mouse, USB suspend, USB resume, USB Function Transmit and Receive Done interrupt flags. A '1' indicates that an interrupt is actively pending. All bits are cleared after a read.

Table 12. USB Interrupt Register

7							0
---	RESUME	SUSPEND	USBRT3INT	USBRx0INT	USBRT2INT	USBRT1INT	USBTx0INT

Bit Number	Bit Mnemonic	Function
7	--	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
6	RESUME	USB SIE has detected a RESUME signaling on the USB lines. This interrupt is used to terminate the powerdown mode.
5	SUSPEND	USB SIE has detected a SUSPEND signaling on the USB lines. The corresponding ISR should put the whole chip into powerdown mode.
4	USBRT3INT	Function Receive /Transmit Done Flag for endpoint 3.
3	USBRx0INT	Function Receive Done Flag for endpoint 0.
2	USBRT2INT	Function Receive /Transmit Done Flag for endpoint 2.
1	USBRT1INT	Function Receive /Transmit Done Flag for endpoint 1.
0	USBTx0INT	Function Transmit Done Flag for endpoint 0.

USBIE

Address: 02H
Reset State: 0000 0000B

USB Interrupt Enable Register.

Table 13. USB Interrupt Enable Register

7							0
NAKINT_IE	RESUME_IE	SUSPEND_IE	RT3INT_IE	Rx0INT_IE	RT2INT_IE	RT1INT_IE	Tx0INT_IE

Bit Number	Bit Mnemonic	Function
7	NAKINT_IE	Not ACK interrupt enable; Enable NAK interrupt for RX or TX.
6	RESUME_IE	RESUME Interrupt Enable.
5	SUSPEND_IE	SUSPEND Interrupt Enable.
4	RT3INT_IE	Function Receive/Transmit Done Interrupt Enable 2: Enable receive/transmit done interrupt for endpoint 2 (USBRT3INT).
3	Rx0INT_IE	Function Receive Done Interrupt Enable 0: Enable receive done interrupt for endpoint 0 (USBRx0INT).
2	RT2INT_IE	Function Receive/Transmit Done Interrupt Enable 2: Enable receive/transmit done interrupt for endpoint 2 (USBRT2INT).
1	RT1INT_IE	Function Receive/Transmit Done Interrupt Enable 1: Enable receive/transmit done interrupt for endpoint 1 (USBRT1INT).
0	Tx0INT_IE	Function Transmit Done Interrupt Enable 0: Enable transmit done interrupt for endpoint 0 (USBTx0INT).

For all bits, a ‘1’ means the interrupt is enabled and will cause an interrupt to be signaled to the microcontroller. A ‘0’ means the associated interrupt source is disabled and cannot cause an interrupt.

USBFI Address: 11H
Reset State: xxxxxx00B

USB Function Interrupt Register. If any input pin of P12~P17 is low it will set interrupt flags. A '1' indicates that an interrupt is actively pending. All bits are cleared after a read

Table 14. USB Function Interrupt Register

7							0
---	---	---	---	---	---	EXT1_INT	EXT0_INT

Bit Number	Bit Mnemonic	Function
7:2	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
1	EXT1_INT	External1 Interrupt Flag. This bit is set when any Input pin - (P15, P16, P17) is low.
0	EXT0_INT	External0 Interrupt Flag. This bit is set when any Input pin - (P12, P13, P14)is low.

USBFIE Address: 12H
Reset State: xxxxxx00B

USB Function Interrupt Enable Register.

Table 15. USB Function Interrupt Enable Register

7							0
---	---	---	---	---	---	EXT1_IE	EXT0_IE

Bit Number	Bit Mnemonic	Function
7:2	---	Reserved:

		Values read from these bits are indeterminate. Write zeros to these bits.
1	EXT1_IE	External1 Interrupt Enable: Enable External1 Interrupt (EXT1_INT). Firmware can set this bit before entering the powerdown mode to enable remote wakeup. External1 Interrupt should be disabled by firmware in normal operation.
0	EXT0_IE	External2 Interrupt Enable: Enable External2 Interrupt EXT0_INT. Firmware can set this bit before entering the powerdown mode to enable remote wakeup. External1 Interrupt should be disabled by firmware in normal operation.

For all bits, a '1' means the interrupt is enabled and will cause an interrupt to be signaled to the microcontroller. A '0' means the associated interrupt source is disabled and cannot cause an interrupt.

SIEI Address: 03H
Reset State: xxxx xxx0B

USB SIE Interface Register.

Table 16. USB SIE Interface Register

7					2	1	0
---	---	---	---	----	---	---	WAKEUP

Bit Number	Bit Mnemonic	Function
7:1	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
0	WAKEUP	This bit is used to initiate a remote wakeup. Set or Clear by firmware to drive resume signaling on the USB lines to the host or upstream hub. Firmware should control the resume duration.

EPINDEX

Address: 05H
Reset State: xxxx xx00B

Endpoint Index Register. This Register identifies the endpoint pair. Its contents select the transmit and receive FIFO pair and serve as an index to endpoint-specific XFRs.

Table 17. Endpoint Index Register

7							0
---	---	---	---	---	---	EPINX1	EPINX0

Bit Number	Bit Mnemonic	Function
7:2	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
1:0	EPINX1:0	Endpoint Index: 00 = Function Endpoint 0. 01 = Function Endpoint 1. 10 = Function Endpoint 2. 11 = Function Endpoint 3.

The value in this register selects the associated bank of endpoint-indexed XFRs including TXDAT, TXCON, TXFLG, TXCNT, TXSTAT, RXDAT, RXCON, RXFLG, RXCNT, RXSTAT and EPCON.

EPCON (Endpoint-indexed)		Address:	06H
	Reset State:	Endpoint 0:	00100101B
		Endpoint 1, 2,3:	00xx0000B

Endpoint Control Register. This XFR configures the operation of the endpoint specified by EPINDEX.

Table 18. Endpoint Control Register

7							0
RXSTL	TXSTL	CTLEP	NR_EN	RXIE	RXEPEN	TXOE	TXEPEN

Bit Number	Bit Mnemonic	Function
7	RXSTL	Stall Receive Endpoint: Set this bit to stall the receive endpoint. Clear this bit ~~only~~ when the host has intervened through commands sent down endpoint 0 or clear by hardware when a SETUP token received. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and RXSETUP is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP token by a control endpoint.
6	TXSTL	Stall Transmit Endpoint: Set this bit to stall the transmit endpoint. This bit should be cleared when the host has intervened through commands sent down endpoint 0 or clear by hardware when a SETUP token received. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid IN token. When this bit is set and RXSETUP is set, the receive endpoint will NAK.
5	CTLEP	Control Endpoint: Set this bit to configure the endpoint as a control endpoint. Only control endpoint is capable of receiving SETUP

		tokens.
4	NR_EN	No Response Enable : When firmware complete Status Transaction, set this bit to '1' to ignore following IN/OUT packet. This function prevent Endpoint 0 to response NAK, ACK or STALL to unsupported IN/OUT transaction.
3	RXIE	Receive Input Enable: Set this bit to enable data from the USB to be written into the receive FIFO. If cleared, the endpoint will not write the received data into the receive FIFO and at the end of reception, but will return a NAK handshake on a valid OUT token if the RXSTL bit is not set. This bit does not affect a valid SETUP token. A valid SETUP token and packet overrides this bit if it is cleared, and place the receive data in the FIFO.
2	RXEPEN	Receive Endpoint Enable: Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to valid OUT or SETUP token. This bit is hardware read-only and has the highest priority among RXIE and RXSTL. Note that endpoint 0 is enabled for reception upon reset.
1	TXOE	Transmit Output Enable: This bit is used to enable the data in TXDAT to be transmitted. If cleared, the endpoint returns a NAK handshake to a valid IN token if the TXSTL bit is not set.
0	TXEPEN	Transmit Endpoint Enable: This bit is used to enable the transmit endpoint. When disabled, the endpoint does not response to a valid IN token. This bit is hardware read only. Note that endpoint 0 is enabled for transmission upon reset.

WDTRST Address: 07H
Reset State: 0000 0000B

Watch Dog Timer Register.

Table 19. WTCH Dog Timer Register

7							0
WDT_DIS				WDT_EN			

Bit Number	Bit Mnemonic	Function
7:4	WDT_DIS	Disable Watch Dog Timer. Set “1010” to disable watch dog timer. WDT_DIS has high priority.
3:0	WDT_EN	Enable Watch Dog Timer. Set “1010” to enable watch dog timer.

TXSTAT Address: 0CH
(Endpoint-indexed) Reset State: 0xxxx000B

Endpoint Transmit Status Register. Contains the current endpoint status of the transmit FIFO specified by EPINDEX.

Table 20. Endpoint Transmit Status Register

7							0
TXSEQ	---	---	---	---	TXVOID	TXERR	TXACK

Bit Number	Bit Mnemonic	Function
7	TXSEQ	Transmit Current Sequence Bit (read, clear -only): This bit will be transmitted in the next PID and toggled on a valid ACK handshake. This bit is toggled by hardware on a valid SETUP token.
6:3	---	Reserved: Write zeros to these bits.
2	TXVOID	Transmit Void (read-only):

		A void condition has occurred in response to a valid IN token. Transmit void is closely associated with the NAK/STALL handshake returned by the function after a valid IN token, due to the conditions that cause the transmit FIFO to be unable or not ready to transmit. Use this bit to check any NAK/STALL handshake returned by the function. This bit does not affect the USBTx*x*INT, TXERR or TXACK bit. This bit is updated by hardware at the end of a non-isochronous transaction in response to a valid IN token.
1	TXERR	Transmit Error (read-only): An error condition has occurred with the transmission. Complete or partial data has been transmitted. The error can be one of the following: 1. Data transmitted successfully but no handshake received. 2. Transmit FIFO goes into underrun condition while transmitting. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXACK bit at the end of data transmission (this bit is mutually exclusive with TXACK).

Bit Number	Bit Mnemonic	Function
0	TXACK	Transmit Acknowledge (read-only): Data transmission completed and acknowledged successfully. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXERR bit at the end of data transmission (this bit is mutually exclusive with TXERR).

RXSTAT Address: 1CH

Reset State: 0000 x000B

Endpoint Receive Status Register. Contains the current endpoint status of the receive FIFO specified by EPINDEX.

Table 21. Endpoint Receive Status Register

7							0
RXSEQ	RXSETUP	STOVW	EDOVW	---	RXVOID	RXERR	RXACK

Bit Number	Bit Mnemonic	Function
7	RXSEQ	Receive Endpoint Sequence Bit (read, clear-only): This bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit will be set (or created) by hardware after reception of SETUP token.
6	RXSETUP	Receive Setup Token (read-, clear-only): This bit is set by hardware when a valid SETUP token has been received. When set, this bit causes received IN or OUT token to be NAKed until the bit is cleared to allow a control transaction. IN or OUT token is NAKed even if the endpoint is stalled (RXSTL or TXSTL) to allow a control transaction to clear a stalled endpoint. Clear this bit upon detection of a SETUP token after the firmware is ready to complete the setup stage of control transaction.
5	STOVW	Start Overwrite Flag (read-only): Set by hardware upon receipt of SETUP token for any control endpoint to indicate that the receive FIFO is being overwritten with new SETUP data. When set, the FIFO state (RXFULL and read pointer) resets and is locked for this endpoint until EDOVW is set. This prevents a prior, ongoing firmware read from corrupting the read pointer as the receive FIFO is being cleared and new data is being written into it. This bit is cleared by hardware at the end of handshake phase transmission of the setup stage. This bit is used only for control endpoint.

4	EDOVW	End Overwrite Flag (read-, clear-only): This flag is set by hardware during the handshake phase of a SETUP stage. It is set after every SETUP packet is received and must be cleared prior to reading the contents of the FIFO. When set, the FIFO state (RXFULL and read pointer) remains locked for this endpoint until this bit is cleared. This prevents a prior, ongoing firmware read from corrupting the read pointer after the new data has been written into the receive FIFO. This bit is only used for control endpoint. **Note:** Make sure the EDOVW bit is cleared prior to reading the contents of the receive FIFO.
3	---	Reserved: Write zero to this bit.
2	RXVOID	Receive Void Condition (read-only): This bit is set when no valid data is received in response to a SETUP or OUT token due to one of the following conditions: 1. The receive FIFO is still locked. 2. The EPCON register RXSTL bit is set. This bit is set and cleared by hardware. This bit is updated by hardware at the end of the transaction in response to a valid OUT token.
1	RXERR	Receive Error (read-only): Set when an error condition has occurred with the reception. Complete or partial data has been written into the receive FIFO. No handshake is returned. The error can be one of the following conditions: 1. Data failed CRC check. 2. Bit stuffing error. 3. A receive FIFO goes into overrun or underrun condition while receiving. This bit is updated by hardware at the end of a valid SETUP or OUT token transaction. The corresponding receive done bit is set when active. This bit is updated with the RXACK bit at the end of data reception and is mutually exclusive with RXACK.
0	RXACK	Receive Acknowledged (read-only): This bit is set when data is received completely into a receive FIFO and an ACK handshake is sent. This read-only bit is updated by hardware at the end of valid SETUP or OUT token transaction. The corresponding receive done bit set when active. This bit is updated with the RXERR bit at the end of data reception and is mutually exclusive with RXERR.

TXDAT Address: 08H

(Endpoint-indexed) Reset State: xxxx xxxxB

Transmit FIFO Data Register. Data to be transmitted by the FIFO specified by EPINDEX is first written to this register.

Table 22. Transmit FIFO Data Register

7							0
TXDAT7:0							

Bit Number	Bit Mnemonic	Function
7:0	TXDAT7:0	Transmit Data Byte (write-only): To write data to the transmit FIFO, write to this register. The write pointer is incremented automatically after a write.

TXCNT Address: 0BH
(Endpoint-indexed) Reset State: 0000 0000B

Transmit FIFO Byte Count Register. This register stores the number of bytes for the data packet in the transmit FIFO specified by EPINDEX.

Table 23. Transmit FIFO Byte Count Register

7				0
---	---	---	---	TXCNT3:0

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Write zeros to these bits.
3:0	TXCNT3:0	Transmit Byte Count (write-only): The number of bytes in the data set being written to the transmit FIFO. When this register is written, TXFULL is set. Write the byte count to this register after writing data set to TXDAT.

To send a status stage after a control write or no data control command or a null packet, write 0 to TXCNT.

TXCON Address: 09H

(Endpoint-indexed) Reset State: 0xxx xxxxB

Transmit FIFO Control Register. Controls the transmit FIFO specified by EPINDEX.

Table 24. Transmit FIFO Control Register

7							0
TXCLR	---	---	---	---	---	---	---

Bit Number	Bit Mnemonic	Function
7	TXCLR	Transmit Clear: Setting this bit flushes the transmit FIFO, resets all the read/write pointers, sets the EMPTY bit in TXFLG, and clears all other bits in TXFLG. After the flush, hardware clears this bit.
6:0	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.

TXFLG Address: 0AH

(Endpoint-indexed) Reset State: xxxx 1000B

Transmit FIFO Flag Register. These flags indicate the status of data packets in the transmit FIFO specified by EPINDEX.

Table 25. Transmit FIFO Flag Register

7							0
---	---	---	---	TXEMP	TXFULL	TXURF	TXOVF

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
3	TXEMP	Transmit FIFO Empty Flag (read-only): Hardware sets this bit when the data set has been read out of the transmit FIFO by SIL. Hardware clears this bit when the empty condition no longer exists. This bit always tracks the current transmit FIFO status. This flag is also set when a zero-length data packet is transmitted.
2	TXFULL	Transmit FIFO Full Flag (read-only): This flag indicates the data set is present in the transmit FIFO. This bit is set after write to TXCNT to reflect the condition of the data set. Hardware clears this bit when the data set has been successfully transmitted.
1	TXURF	Transmit FIFO Underrun Flag (read-, clear-only)*: Hardware sets this flag when an addition byte is read from an empty transmit FIFO. This is a sticky bit that must be cleared through firmware by writing a '0' to this bit. When the transmit FIFO underruns, the read pointer will not advance -- it remains locked in the empty position.
0	TXOVF	Transmit FIFO Overrun Flag (read-, clear-only)*: This bit is set when an additional byte is written to a FIFO with TXFULL = 1. This is a sticky bit that must be cleared through firmware by writing a '0' to this bit. When the transmit FIFO overruns, the write pointer will

		not advance -- it remains locked in the full position.

Note (*): When set, all transmission are NAKed.

RXDAT Address: 18H
Reset State: xxxx xxxxB

Receive FIFO Data Register. Receive FIFO data specified by EPINDEX is stored and read from this register.

Table 26. Receive FIFO Data Register

7							0
RXDAT7:0							

Bit Number	Bit Mnemonic	Function
7:0	RXDAT7:0	Receive Data Byte (read-only): To write data to the receive FIFO, the SIL writes to this register. To read data from the receive FIFO, the 8052 CPU reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively.

RXCNT

Address: 1BH
Reset State: 0000 0000B

Receive FIFO Byte Count Register. This register is used to store the number of byte for the data packed received in the receive FIFO specified by EPINDEX.

Table 27. Receive FIFO Byte Count Register

7				0
---	---	---	---	RXCNT3:0

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Always zeros.
3:0	RXCNT3:0	Byte Count (read-only): The number of bytes in data set being written to the receive FIFO. When this register is written, RXFULL is not set until reception is successfully acknowledged. After the SIL writes a data set to the RXFIFO, it writes the byte count to this register. The 8052 CPU reads the byte count from this register to determine how many bytes to read from the RXFIFO.

RXCON

Address: 19H
Reset State: 0xx0 xxxxB

Receive FIFO Control Register. Controls the receive FIFO.

Table 28. Receive FIFO Control Register

7							0
RXCLR	---	---	RXFFRC	---	---	---	---

Bit Number	Bit Mnemonic	Function
7	RXCLR	Clear the Receive FIFO: Set this bit to flush the entire receive FIFO. All flags in RXFLG revert to their reset states (RXEMP is set; all other flags clear). Hardware clears this bit when the flush operation is complete.
6:5	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
4	RXFFRC	FIFO Read Complete: Set this bit to release the receive FIFO when a data set read is complete. Setting this bit clears the RXFULL bit (in the RXFLG register) corresponding to the data set that was just read. Hardware clears this bit after the RXFULL bit is cleared. All data from this data set must have been read. Note that FIFO Read Complete only works if STOVW and EDOVW are cleared.
3:0	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.

RXFLG

Address: 1AH
Reset State: xxxx 1000B

Receive FIFO Flag Register. These flags indicate the status of data packets in the Receive FIFO.

Table 29. Receive FIFO Flag Register

7							0
---	---	---	---	RXEMP	RXFULL	RXURF	RXOVF

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
3	RXEMP	Receive FIFO Empty Flag (read-only): Hardware sets this bit when the data set has been read out of the receive FIFO. Hardware clears this bit when the empty condition no longer exists. This is not a sticky bit and always tracks the current status. This flag is also set when a zero-length packet is received.
2	RXFULL	Receive FIFO Full Flag (read-only): This flag indicates the data set is present in the receive FIFO. Hardware sets this bit when the data set has been successfully received. This bit is cleared after write to RXCNT to reflect the condition of the data set. Likewise, this bit is cleared after setting of the RXFFRC bit.
1	RXURF	Receive FIFO Underrun Flag (read-, clear-only)*: Hardware sets this bit when an additional byte is read from an empty receive FIFO. This bit is cleared through firmware by writing a '0' to this bit. When the receive FIFO underruns, the read pointer will not advance -- it remains locked in the empty position.
0	RXOVF	Receive FIFO Overrun Flag (read-, clear-only)*: This bit is set when the SIL writes an additional byte to a receive FIFO with RXFULL = 1. This is a sticky bit that must be cleared through firmware by writing a '0' to this

		bit, although it can be cleared by hardware if a SETUP packet is received after an RXOVF error had already occurred. When the receive FIFO overruns, the write pointer will not advance -- it remains locked in the full position.

* When set, all transmission are NAKed.

CLKCON

Address: 1DH
Reset State: xxxx xx00B

Endpoint Index Register. This Register identifies the endpoint pair. Its contents select the transmit and receive FIFO pair and serve as an index to endpoint-specific XFRs.

Table 30. CPU Clock seletion Register

7							0
---	---	---	---	---	---	CPUSEL1	CPUSEL0

Bit Number	Bit Mnemonic	Function
7:2	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
1:0	CPUSEL1:0	CPU clock selection: 00 : PLLx6 or clk_osc 01 : PLLx6%2 or clk_osc%2 10 : PLLx8%2 or clk_osc%2 11 : PLLx8%4 or clk_osc%4

SWCON

Address: 1EH
Reset State: xxxx 0000B

Analog Switch Control Register.

Table 31. Analog Switch Control Register

7							0
---	---	---	---	SW4_E	SW3_E	SW2_E	SW1_E

Bit Number	Bit Mnemonic	Function
3:0	SWx_E	Analog switch enable control bit, A ‘1’ indicates that Analog Switch is enabled and SWx0 is connect to SWx1

USBCON Address: 1FH

Reset State: 0000 0x00B

USB Control Register. Sets this register to control the function of USB Device enable, USB Low speed/ Full Speed control, D+ Pull High resistor On/ Off control and D- Pull High resistor On/ Off control .

Table 32. USB Control Register

7							0
USBDE	LVRSEL2	LVRSEL1	SPLF	USBRSTEN	V33EN	DPR	DMR

Bit Number	Bit Mnemonic	Function
7	USBDE	A‘1’ enable the USB Device, A‘0’ USB Device disabled. When set to ‘0’, transceiver is powered down.
6	LVRSEL2	A‘1’ enable LVR2;a ‘0’ disable LVR2
5	LVRSEL1	A‘1’ enable LVR1;a ‘0’ disable LVR1
4	SPLF	A‘1’ set the USB to Full Speed; a ‘0’ set to Low Speed
3	USBRSTEN	USB Reset Enable, a ‘1’ enable.
2	V33EN	V33 Power Enable; A‘1’ set the V33 Power output to the V33 Pin. When set to ‘0’, regulator and transceiver are powered off.
1	DPR	A‘1’ set the D+ internal Pull up resistor ON, ie D+ pull up to V3.3 in Full Speed mode.
0	DMR	A‘1’ set the D- internal Pull up resistor ON, ie D- pull up to V3.3 in Low Speed mode.

5 AC and DC Specification

(VCC=5V, GND=0V, TA=25°C, F_{osc}=6MHz, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Active current	I_{CC}			10	mA	
Power-down current	I_{PD}		0.3	0.5	mA	
Input high voltage (except XTAL1, RESET)	V_{IH}	0.2VCC+0.9		VCC+0.5	V	
Input high voltage (XTAL1, RESET)	V_{IH1}	0.7VCC		VCC+0.5	V	
Input low voltage (except RESET)	V_{IL}	-0.5		1.2	V	
Input low voltage (RESET)	V_{IL1}	0		2.4	V	
Output high voltage	V_{OH}	VCC-0.3			V	I_{OH}=-25μA *(Note)*
		VCC-0.7			V	I_{OH}=-65μA *(Note)*
		VCC-1.5			V	I_{OH}=-100μA *(Note)*
Output low voltage	V_{OL}			0.45	V	I_{OL}=4mA *(Note)*
Low voltage reset	V_{LVR}	3.1	3.4	3.7	V	
Input high leakage current	I_{IH}			300	nA	V_{IH}=5V
RESET pull-down resistor	R_{RST}	50		200	KΩ	
Input pull-up resistor	R_I		10		KΩ	V_{IL}=0V
I/O pin capacitor (except XTAL1, XTAL2, RESET)	C_{IO}			15	pF	

Note : Needs external 10KΩ pull-up resistor

Table 51. DC Electrical Characteristics

DC supply voltage	-0.3V to +7.0V
Input / Output voltage	GND-0.2V to VCC +0.2V
Operating ambient temperature	-0°C to +70°C
Storage temperature	-55°C to +125°C
Operating voltage (VCC)	+4.0V to 5.25V

Table 52. Absolute Maximum Rating

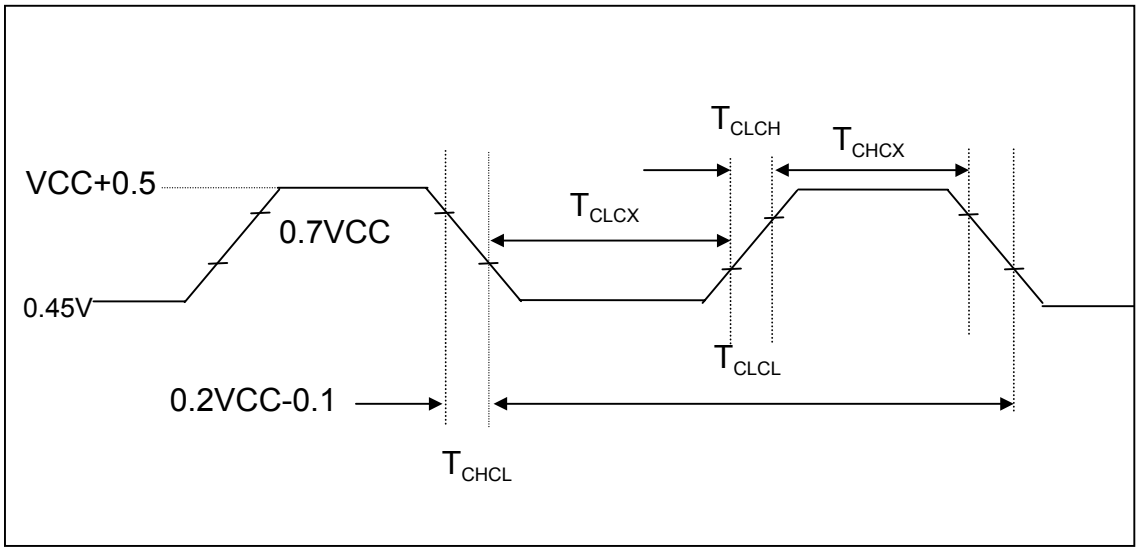


Figure 3. External Clock Drive Waveform

Symbol	Parameter	Min.	Max.	Units
$1/T_{CLCL}$	Oscillator frequency	5.94	6.06	MHz
T_{CHCX}	High time	0.35 T_{CLCL}	0.65 T_{CLCL}	nS
T_{CLCX}	Low time	0.35 T_{CLCL}	0.65 T_{CLCL}	nS
T_{CLCH}	Rise time		20	nS
T_{CHCL}	Fall time		20	nS
T_{POR}	Power on reset internal high time	30		μS

Note : 10 KΩ pull-up resistor, C=50pF

Table 53. AC Electrical Characteristics