WT50F6

8-bit μC with 8KB ISP Flash Memory, 8-CH 12-bit A/D Converter and 16x4 LCD Driver

Preliminary

DESCRIPTION

The WT50F6 is a high-performance, low-cost, CMOS 8-bit single-chip micro controller with 8Kbytes in-system-programmable flash memory, an 8-channel 12-bit rail-rail A/D converter and 16x4 LCD driver. This chip is suitable for variable applications, especially where analog signal (sensor output) to digital signal conversion, LCD display and short development cycle are required, including industrial control, consumer, communications, and security products.

This chip has 8-bit CPU, RAM, flash memory, I/Os, dual 16-bit timer/counters; interrupt controller, 16x4 LCD driver and an 8-channel 12-bit A/D converter. To be suitable for portable battery-powered applications, a power saving function is included.

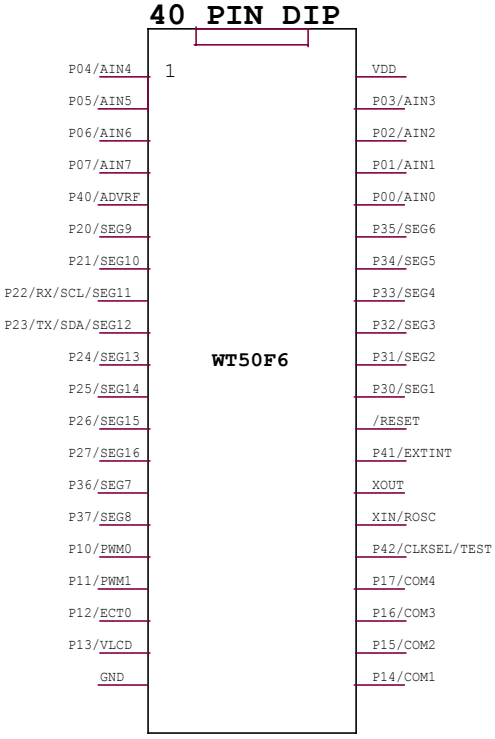
FEATURES

- 8-bit single chip micro controller with 8K bytes flash memory and 384bytes SRAM
- Wide voltage operating range from 2.7 V to 5.5 V
- On-chip RC oscillator runs at 8MHz and crystal oscillator can run up to 8.0 MHz
- 8 interrupt sources (external:2; internal:6) ; all sources have independent latches each and multiple interrupt control is available
- I/O port (32 pins)
  - Port P0 8 pins (shared with analog inputs)
  - Port P1 8 pins (P10~P13 25 *m*A source; P10~P17 25mA sink current)
  - Port P2 8 pins (shared with SEG9~SEG16)
  - Port P3 8 pins (shared with SEG1~SEG8)
  - Port P4 3 pins P42(output only) share with CLKSEL
    P41 share with EXTINT
    P40 share with ADvrf
- Interval Timer (Internal time base generator)
- Operating current 2*m*A/4MHz@5V; providing standby mode (OSC is stopped and current consumption < 1 *u*A@5V) and external pin wake-up mode
- Watchdog timer

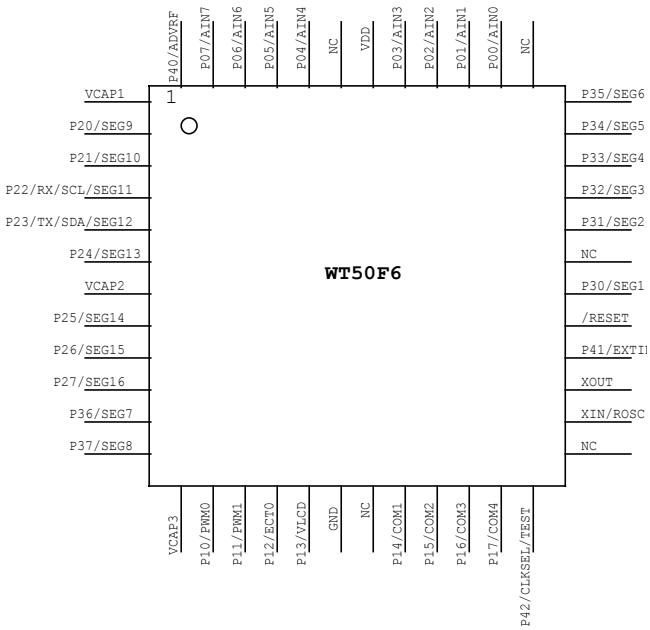
- Dual PWM
- Dual 16-bit timer/counters
- UART and serial I/O interface
- A/D converter module
  - 8 analog inputs multiplexed into one A/D converter
  - Sample and hold
  - 20 μS conversion time/per channel
  - 12-bit resolution rail to rail with ±2 LSB accuracy
  - Selectable reference voltage from external input AD_{VRF} or internal VDD
- LCD driver
  - LCD direct drive (max. 64dots LCD display at 1/4 duty)
  - Selectable LCD bias voltage from external input VLCD or internal VDD
  - 1/4, 1/3, 1/2 duties and 1/2, 1/3 biases can be selected by programming
- Programming for flash memory
  - Programming lock for software security; read/write protection (signature compare)
  - In-system-programming via two-wire serial control protocol
- Package: Die/48-pin LQFP/40-pin PDIP/28-pin PDIP/28-pin SOP(300mil)

PACKAGE PIN ASSIGNMENT

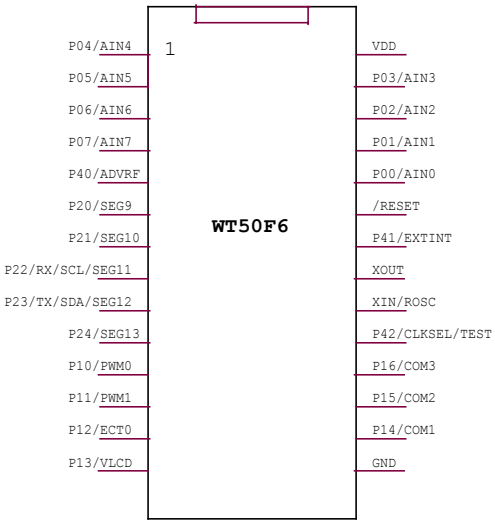
40 PIN DIP



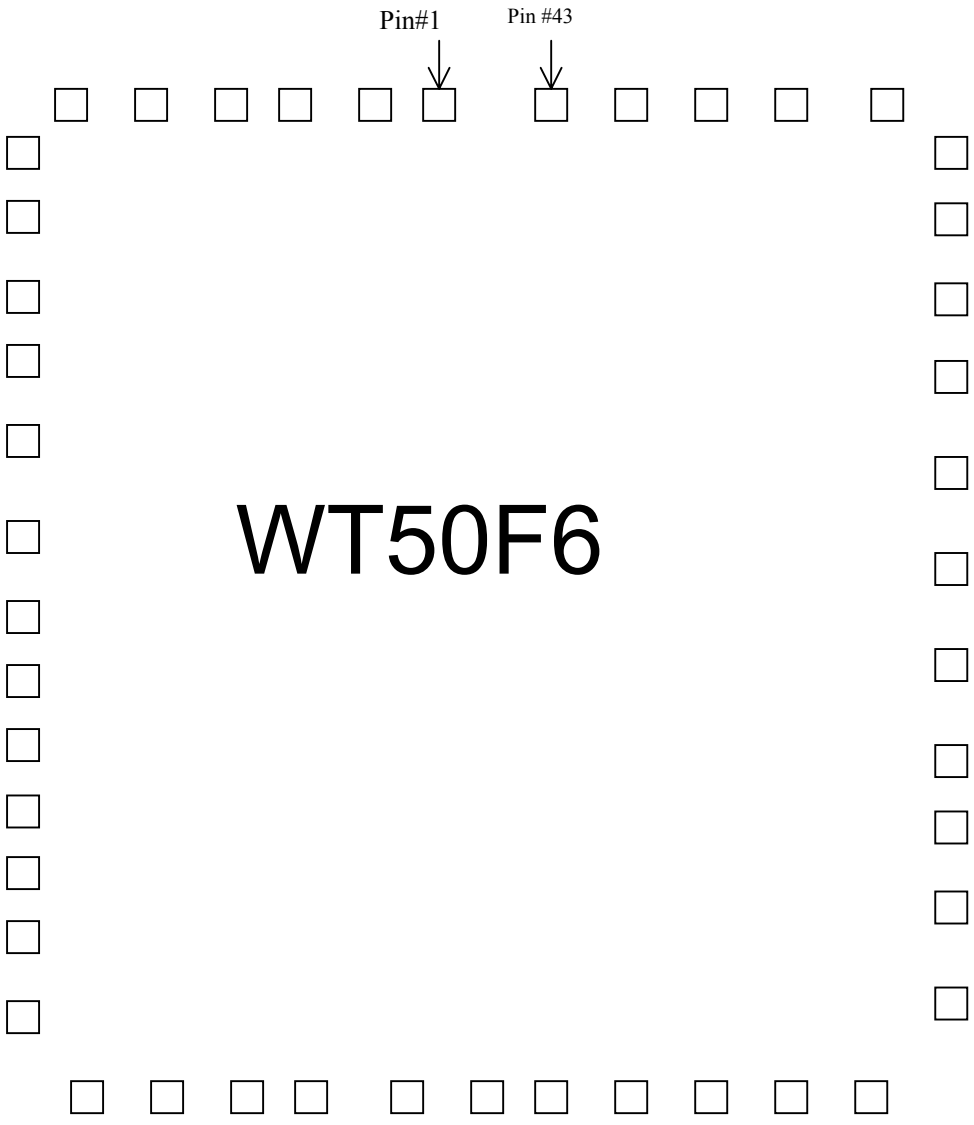
48 PIN LQFP



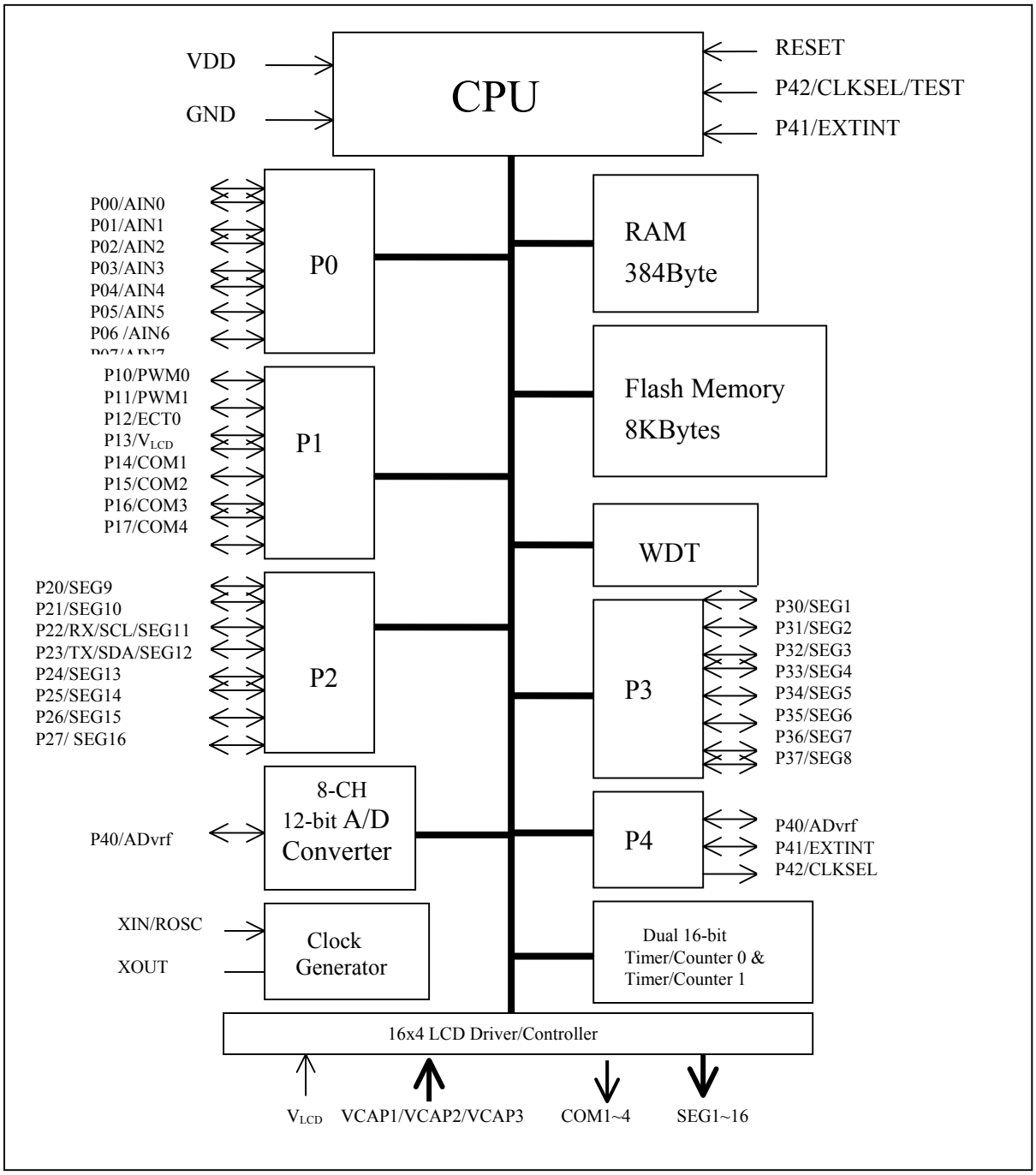
28 PIN DIP/SOP(300mil)



PAD LAYOUT (DIE FORM)



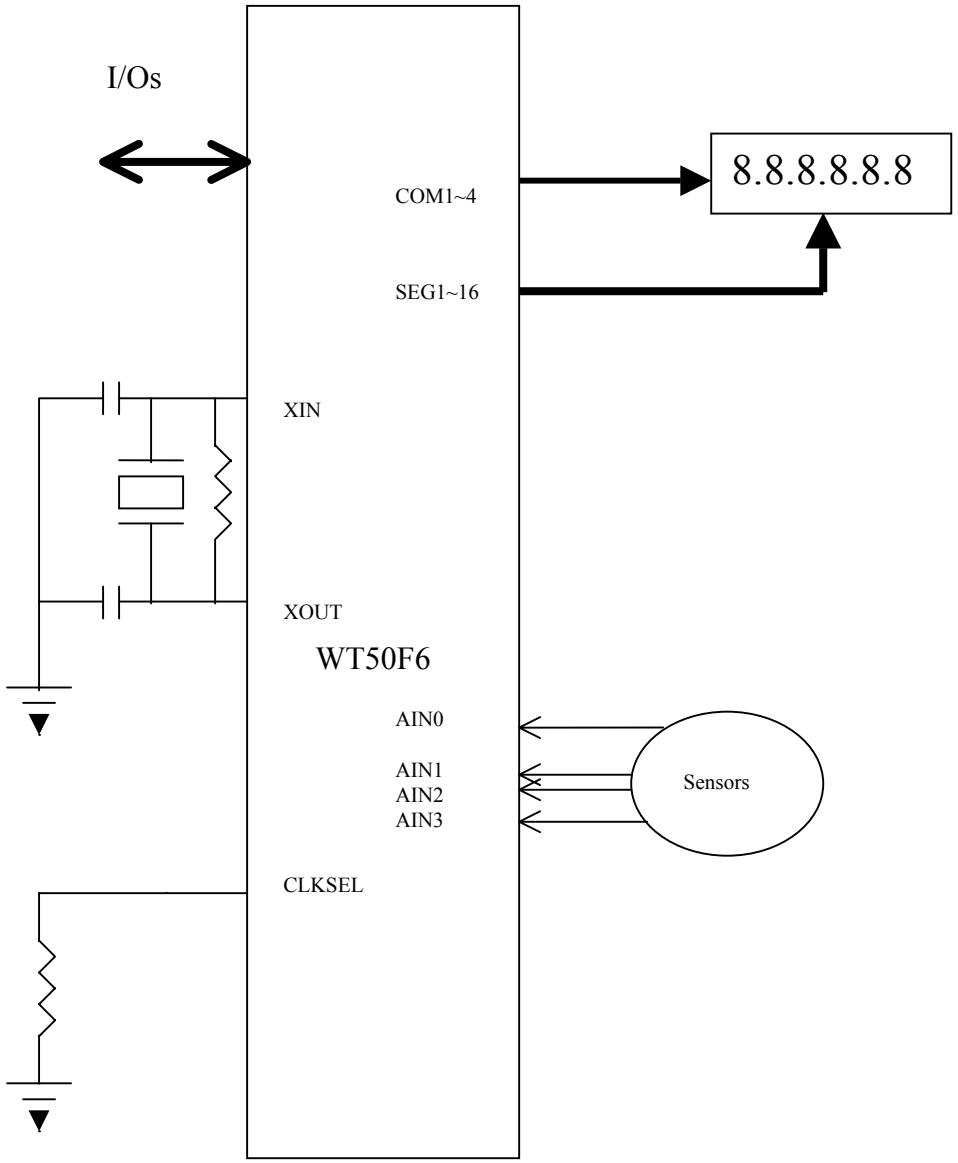
BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Die	40-pin	48-pin	28-pin	In/Out	FUNCTIONS
P00/AIN0~ P03/AIN3 P04/AIN4~P07/AIN7	39 ~ 42 1~4	36 ~ 39 1~4	38~41 44~47	24~27 1~4	I/O	8-bit I/O port; internal pull-up; ; i/p: external pull-low (Shared with analog inputs)
P10/PWM0 P11/PWM1 P12/ECT0 P13/V_{LCD} P14/COM1 P15/COM2 P16/COM3 P17/COM4	19 20 21 22 24 25 26 27	16 17 18 19 21 22 23 24	14 15 16 17 20 21 22 23	11 12 13 14 16 17 18 *	I/O	(Shared with PWM output); 8-bit I/O port; internal pull-up; o/p: 4-pin source 25mA; 8-pin sink 25mA i/p: external pull-low (External counter) (External bias voltage to LCD) (LCD common output) (LCD common output) (LCD common output) (LCD common output)
P20/SEG9 P21/SEG10 P22/Rx/SCL/SEG11 P23/Tx/SDA/SEG12 P24/SEG13 P25/SEG14 P26/SEG15 P27/SEG16	7 8 9 10 11 13 14 15	6 7 8 9 10 11 12 13	2 3 4 5 6 8 9 10	6 7 8 9 10 * * *	I/O	8-bit I/O port; internal pull-up; i/p: external pull-low (Shared with LCD segment output) P20~P23 support key wake-up & interrupt function P22 shared with serial interface Rx (asyc.)/SCL (sync.) P23 shared with serial interface Tx (asyc.)/SDA (sync.)
P30/SEG1 P31/SEG2 P32/SEG3 P33/SEG4 P34/SEG5 P35/SEG6 P36/SEG7 P37/SEG8	33 34 35 36 37 38 16 17	30 31 32 33 34 35 14 15	30 32 33 34 35 36 11 12	* * * * * * * *	I/O	8-bit I/O port; internal pull-up; i/p: external pull-low (Shared with LCD segment output)
XIN/ROSC	29	26	26	20	Input	Crystal input/ROSC input
XOUT	30	27	27	21	Output	Crystal output
/RESET	32	29	29	23	Input	System reset signal input; low active
VDD	43	40	42	28	Input	Power source
GND	23	20	18	15	Input	Ground
P40/AD_{VRF}	5	5	48	48	I/O	I/O pin or A/D Reference voltage input
P41/EXTINT	31	28	28	5	I/O	I/O pin or External interrupt input
P42/CLKSEL/TEST	28	25	24	19	Output	Normal state use as output only pin, in the initial state use for Clock sources select, connected to pull-up Resistor for ROSC or to pull-down resistor for Crystal (Test Pin)
VCAP1, VCAP2, VCAP3	6,12,18	*	1,7,13	*	Input	LCD capacitor for power saving use *40-pin don't support this function

APPLICATION DIAGRAM



WT50F6 REGISTOR MAPPING

NAME	ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
P0DR	$00	R/W	P0DR7	P0DR6	P0DR5	P0DR4	P0DR3	P0DR2	P0DR1	P0DR0
P1DR	$01	R/W	P1DR7	P1DR6	P1DR5	P1DR4	P1DR3	P1DR2	P1DR1	P1DR0
P2DR	$02	R/W	P2DR7	P2DR6	P2DR5	P2DR4	P2DR3	P2DR2	P2DR1	P2DR0
P3DR	$03	R/W	P3DR7	P3DR6	P3DR5	P3DR4	P3DR3	P3DR2	P3DR1	P3DR0
P4DR	$04	R/W	-	-	-	-	-	P4DR2	P4DR1	P4DR0
CRYC	$05	R/W	FQHENA	FQLENA	-	SLPRST	WUT1	WUT0	CRYST/PSM	ENAB
INTC0	$06	R/W	P2SIOINT	ADCI	FQHINT	EXTINT	P2SIONMI	T/C1INT	T/C0INT	FQLINT
TMC	$07	W	TC1EN	T1TCS2	T1TCS1	T1TCS0	TC0EN	T0TCS2	T0TCS1	T0TCS0
Reserved	$08	R/W	-	-	-	-	-	-	-	-
SLPST	$09	W	-	-	-	-	-	-	-	-
LDTC0	$0A	W	-	-	-	-	-	-	-	-
TC0H	$0B	R/W	B7	B6	B5	B4	B3	B2	B1	B0
TC0L	$0C	R/W	B7	B6	B5	B4	B3	B2	B1	B0
LDTC1	$0D	W	-	-	-	-	-	-	-	-
TC1H	$0E	R/W	B7	B6	B5	B4	B3	B2	B1	B0
TC1L	$0F	R/W	B7	B6	B5	B4	B3	B2	B1	B0
TCCR10	$10	R/W	-	-	-	INTEG1	INTEG0	PWMS2	PWMS1	PWMS0
PORTSEL	$11	R/W	-	P3SCHN	P3SCLN	P2SCHN	P2SCLN	P1LCD	P1PWM1	P1PWM0
WDTMR	$12	W	FQHS2	FQHS1	FQHS0	-	WDTEN	WDTS2	WDTS1	WDTS0
ADCR	$13	R/W	ADON	CKS1	CKS0	CKS2	B3	B2/ADS2	B1/ADS1	B0/ADS0
ADR	$14	R	B7	B6	B5	B4	B3	B2	B1	B0
P2SEL	$14	W	P27S16S	P26S15S	P25S14S	P24S13S	P23S12S	P22S11S	P21S10S	P20S9S
LCDC	$15	W	-	-	LFS2	LCDPS	LFS1	LFS0	DTY1	DTY0
DDA11	$16	W	B7	B6	B5	B4	B3	B2	B1	B0
DDA12	$17	W	B7	B6	B5	B4	B3	B2	B1	B0
SBUF	$18	R/W	B7	B6	B5	B4	B3	B2	B1	B0
SCON	$19	W	URSIO	UR89	URTB8	URREN/STXNAK	MSTR	MSTOP	SIORW	SLAVE
SSTA	$19	R	UNWORK	-	URRB8	SRXNAK	SFIRST	SSTOP	SSRW	SIORDY
DDA21	$1A	W	B7	B6	B5	B4	B3	B2	B1	B0
DDA22	$1B	W	B7	B6	B5	B4	B3	B2	B1	B0
TSIOSEL	$1C	W	-	SIOSEL	TC1CLK	TC0SEL	TC0HEN	T0HTCS2	T0HTCS1	T0HTCS0
TSIO	$1D	W	B7	B6	B5	B4	B3	B2	B1	B0
DDA31	$1E	W	B7	B6	B5	B4	B3	B2	B1	B0
DDA32	$1F	W	B7	B6	B5	B4	B3	B2	B1	B0
SIO_ADR	$20	W	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	-
Reserved	$21	W	-	-	-	-	-	-	-	-
DDA41	$22	W	B7	B6	B5	B4	B3	B2	B1	B0
DDA42	$23	W	B7	B6	B5	B4	B3	B2	B1	B0
INTC1	$24	R/W	-	-	-	SIOINT	P23INT	P22INT	P21INT	P20INT
P4DCR	$25	R/W	-	-	-	-	-	-	P4DCR1	P4DCR0
P0DCR	$26	R/W	P0DCR7	P0DCR6	P0DCR5	P0DCR4	P0DCR3	P0DCR2	P0DCR1	P0DCR0
P1DCR	$27	R/W	P1DCR7	P1DCR6	P1DCR5	P1DCR4	P1DCR3	P1DCR2	P1DCR1	P1DCR0
P2DCR	$28	R/W	P2DCR7	P2DCR6	P2DCR5	P2DCR4	P2DCR3	P2DCR2	P2DCR1	P2DCR0
P3DCR	$29	R/W	P3DCR7	P3DCR6	P3DCR5	P3DCR4	P3DCR3	P3DCR2	P3DCR1	P3DCR0
OCR10H	$2A	R/W	B7	B6	B5	B4	B3	B2	B1	B0
OCR10L	$2B	R/W	B7	B6	B5	B4	B3	B2	B1	B0
OCR11H	$2C	R/W	B7	B6	B5	B4	B3	B2	B1	B0
OCR11L	$2D	R/W	B7	B6	B5	B4	B3	B2	B1	B0
ISPEN	$30	W	-	-	-	-	-	-	-	ISP
ISPHADD	$31	W	XADR7 A12	XADR6 A11	XADR5 A10	XADR4 A9	XADR3 A8	XADR2 A7	XADR1 A6	XADR0 A5
ISPLADD	$32	W	-	-	-	YADR4 A4	YADR3 A3	YADR2 A2	YADR1 A1	YADR0 A0

ISPCTL	$33	W	XE	YE	SE	OE	ERASE	MAS1	PROG	NVSTR
ISPDATA	$34	R/W	IDAT7	IDAT6	IDAT5	IDAT4	IDAT3	IDAT2	IDAT1	IDAT0

FUNCTION DESCRIPTION

【1】 I/O PORTS

The WT50F5 has 4 ports (32 pins) each as follows:

- P00 ~ P07 ; 8-bit I/O port (shared with analog input AIN0~AIN7)
- P10 ~ P17 ; 8-bit I/O port (shared with PWM0/PWM1, COM1~4, ECT0,V_{LCD})
- P20 ~ P27 ; 8-bit I/O port (shared with SEG9~16)
- P30 ~ P37 ; 8-bit I/O port (shared with SEG1~8)
- P40 ~ P42 ; 3-bit I/O port (shared with Advrf, EXTINT & CLKSEL,)

Port P0 (P00 ~P07)

Port P0 Data Register (P0DR; $00); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P0DR7	P0DR6	P0DR5	P0DR4	P0DR3	P0DR2	P0DR1	P0DR0

Port P0 Data Direction Control Register (P0DCR; $26); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P0DCR7	P0DCR6	P0DCR5	P0DCR4	P0DCR3	P0DCR2	P0DCR1	P0DCR0

Table 1. Port P0 Configuration

P0DCR0~7	P0DR0~7	I/O	Pull-up	Results
0	0	In	No	Tri-state (Hi-Z)
0	1	In	Yes	P00~P07 with Pull-up resistor (MOS)(NOTE)
1	0	Output	No	Output “0”
1	1	Output	No	Output “1”

Port P1 (P10 ~ P13 25mA current source; P10~P17 25mA current sink)

Port P1 Data Register (P1DR; $01); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P1DR7	P1DR6	P1DR5	P1DR4	P1DR3	P1DR2	P1DR1	P1DR0

Port P1 Data Direction Control Register (P1DCR; $27); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P1DCR7	P1DCR6	P1DCR5	P1DCR4	P1DCR3	P1DCR2	P1DCR1	P1DCR0

Table 2: Port P1 Configuration

P1DCR0~7	P1DR0~7	I/O	Pull-up	Results
0	0	In	No	Tri-state (Hi-Z)
0	1	In	Yes	P10~17 with Pull-up resistor (MOS)(NOTE)
1	0	Output	No	Output “0”
1	1	Output	No	Output “1”

Port P2 (P20 ~ P27)

Port P2 Data Register (P2DR; $02); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P2DR7	P2DR6	P2DR5	P2DR4	P2DR3	P2DR2	P2DR1	P2DR0

Port P2 Data Direction Control Register (P2DCR; $28); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P2DCR7	P2DCR6	P2DCR5	P2DCR4	P2DCR3	P2DCR2	P2DCR1	P2DCR0

Table 3: The Configuration of port P2

P2DCR0~7	P2DR0~7	I/O	Pull-up	Results
0	0	In	No	Tri-state (Hi-Z)
0	1	In	Yes	P20~27 with Pull-up resistor (MOS)(NOTE)
1	0	Output	No	Output “0”
1	1	Output	No	Output “1”

Port P3 (P30~P37)

Port P3 Data Register (P3DR; $03); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P3DR7	P3DR6	P3DR5	P3DR4	P3DR3	P3DR2	P3DR1	P3DR0

Port P3 Data Direction Control Register (P3DCR; $29); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0

P3DCR7	P3DCR6	P3DCR5	P3DCR4	P3DCR3	P3DCR2	P3DCR1	P3DCR0

Table 4: The Configuration of Port P3

P3DCR0~7	P3DR0~7	I/O	Pull-up	Results
0	0	In	No	Tri-state (Hi-Z)
0	1	In	Yes	P30~P37 with Pull-up resistor (MOS)
1	0	Output	No	Output “0”
1	1	Output	No	Output “1”

Port P4 (P40~P42)

Port P4 Data Register (P4DR; $04); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
-	-	-	-	-	P4DR2	P4DR1	P4DR0

Port P4 Data Direction Control Register(P4DCR; $25); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
-	-	-	-	-	-	P4DCR1	P4DCR0

Table 5: The Configuration of Port P4

P4DCR0	P4DR0	I/O	Pull-up	Results
0	0	In	No	Advrf pin or P41 Input Tri-state function
0	1	In	Yes	P40 Input with pull-up resistor
1	0	Output	No	P40 Output “0”
1	1	Output	No	P40 Output “1”

P4DCR1	P4DR1	I/O	Pull-up	Results
0	0	In	No	EXTINT pin or P41 Input Tri-state function
0	1	In	Yes	P41 Input with pull-up resistor
1	0	Output	No	P41 Output “0”
1	1	Output	No	P41 Output “1”

P4DR2	I/O	Pull-up	Results
0	Output	No	P42 Output “0”
1	Output	No	P42 Output “1”

PORTSEL ($11); R/W; Initial 00_H

B7	B6	B5	B4	B3	B2	B1	B0

VLCDSEL	P3SCHN	P3SCLN	P2SCHN	P2SCLN	P1LCD	P1PWM1	P1PWM0

B7: VLCDSEL; "1": external LCD voltage via Vlcd pin
"0": Internal LCD voltage via Vdd
B6: P3SCHN; P3 segments or I/Os select (high nibble); 0: I/Os, 1:segments
B5: P3SCLN; P3 segments or I/Os select (low nibble); 0: I/Os, 1:segments
B4: P2SCHN; P2 segments or I/Os select (high nibble); 0: I/Os, 1:segments
B3: P2SCLN; P2 segments or I/Os select (low nibble); 0: I/Os, 1:segments
B2: P1LCD; LCD VLCD or I/Os select; 0: P13 I/O function
1: VLCD pin function
B1: P1PWM1; PWM1 or I/O select; 0: I/O, 1:PWM1 output
B0: P1PWM0; PWM0 or I/O select; 0: I/O, 1:PWM0 output

P2SEL ($14); W; Initial 00_H

B7	B6	B5	B4	B3	B2	B1	B0
P27S16S	**P26S15S**	**P25S14S**	**P24S13S**	**P23S12S**	**P22S11S**	**P21S10S**	**P20S9S**

B7: P27S16S; "0": Base on P2SCHN ; "1":P27 I/O Function
B6: P26S15S; "0": Base on P2SCHN ; "1":P26 I/O Function
B5: P25S14S; "0": Base on P2SCHN ; "1":P25 I/O Function
B4: P24S13S; "0": Base on P2SCHN ; "1":P24 I/O Function
B3: P23S12S; "0": Base on P2SCLN ; "1":P23 I/O Function
B2: P22S11S; "0": Base on P2SCLN ; "1":P22 I/O Function
B1: P21S10S; "0": Base on P2SCLN ; "1":P21 I/O Function
B0: P20S9S; "0": Base on P2SCLN ; "1":P20 I/O Function

EXTINT Input Pin

TCCR10 ($10); R/W; Initial 00_H

B7	B6	B5	B4	B3	B2	B1	B0
-	-	-	**INTEG1**	**INTEG0**	**PWMS2**	**PWMS1**	**PWMS0**

Table6: The Configuration of INTEG1 & INTEG0

INTEG1	INTEG0	Results
0	0	EXTINT pin rising edge interrupt with pull-down resistor
0	1	EXTINT pin falling edge interrupt with pull-up resistor
1	0	EXTINT pin both edge interrupt with Hi-Z

1	1	Don't care

【2】 NMI SOURCE

- Interrupt from P20~P23 & SIO

【3】 INT Source

- INT0 from T/C0
- INT1 from T/C1
- FQL INT
- FQH INT
- A/D conversion completion interrupt
- EXTINT (rising/falling/both edge selectable)
- P2SIOINT (Port 20~Port 23 status change or SIO interrupt)

INTC0 Register ($06); Interrupt control command register; R/W

Read: read interrupt flag

B7	B6	B5	B4	B3	B2	B1	B0
P2SIOINT	**ADCI**	**FQHINT**	**EXTINT**	**P2SIONMI**	**T/C1INT**	**T/C0INT**	**FQLINT**

Write: Interrupt enable/disable control

B7	B6	B5	B4	B3	B2	B1	B0	FUNCTION
*	*	*	*	*	*	*	**1**	Low frequency interrupt enable
*	*	*	*	*	*	*	**0**	Low frequency interrupt disable & clear
*	*	*	*	*	*	**1**	*	T/C0 INT0 interrupt enable
*	*	*	*	*	*	**0**	*	T/C0 INT0 interrupt disable & clear
*	*	*	*	*	**1**	*	*	T/C1 INT1 interrupt enable
*	*	*	*	*	**0**	*	*	T/C1 INT1 interrupt disable & clear
*	*	*	*	**1**	*	*	*	P2 & SIO NMI interrupt enable
*	*	*	*	**0**	*	*	*	P2 & SIO NMI interrupt disable & clear
*	*	*	**1**	*	*	*	*	External interrupt (EXTINT) enable
*	*	*	**0**	*	*	*	*	External interrupt (EXTINT) disable & clear
*	*	**1**	*	*	*	*	*	High frequency interrupt enable
*	*	**0**	*	*	*	*	*	High frequency interrupt disable & clear

*	**1**	*	*	*	*	*	*	A/D converter interrupt enable (hold & conversion start)
*	**0**	*	*	*	*	*	*	A/D converter interrupt disable & clear (sampling start)
1	*	*	*	*	*	*	*	P20~P23 status change & SIO interrupt enable
0	*	*	*	*	*	*	*	P20~P23 status change & SIO interrupt disable & clear

INTC1 Register ($24); Interrupt control command register; R/W

Read: read interrupt flag

B7	B6	B5	B4	B3	B2	B1	B0
-	**-**	**-**	**SIOINT**	**P23INT**	**P22INT**	**P21INT**	**P20INT**

Write: Interrupt enable/disable control

B7	B6	B5	B4	B3	B2	B1	B0	FUNCTION
*	*	*	*	*	*	*	**1**	P20 interrupt enable
*	*	*	*	*	*	*	**0**	P20 interrupt disable & clear
*	*	*	*	*	*	**1**	*	P21 interrupt enable
*	*	*	*	*	*	**0**	*	P21 interrupt disable & clear
*	*	*	*	*	**1**	*	*	P22 interrupt enable
*	*	*	*	*	**0**	*	*	P22 interrupt disable & clear
*	*	*	*	**1**	*	*	*	P23 interrupt enable
*	*	*	*	**0**	*	*	*	P23 interrupt disable & clear
*	*	*	**1**	*	*	*	*	I^2C or UART interrupt enable
*	*	*	**0**	*	*	*	*	I^2C or UART disable & clear

【4】 CLOCK SOURCE

CPU clock from RC oscillator: CLKSEL pin is connected to VDD via resistor

CPU clock from Crystal oscillator: CLKSEL pin is connected to GND via resistor

CRYC register ($05); Oscillator control

B3~B0:R/W

B7	B6	B5	B4	B3	B2	B1	B0

FQHENA	FQLENA	-	SLPRST	WUT1	WUT0	CRYST/PSM	ENAB

B0: ENAB; 0: enable (default), 1: disable

Note: b0 is set to 1 in normal operation, and can be set to 0 to stop the crystal (sleep mode)

B1: CRYST/PSM; 0: crystal starts (default), 1: power saving mode

Note: While crystal is being started (strong current mode), b1 is set to 0; once it starts, b1 can be set to 1 in order to switch the crystal from "strong current mode" to "Weak current mode" for power saving

B3:B2: WUT1: WUT0 (set the warm-up time at release of the hold operating mode)

00: 2^{18}/fc .....65.5 ms (when fc=4MHz) ➔ 4.1ms(new version)

01: 2^{14}/fc .....4.1 ms (when fc=4MHz) ➔ 65.5ms(new version)

10: 2^{10}/fc .....256 us (when fc=4MHz)

11: 2^{6}/fc .....16 μs (when fc=4MHz)

B4: SLPRST; 0: go through reset process,

1: without going through reset process

B6: FQLENA; 0: disable FQL (default), 1: enable FQL

B7: FQHENA; 0: disable FQH (default), 1: enable FQH

【5】 TIMER/COUNTER/PWM

WT50F5 has two 16-bit timer/counters, namely T/C0 and T/C1, one low-frequency timer, and one high-frequency timer. Both T/C0 and T/C1 can be used as either a timer or a counter, and also have auto-reload capability.

IN COUNTER MODE

Registers for loading T/C0&1 16 bit data

LDT/C0 ($0A); Write	**Load (&latch) T/C0 16-bit data**
LDT/C1 ($0D); Write	**Load (&latch) T/C1 16-bit data**

T/C0&1 16-bit data locations

	High Byte Data (D_{15} ~ D_8)	Low Byte Data (D_7 ~ D_0)
T/C0	**T/C0H ($0B) ; b7 ~ b0**	**T/C0L ($0C) ; b7 ~ b0**
T/C1	**T/C1H ($0E) ; b7 ~ b0**	**T/C1L ($0F) ; b7 ~ b0**

TMC Register ($07); Timer control register, Write

B7	B6	B5	B4	B3	B2	B1	B0
TC1EN	**T1TCS2**	**T1TCS1**	**T1TCS0**	**TC0EN**	**T0TCS2**	**T0TCS1**	**T0TCS0**

B3: T/C0 enable/disable control (can be stop on-the-fly)

"0": disable; "1": enable

B7: T/C1 enable/disable control (can be stop on-the-fly)

"0": disable; "1": enable

B2 ~ B0: T/C0 timer sources and timer/counter mode selection

T/C0 Clock Source Table

T0TCS2	T0TCS1	T0TCS0	Mode	Selected Source
0	**0**	**0**	**Timer**	**CPU Clock (T)**
0	**0**	**1**	**Timer**	**T/4**
0	**1**	**0**	**Timer**	**T/8**
0	**1**	**1**	**Timer**	**T/16**
1	**0**	**0**	**Timer**	**T/32**
1	**0**	**1**	**Timer**	**T/64**
1	**1**	**0**	**Timer**	**T/128**
1	**1**	**1**	**Timer**	**External counter (ETC0)**

B6 ~ B4: T/C1 timer sources and timer/counter mode selection

T/C1 Clock Source Table

T1TCS2	T1TCS1	T1TCS0	Mode	Selected Source
0	**0**	**0**	**Timer**	**CPU Clock (T)**
0	**0**	**1**	**Timer**	**T/4**
0	**1**	**0**	**Timer**	**T/8**
0	**1**	**1**	**Timer**	**T/16**
1	**0**	**0**	**Timer**	**T/32**
1	**0**	**1**	**Timer**	**T/64**
1	**1**	**0**	**Timer**	**T/128**
1	**1**	**1**	**Timer**	**Clock source from T/C0 output**

IN TIMER MODE

In regular timer mode, T/C0 and T/C1 can be re-loaded and always counts down from the value set by the user. If the specified bit is enabled in INTC register ($06) and the timer counts down from the value set by the user toward 0000_H, then once it hits 0000_H and becomes underflow, an interrupt signal will be generated. The value set by the user will be re-loaded to the timer automatically, and, again, the timer counts down from the value set by the user toward 0000_H.

T/C1 IN PWM MODE

When the PWM mode is selected, T/C1 incorporated with the output compare registers OCR10 and OCR11 performs a dual 6,7,8, 9 or 10-bit, free-running, glitch-free and phase correct PWM with outputs on the P10/PWM0 and P11/PWM1 pins. The PWM output frequency is depends on the resolutions, i.e. 6,7,8, 9, or 10-bit, and the OSC frequency, $F_{OSC.}$ Referring to Table 5 for more detail.

In this mode T/C1 acts as a down counter, counting down from MAX to 0000H. When the counter value matches the contents of the 10 least significant bits (for 10-bit PWM case) of OCR10 or OCR11, the P10 (PWM0)/P11 (PWM1) pins are set to “high”.

Write procedure for PWM operation should be OCR10L ($2B) first, followed by OCR10H ($2A), and then finally TCCR10 ($10).

TCCR10 ($10); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
-	-	-	**INTEG1**	**INTEG0**	**PWMS2**	**PWMS1**	**PWMS0**

PWMS2	PWMS1	PWMS0	Description
0	0	0	PWM function is disable (default)
0	0	1	T/C1 is an 8-bit PWM
0	1	0	T/C1 is a 9-bit PWM
0	1	1	T/C1 is a 10-bit PWM
1	0	1	T/C1 is an 6-bit PWM
1	1	0	T/C1 is an 7-bit PWM

Table 5: The relationship between the PWM output frequency and its resolution

PWM Resolution	Timer MAX value	Frequency
6-bit	$003F	$F_{OSC}/64$
7-bit	$007F	$F_{OSC}/128$
8-bit	$00FF	$F_{OSC}/256$
9-bit	$01FF	Fosc/512
10-bit	$03FF	Fosc/1024

OCR10H ($2A)/OCR10L ($2B); T/C1 output compare register; R/W; Initial value 00_H

OCR10H	B7(MSB)	B6	B5	B4	B3	B2	B1	B0
OCR10L	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)

OCR11H ($2C)/OCR11L ($2D); T/C1 output compare register; R/W; Initial value 00_H

OCR11H	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
OCR11L	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)

To avoid the false counting of the PWM pulse in the event of abnormal OCR10/OCR11 write (glitch case), the OCR10/OCR11contents while being written, are copied to a temporary location and are latched when T/C1 reaches the value MAX.

Note: **The value in OCR10/OCR11 can't be 0000_H or MAX; the minimal value is 0001_H and the maximal value is MAX-1.**

WDTMR register ($12)
Watchdog timer must reset within T_{WDT} seconds; otherwise the system will be reset.

B7	B6	B5	B4	B3	B2	B1	B0
FQHS2	**FQHS1**	**FQHS0**	**-**	**WDTEN**	**WDTS2**	**WDTS1**	**WDTS0**

B2:B0: Watchdog timer or FQL output frequencies select (f_{WDT})

WDTS2	WDTS1	WDTS0	Output Frequency (f_{WDT}) @OSC=4MHz
0	**0**	**0**	**OSC1/2^{17} (0.25Hz)**
0	**0**	**1**	**OSC1/2^{16} (0.5Hz)**
0	**1**	**0**	**OSC1/2^{15} (1.0Hz)**
0	**1**	**1**	**OSC1/2^{14} (2.0Hz)**
1	**0**	**0**	**OSC1/2^{13} (4.0Hz)**
1	**0**	**1**	**OSC1/2^{12} (8.0Hz)**
1	**1**	**0**	**OSC1/2^{11} (16.0Hz)**
1	**1**	**1**	**OSC1/2^{10} (32.0Hz)**

Where OSC1=OSC/2^7, so when OSC=4MHz then OSC1=32KHz

B3: WDTEN: Watchdog timer/FQL select; 1: watchdog function,
0: FQL function

B7:B5: FQS2~FQH0; FQH output frequencies select

FQHS2	FQHS1	FQHS0	Output Frequency (@OSC=4MHz)
0	0	0	OSC1 (32kHz)
0	0	1	OSC1/2 (16kHz)
0	1	0	OSC1/2^2 (8kHz)
0	1	1	OSC1/2^3 (4kHz)
1	0	0	OSC1/2^4 (2kHz)
1	0	1	OSC1/2^5 (1kHz)
1	1	0	OSC1/2^6 (512Hz)
1	1	1	OSC1/2^7 (256Hz)

【6】SERIAL BUS INTERFACE

WT50F6 has an 8-bit serial bus interface. It support two kinds of serial bus, one is 2-wire I^2C interface, and the other is UART. Register "SBUF ($18)" is the 8-bit receive & transmit data buffer.

Register "SCON ($19)" is the mainly control register and register "SSTA ($19)"status register of this interface.

The synchronous clock or baud rate source came from TC0 and can be selected via register "TSIOSEL".

At UART transmitted mode, stores the data to "SBUF" 8-bit data start to transmit. After transmitted 8-bit data the interrupt condition will happen.

SCON ($19); b7-b0, Write, initial value 00H

b7	b6	b5	b4	b3	b2	b1	b0
URSIO	**UR89**	**URTB8**	**URREN/ STXNAK**	**MSTR**	**MSTOP**	**SIORW**	**SLAVE**

B7: URSIO "0" UART Mode
"1" I^2C Mode, SCL pin clock generate by TC0 or TC0H

B6: UR89 "0" UART mode, 8-bit UART Tx, Rx baud rate generate by TC0 or TC0H
"1" UART mode, 9-bit UART Tx, Rx baud rate generate by TC0 or TC0H

B5: URTB8 "0" In UART mode the 9th bit of transmit data is "0"
"1" In UART mode the 9th bit of transmit data is "1"

B4: URREN "0" UART mode, Data Receive Disable
"1" UART mode, Data Receive Enable

STXNAK "0" In I^2C mode output NACK
"1" In I^2C mode output ACK (pull low the SDA pin on acknowledge bit

B3: MSTR "0" I^2C mode, disable START condition output in master mode
"1" I^2C mode, enable START condition output in master mode

B2: MSTOP "0" I^2C mode, disable STOP condition output in master mode
"1" I^2C mode, enable STOP condition output in master mode

B1: SIORW "0" Transmitter in master mode; Receiver in slave mode
"1" Receiver in master mode; Transmitter in slave mode
("0" I^2C write mode, "1" I^2C read mode)

B0: SLAVE "0" Slave mode
"1" Master mode

SSTA ($19); b7-b0, Read, initial value 00H

b7	b6	b5	b4	b3	b2	b1	b0
UNWORK	**-**	**URRB8**	**SRXNAK**	**SFIRST**	**SSTOP**	**SSRW**	**SIORDY**

B7: UNWORK "0" WT50F6 allow I^2C bus work
"1" WT50F6 is busy, I^2C bus unwork

B5: URRB8 "0" In UART mode the 9th bit of receive data is "0"
"1" In UART mode the 9th bit of receive data is "1"

B4: SRXNAK "0" I^2C mode ACK is received
"1" I^2C mode NACK is received

B3: SFIRST "0" I^2C slave mode, did not receive START condition
"1" I^2C slave mode, received START condition, sub-address match & first byte received

B2: SSTOP "0" I^2C slave mode, did not receive STOP condition
"1" I^2C slave mode, received STOP condition

B1: SSRW "0" I^2C slave mode, receive "Write" command
"1" I^2C slave mode, receiver "Read" command

B0: SIORDY "0" I^2C mode, did not detect an input/output data byte or STOP condition
"1" I^2C mode, detected an input/output data byte or STOP condition

SIO_ADR ($20); b7-b0, Write, initial value xxH

b7	b6	b5	b4	b3	b2	b1	b0
SAR7	**SAR6**	**SAR5**	**SAR4**	**SAR3**	**SAR2**	**SAR1**	**--**

SAR7~SAR1 7-bit address to be compared in I^2C slave mode

TSIOSEL ($1C); b7-b0, Write, initial value 00H

b7	b6	b5	b4	b3	b2	b1	b0
-	**SIOSEL**	**TC1CLK**	**TC0SEL**	**TC0HEN**	**T0HTCS2**	**T0HTCS1**	**T0HTCS0**

T0HTCS2	T0HTCS 1	T0HTCS 0	TC0H serial bus clock divider source
0	**0**	**0**	**CPU Clock (T)**
0	**0**	**1**	**T/2**

0	**1**	**0**	**T/4**
0	**1**	**1**	**T/8**
1	**0**	**0**	**T/16**
1	**0**	**1**	**T/32**
1	**1**	**0**	**T/64**
1	**1**	**1**	**T/128**

B3: TC0HEN "0" Disable TC0H 8-bit timer/counter
"1" Enable TC0H 8-bit timer/counter

B4: TC0SEL "0" TC0 is a 16-bit timer/counter
"1" TC0 change to two 8-bit timer/counter TC0H & TC0L
TC0H is dedicated to use by I^2C clock or UART baud rate

B5: TC1CLK "0" Disable TC1 clock output to P11
"1" Enable TC1 clock output pin P11 & disable PWM1 function

B6: SIOSEL "0" Disable I^2C function (P22 & P23 I/O function)
"1" Enable I^2C function

TC0H & TC0L ($0B & $0C); b7-b0, Write, initial value 00H

If TC0SEL is "0" TC0 is a 16-bit auto-reload timer it can be either use as normal timer/counter or I^2C, UART & Timer output time base.

If TC0SEL is "1" TC0 is compose by two 8-bit timer TC0H & TC0L. TC0H is dedicated to use by I^2C, UART or timer output pin.

TC0H can be re-loaded and always counts down from the value set by the user.

Master/Slave I²C interface

The master/slave I²C interface is provided for communicating with other I²C devices such as EEPROM and SMB interface IC.

Master Mode

To choose master mode, clear the SLAVE bit. The clock frequency can be programmed to various frequencies by setting TSIOSEL and TC0H registers.

Send out START and the first byte (START, 7-bit address and R/W bit)

First, clear SIORW bit to select transmitter mode and write first byte (7-bit address and R/W bit) to SBUF register. Then set MSTR bit, master will generate a START condition and send out the first byte with the clock speed specified in TSIOSEL and TC0H registers. After the whole data byte is transmitted and the 9th bit is received, the SIORDY bit is set and generates an interrupt if it is enabled. The 9th bit will be stored in SRXNAK bit for checking the slave acknowledge or not. The SCL pin will keep low to wait next byte operation.

Send out the following bytes

If it is a write command, write a data byte to SBUF register, then write any value to SIO_ADR register to clear SIORDY bit. It will send out the data byte and store the acknowledge bit from slave in SRXNAK bit. Again, the SIORDY bit is set after the acknowledge bit is received.

If it is a read command, set SIORW bit to be receiver mode and write STXNAK bit to determine what will be sent on acknowledge bit, then write SIO_ADR register to clear SIORDY bit and it will send out the clock for receiving next byte. After the acknowledge bit is transmitted, the SIORDY bit will be set. If master wants to stop the read operation, send NACK on acknowledge bit to inform slave device.

Send out STOP

Set MSTOP bit will generate STOP condition.

Slave Mode

At the slave mode, firstly set the SLAVE bit and set the SIORW bit to be receiver

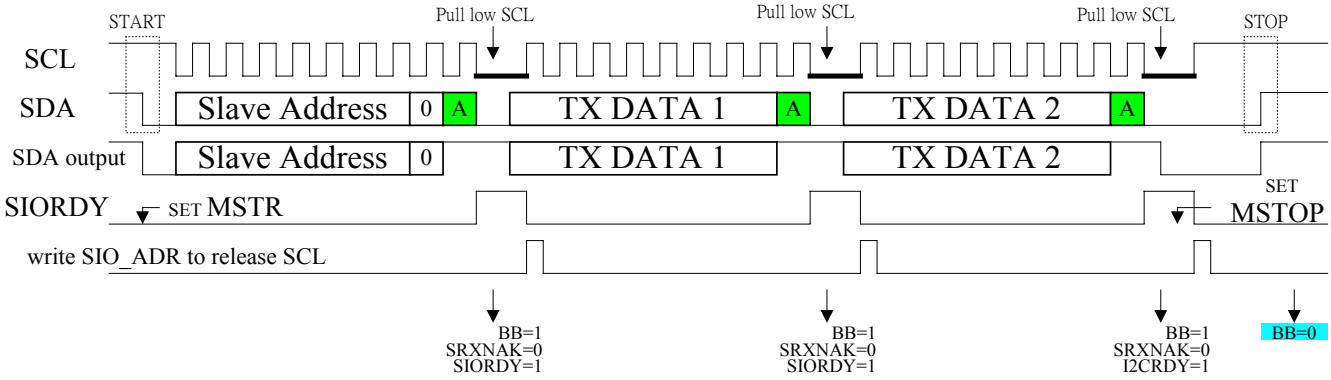
mode. When CPU is ready to receive, clear STXNAK bit. It will response ACK when a START condition followed by an address (which is equal to SIO_ADR register) are received. An interrupt can be generated if it is enabled and the R/W bit is stored in SIORW bit for checking read/write operation. After the ACK bit, SCL pin outputs low level to stop the clock for handshaking.

If a write command is received (SSRW bit=0), read the SBUF register, clear SIORW bit to receive next byte, then write SIO_ADR to clear SIORDY bit and stop pulling low the SCL pin for receiving next byte from master. The output acknowledge bit is controlled by STXNAK bit.

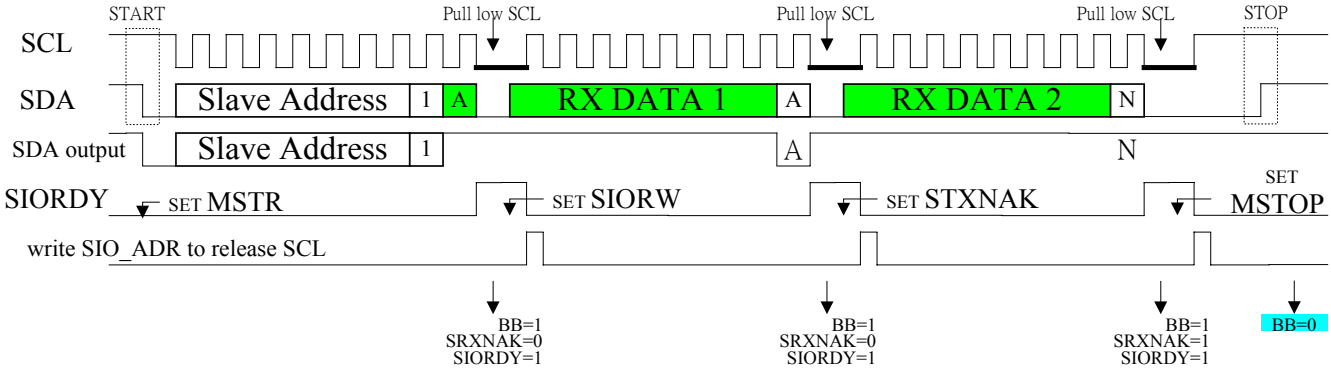
If a read command is received (SSRW bit=1), write data to SBUF register, clear SIORW bit and write SIO_ADR register to clear SIORDY bit and stop pulling low the SCL pin for master sending out clock The received acknowledge bit is stored in SRXNAK bit.

Master I²C Data Sequence

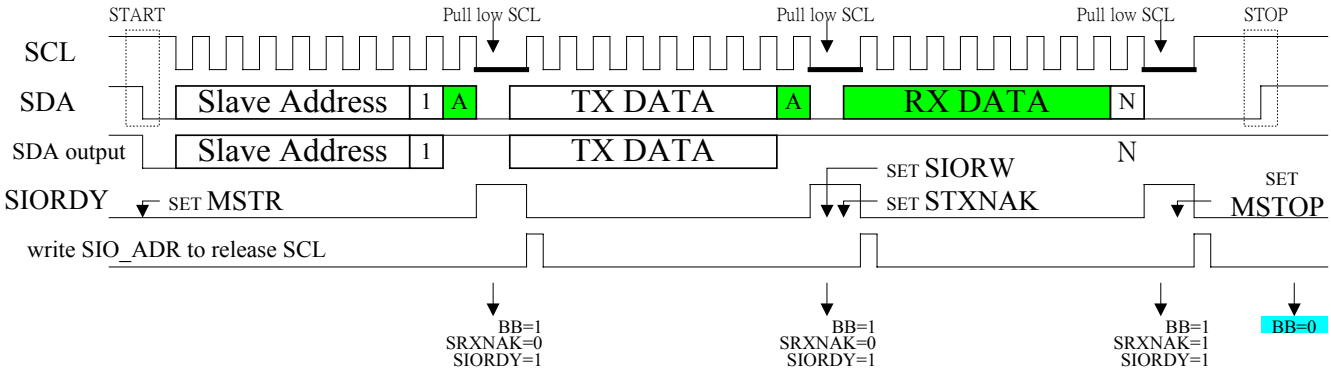
(1) Write mode :



(2) Read mode (I) :

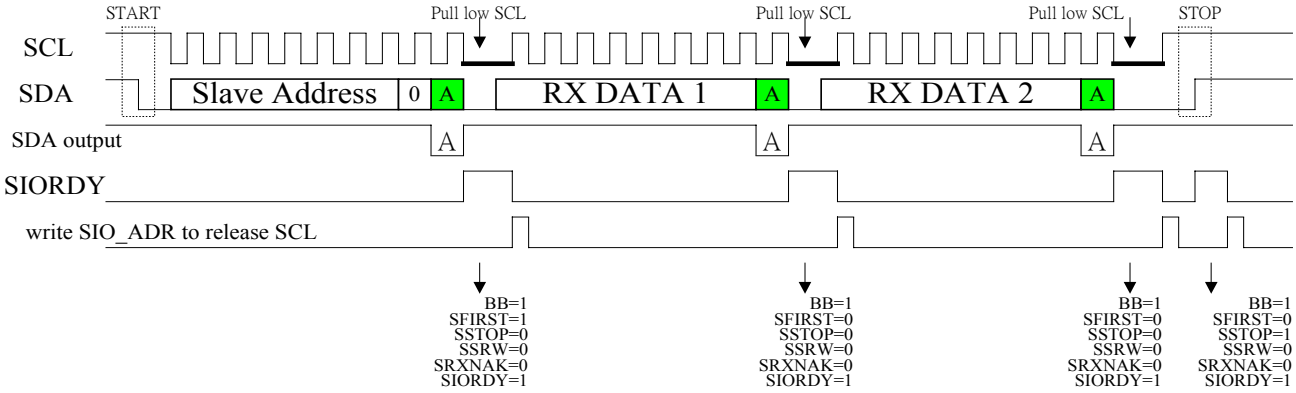


(3) Read mode (II) :

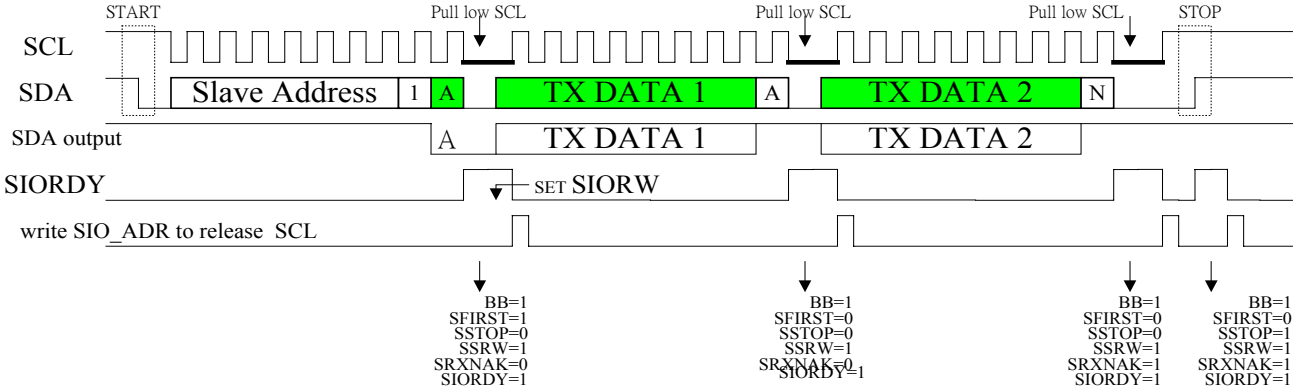


Slave I²C Data Sequence

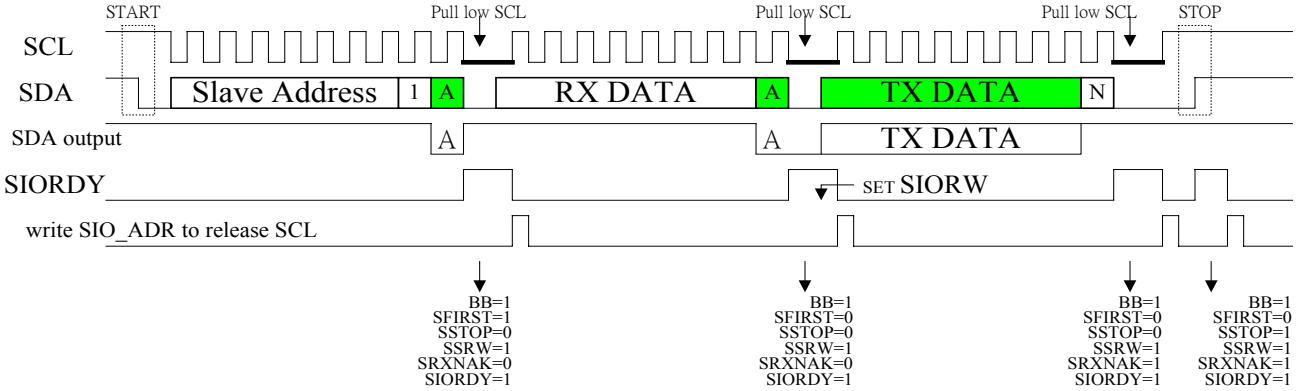
(1) Write mode :



(2) Read mode (I) :



(3) Read mode (II) :



Bit Name	Description
BB	"1" : Bus busy. "0" : Bus idle. Both SDA2 and SCL2 pins keep in high level for 5us after STOP condition.
SFIRST	This bit is set when received START and first byte in slave mode.
SSTOP	This bit is set when received STOP condition in slave mode.
SSRW	Received R/W bit in slave mode. "1" : Read command is received. "0" : Write command is received.
SRXNAK	"1" : NACK is received. "0" : ACK is received.
SIORDY	This bit is set when a byte is received, transmitted or STOP condition is detected.

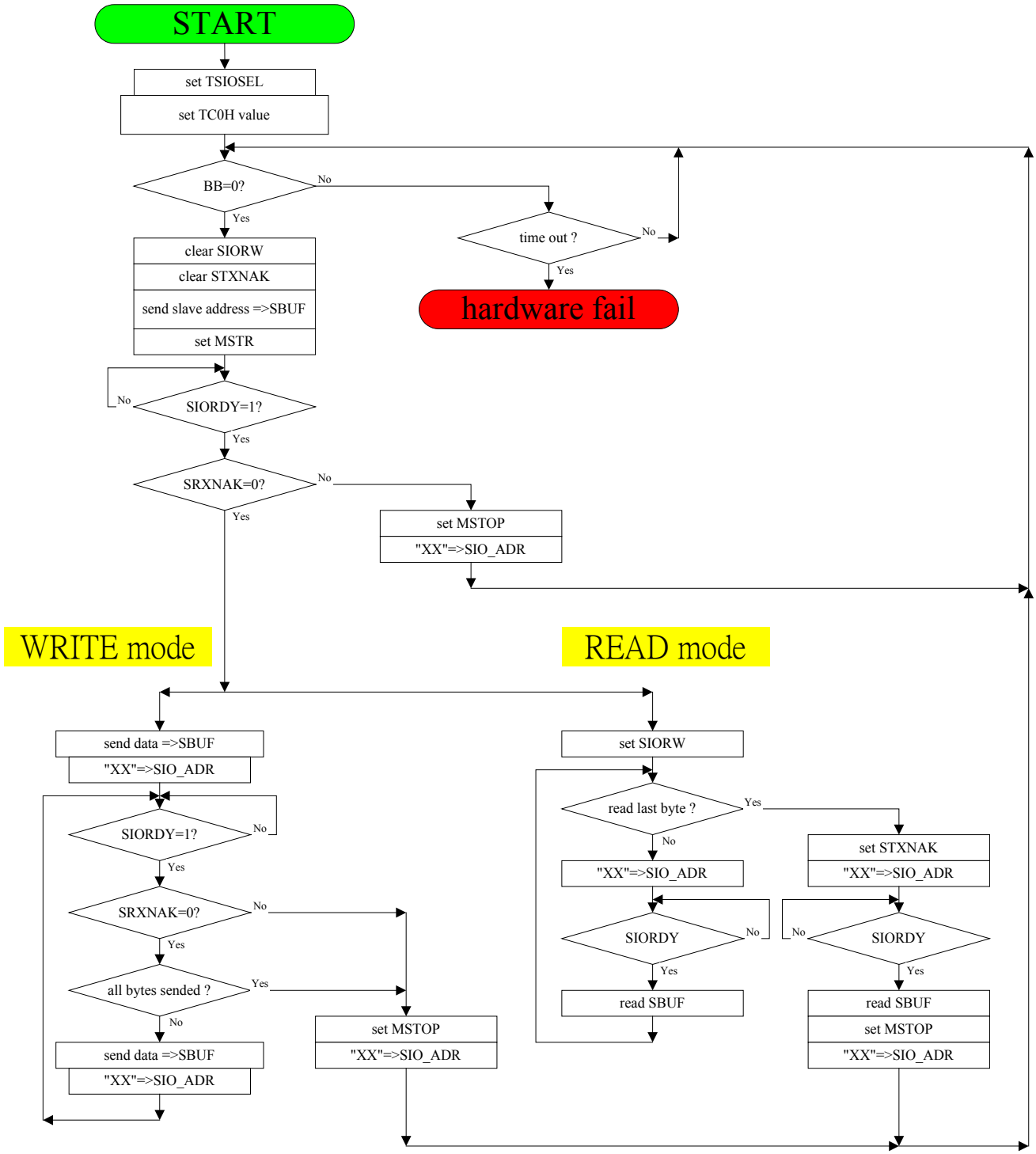
Bit Name	Description
MSTR	Output START condition in master mode when this bit is set.
MSTOP	Output STOP condition in master mode when this bit is set.
SIORW	"0" : Transmitter , "1" : Receiver in master mode. "1" : Transmitter , "0" : Receiver in slave mode ("0" : I2C write mode, "1" : I2C read mode.)
STXNAK	"1" : Output NACK. "0" : Output ACK. It will pull low the SDA pin on acknowledge bit.
SLAVE	"1" : Slave mode. "0" : Master mode.

I^2C interface Address Register

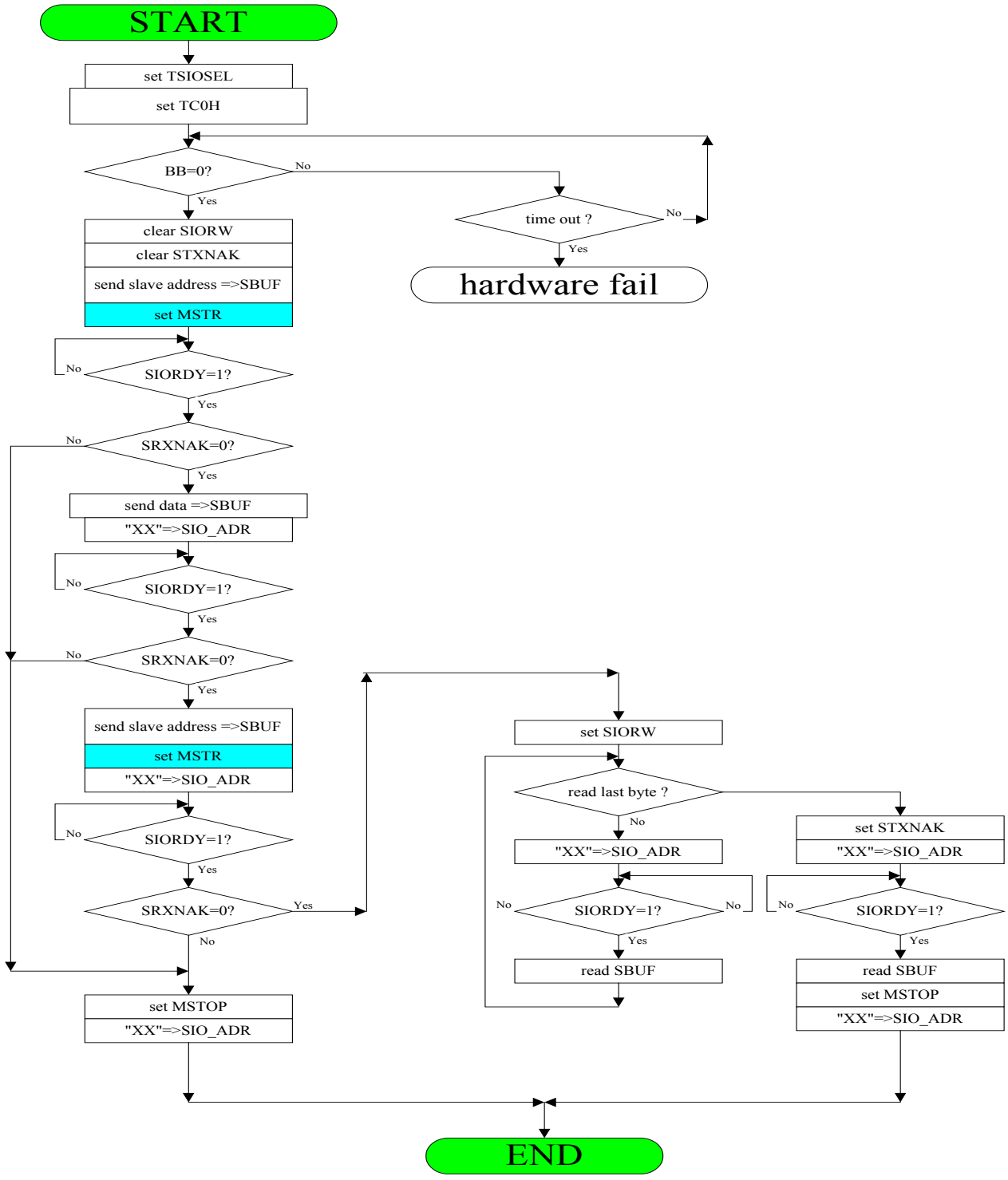
Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
SIO_ADR	0020h	W	xxh	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	--

Bit Name	Description
SAR7 ~ SAR1	7-bit address to be compared in slave mode.

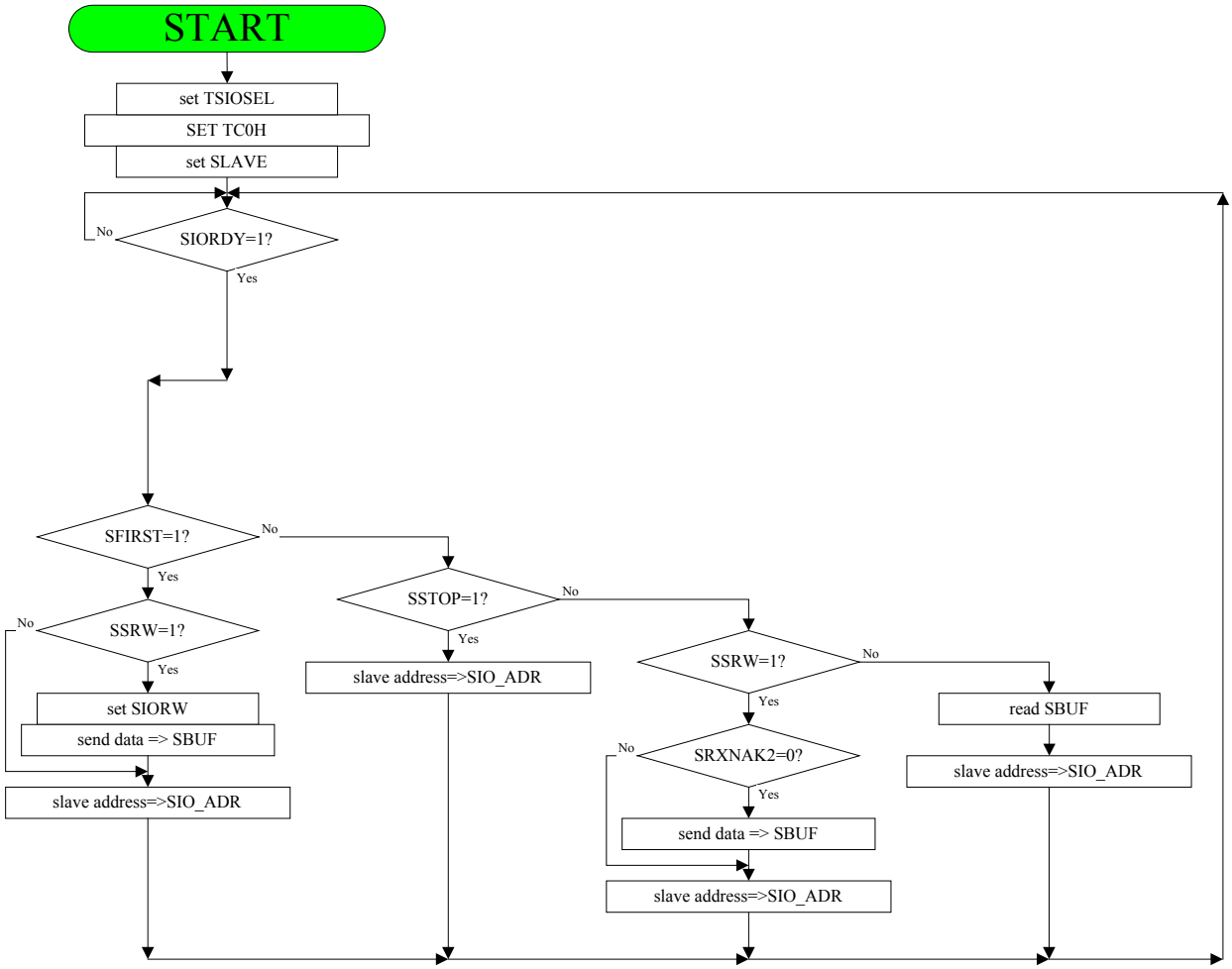
Master I²C Flow Chart



Master I²C (restart mode) Flow Chart

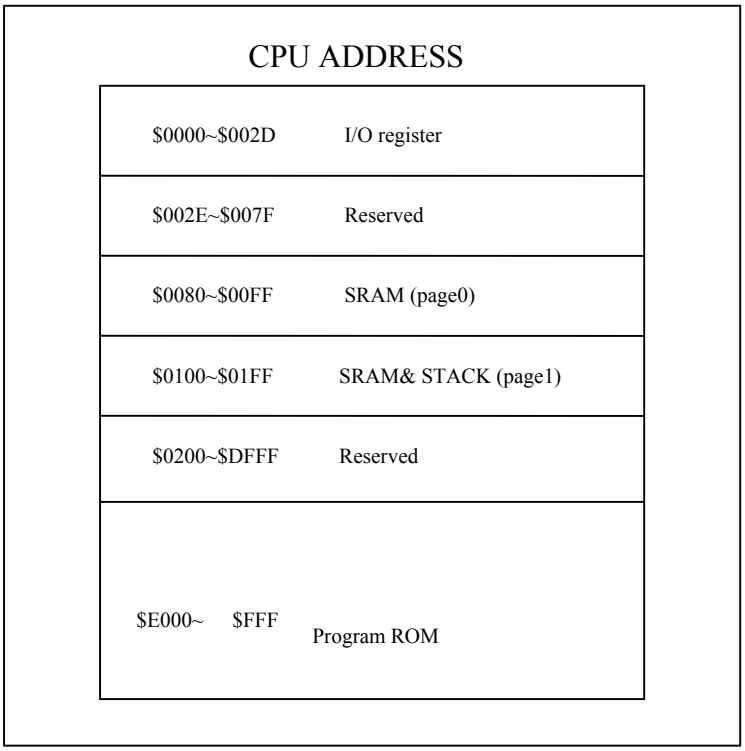


Slave I²C Flow Chart

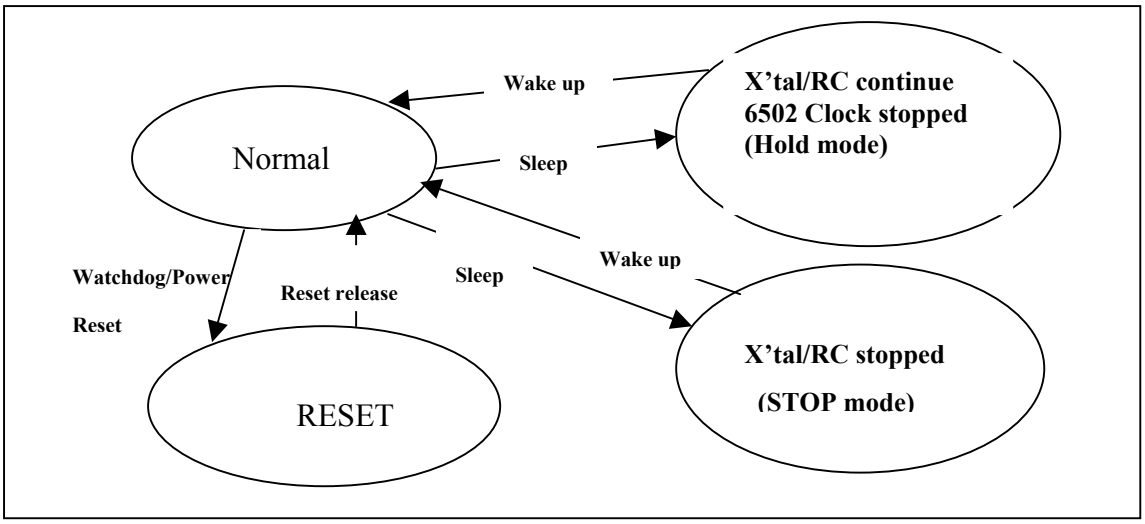


【7】MEMORY MAP

The following figure shows the location of memory mapping.



【8】STAND-BY MODES



SLPST register ($09), Write

Write: Sleep start

To get into sleep mode, the program should be written as below (two consecutive instructions):

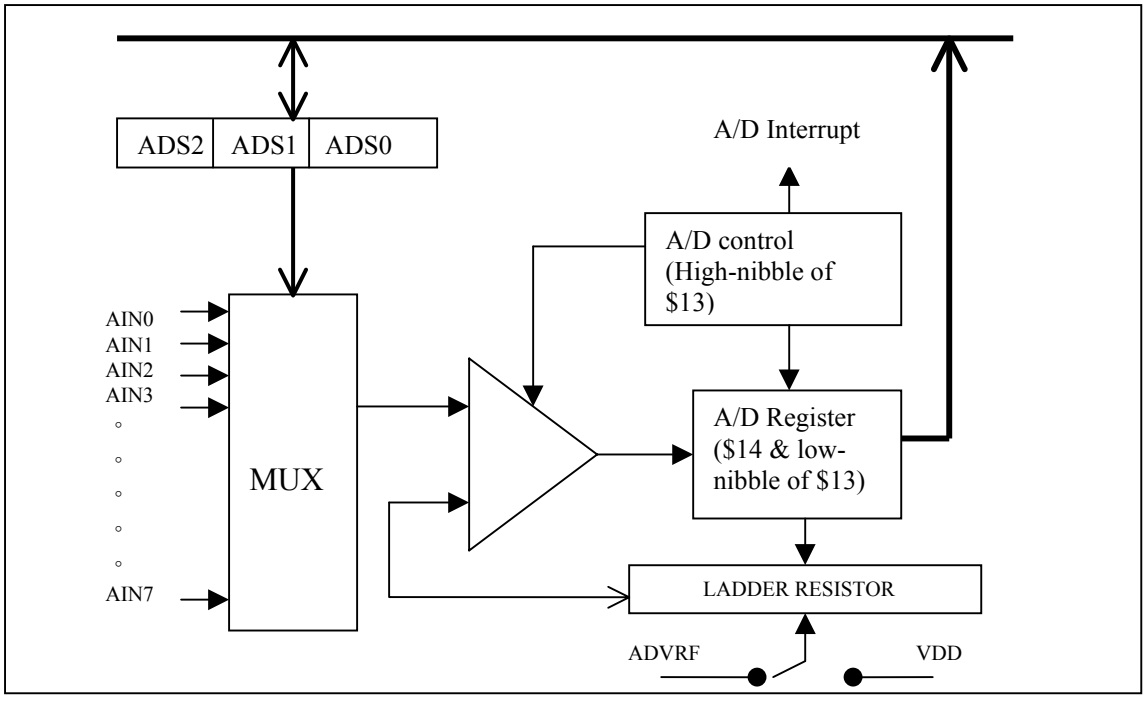
STA 08_H

STA 09_H

Before get into sleep mode make sure set up the suitable interrupt source that your system need, the interrupt vector will wake up either “STOP” or “HOLD” mode.

【9】A/D CONVERTER

A 12-bit successive approximation method is used in this A/D converter, as shown in the following figure. By multiplexing method, this A/D converter can manage up to eight analog inputs. A/D conversion is started by a write operation to the analog input selection bit in the A/D control register and by selecting the analog voltage input pins. When the conversion is completed, the A/D interrupt request bit in the interrupt request register is set. The result of A/D conversion is stored in the A/D register. During A/D conversion stage, the A/D register must not be read, otherwise the incorrect value may be obtained.



ADCR ($13): A/D control register;

b7: A/D On/Off control;

b7=0, A/D Off(default); b7=1, A/D On (write)

b3:b0: High-nibble of A/D data

B7	B6	B5	B4	B3	B2	B1	B0
ADON	CKS1	CKS0	CKS2	B3	B2/ADS2	B1/ADS1	B0/ADS0

CKS2	CKS1	CKS0	Input Clock Selection
0	0	0	Φ_0/4(when CPU clock is 1MHz, this option is recommended)
0	0	1	Φ_0/8(when CPU clock is 2MHz, this option is recommended)
0	1	0	Φ_0/16(when CPU clock is 4 MHz, this option is recommended)
0	1	1	Φ_0/32(when CPU clock is 8MHz, this option is recommended)
1	0	0	Φ_0/2(when CPU clock is 400KHz, this option is recommended)
1	0	1	Φ_0 (when CPU clock is 32KHz, this option is recommended)

* Φ_0 represents CPU/System clock

ADS2	ADS1	ADS0	Input Selection
0	0	0	AIN0
0	0	1	AIN1
0	1	0	AIN2
0	1	1	AIN3
1	0	0	AIN4
1	0	1	AIN5
1	1	0	AIN6
1	1	1	AIN7

ADR ($14): A/D register; Low Byte of A/D data [D7~D0; note: D11~D8 in register ADCR ($13)]

【10】LCD DRIVER/CONTROLLER

The WT50F5 contains 64-segment LCD driver/controllers and it has circuit that directly drives the Liquid Crystal Display (LCD) and its control circuit.

The WT50F5 has the following connecting pins with

(1) Segment output; 16 pins (SEG1-SEG16)
(2) Common output; 4 pins (COM1-COM4)

In addition, VCAP1, VCAP2, VCAP3, and V_{LCD} are bias voltage input pins to drive the LCD. In power saving mode, VCAP1, VCAP2 and VCAP3 should be connected with 0.01*u*F capacitors.
The devices that can be directly driven is selected for LCD drivers of following drive methods:

(1) 1/4 duty (1/3 bias) LCD; Max. 64 segments (8 segments X 8 digits)
(2) 1/3 duty (1/3 bias) LCD; Max. 48 segments (8 segments X 6 digits)
(3) 1/3 duty (1/2 bias) LCD; Max. 48 segments (8 segments X 6 digits)
(3) 1/2 duty (1/2 bias) LCD; Max. 32 segments (8 segments X 4 digits)

Control of LCD Driver

LCDC ($15); b5-b0, Write, initial value 00H

b7	b6	b5	b4	b3	b2	b1	b0
-	**-**	**LFS2**	**LCDPS**	**LFS1**	**LFS0**	**DTY1**	**DTY0**

DTY1	DTY0	Duty & Bias Selection
0	**0**	**1/4 duty (1/3 bias)**
0	**1**	**1/3 duty (1/3 bias)**
1	**0**	**1/3 duty (1/2 bias)**
1	**1**	**1/2 duty (1/2 bias)**

LFS2	LFS1	LFS0	LCD frequency select (frequency=64Hz)
0	**0**	**0**	**When OSC ≈ 4MHz, this option is recommended**
	0	**1**	**When OSC ≈ 8MHz, this option is recommended**
	1	**0**	**When OSC ≈ 2MHz, this option is recommended**
	1	**1**	**When OSC ≈ 1MHz, this option is recommended**
1	**0**	**0**	**When OSC ≈500KHz, this option is recommended**
	0	**1**	**When OSC ≈ 32KHZ, this option is recommended**

LCDPS	LCD power saving select

0	**Normal mode**
1	**LCD power saving mode**

Note: Initially this system is in normal mode, once the LCD is lit then, after around 1 second, this system can be switched to power saving mode for power saving. But, please be careful that the LCD can ONLY be turned on by using normal mode (can't use power saving mode) when it being turned off and would like to turn it on again.

Frame Frequency

Base Freq. @64Hz	1/4 Duty	1/3 Duty	1/2 Duty
Frame Freq.	f = 256 Hz	f = 192 Hz	f = 128 Hz

LCD Drive Voltage

The LCD is on only when the difference in potential between the segment output and common output is $+V_{ON}$ or $-V_{ON}$, and turn off at all other cases, where V_{ON} is the voltage value on V_{LCD} pin. If CPU and LCD drive voltage are different, control P1LCD=1 then VLCD pin is connected to VDD through a 100K ohm variable resister, R; otherwise, if CPU and LCD drive voltage are the same, control P1LCD=0 then LCD driver voltage is connected to VDD internally. If V_R is the voltage drop on R, then V_{ON}= VDD - V_R

LCD Display Operation

The display data stored to the display data area are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Thus, display patterns can be changed easily by overwriting the contents of the display data area with a program.

DISPLAY DATA AREA

Write the following assigned area

	SEG1-SEG8	SEG9-SEG16
COM1	**DDA11 ($16)**	**DDA12 ($17)**
COM2	**DDA21 ($1A)**	**DDA22 ($1B)**
COM3	**DDA31 ($1E)**	**DDA32 ($1F)**
COM4	**DDA41 ($22)**	**DDA42 ($23)**

1/4 DUTY	COM4	COM3	COM2	COM1
1/3 DUTY	P17	COM3	COM2	COM1
1/2 DUTY	P17	P16	COM2	COM1

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (VSS=0 V)

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	VDD	< +7	V
Input Voltage Range	Vin	-0.5 ~ VDD+0.5	V
Operating Temperature	T_{opr}	0 ~ +70	° C
Storage Temperature	T_{stg}	-50 ~ +150	° C

ELECTRICAL CHARACTERISTICS (VSS=0 V, T_{opr} = 0 to 70 ° C)

PARAMETER	SYMBOL	Min.	Typ.	Max.	Unit	CONDITIONS
Operating Voltage	VDD	2.7	-	5.5	V	
Operating Current	I_{OP}			2	*m* A	OSC 4MHz @ 5.0V
Hold Standby Current	I_{HOLD}			8	μA	OSC 32KHz@3.0V, LCD Turn-on
STOP Standby Current	I_{STOP}			1.0	μA	VDD=3.0V
OSC Frequency	F_{OSC}			8.0	MHz	VDD=5.0V
Input High Level	V_{IH}	4.0 2.5			V	VDD=5.0V VDD=3.0V
Input Low Level	V_{IL}			0.8 0.5	V	VDD=5.0V VDD=3.0V
Port 10~P13 Output High I (I/O)	I_{OH}		25		*m*A	VDD=5.0V Voh=4.0V
Port 14~P17 Output High I (I/O)	I_{OH}	4			*m*A	VDD=5.0V Voh=4.0V
Port 1 Output Sink I (I/O)	I_{OL}		25		*m*A	VDD=5.0V Vol=0.8V
Port 0,2 , 3 & 4 Output High I (I/O)	I_{OH}	4			*m*A	VDD=5.0V Voh=4.0V
Port 0, 2 , 3 & 4 Output Sink I (I/O)	I_{OL}	4			*m*A	VDD=5.0V Vol=0.8V
CPU Clock	F_{CPU}	0.03		8.0	MHz	$F_{CPU}=F_{OSC}$ @5.0V

A/D CONVERSION CHARACTERISTICS (T_{opr} = 0 to 70 ° C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	AD_{VRF}		3.0	-	AV_{DD}	V
Valid Voltage Range	V_{RNG}	AD_{VRF}=5V	0.05		4.95	V
Valid Voltage Range	V_{RNG}	AD_{VRF}=3V	0.05		2.95	V
Analog Input Voltage	AV_{IN}		AV_{SS}	-	AV_{DD}	V
Analog Supply Current	I_{REF}		-	0.5	1	*m*A
Input Impedance	Z		-	20		*M* Ω

Differential nonlinear error[1]	E_{NL}				±1	*LSB*
Integral nonlinear error[2]	E_{INL}				±2	*LSB*
Offset error[3]	E_{OS}				±2	*LSB*
Absolute Error[4]	E_{ABS}	VDD=5V,V_{SS}=0V AD_{VRF}=5V,AV_{SS}=0V	-	-	±3	LSB
Conversion Time	T_{CV}		-	-	30	μS

1. The differential nonlinear error (E_{NL}) is the step width difference of the actual and the ideal transfer curves.
2. The integral nonlinear error (E_{INL}) is the peak difference between the centers of the actual and the ideal transfer curves.
3. The offset error (E_{OS}) is the absolute difference of the straight lines, which fit the actual and the ideal transfer curves.
4. The absolute error (E_{ABS}) is the maximum difference between the center of the steps of the actual and the ideal transfer curves for a non-calibrated ADC.