Jess Technology Co., Ltd.
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DESCRIPTION

The WT5082 is a high-performance, low-cost, CMOS 8-bit single-chip micro-controller with POCSAG decoder、12KB SRAM 、296KB ROM and 56x32 / 56x33 dot-matrix LCD driver embedded, which is suitable for information paging applications, especially when large number of LCD dots and large ROM and SRAM space are needed, such as Chinese character display pagers.

This chip has 8-bit CPU, RAM, ROM, I/Os, two timers/counters, interrupt controller, LCD driver and watchdog timer. To be suitable for portable battery-powered applications, a power saving function is included.

FEATURES

- POCSAG pager code decoder
  - ✧ Single crystal support 512, 1200 and 2400 baud rates (76.8kHz crystal)
  - ✧ Support 6 RICs addresses and 6 independent frame numbers
  - ✧ Support partial address match facility for address F (up to 260k addresses are provided)
  - ✧ 3 RF control lines (PLL, quick charge and enable)
  - ✧ Build in data filter (16-times over-sampling) and data bit clock recovery
  - ✧ Interrupt 6502 CPU when there are any status change
  - ✧ DMA or interrupt mode to send the received message data to CPU
- 8-bit single chip Microcontroller with 56x32 / 56x33 LCD driver
- 12Kbytes SRAM (~ 2K bits for LCD display SRAM) , 256 Kbytes character pattern ROM , 32Kbytes program ROM and 8Kbytes ROM for test program
- Wide voltage operating range from 2.5 V to 3.6 V
- Built-in Ring Oscillator with maximum frequency up to 2.0 MHz
- I/O port (21 pins)
  - Input port 8 pins
  - Input/output port 13 pins
- Watchdog Timer
- Operating current 0.5mA / 1MHz @ 3V **;** providing standby mode and key wake-up mode
  - ✧ Ring OSC OFF and 76.8KHz X'tal OSC ON: current consumption < 60 *uA @ 3V*

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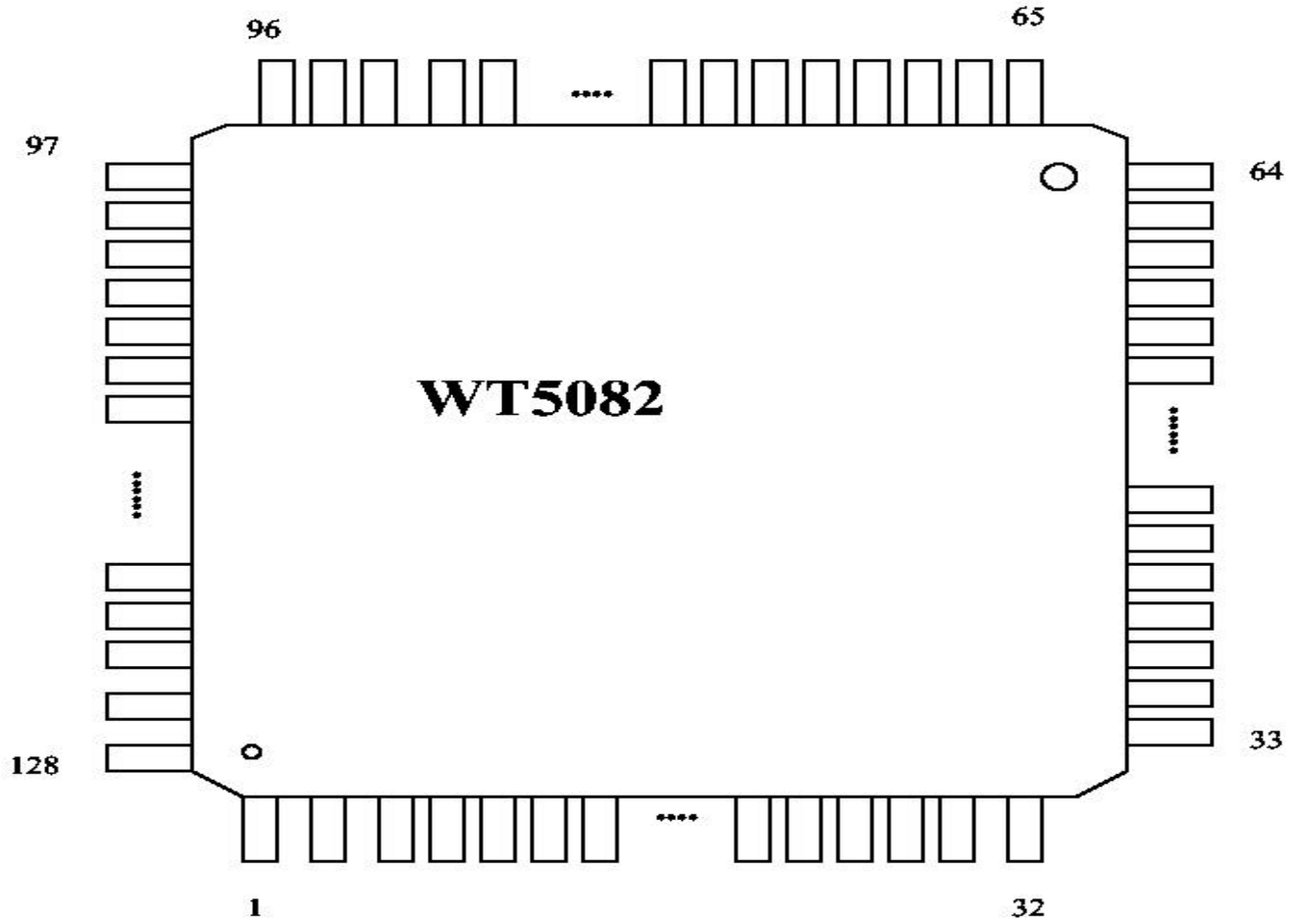
- ✧ Both 1Mhz OSC and 76.8KHz X'tal OSC are OFF: current consumption < 5 *uA @ 3V*
- ◆ Dual timer / counters
- ◆ 7-bit EPI (external port interrupt) for key wake-up interrupt
- ◆ l-bit EPI (external port interrupt to 6502 NMI) for battery remove detect
- ◆ SIO for flex decoder (32bit)
- ◆ UART(10 bits)
- ◆ One PWM signal function
- ◆ 2.2V threshold automatic power on reset
- ◆ 2.0V low power reset
- ◆ Package: Chip form or 128-pin LQFP (14mm x 14mm x 1.4mm)

PACKAGE OUTLINE



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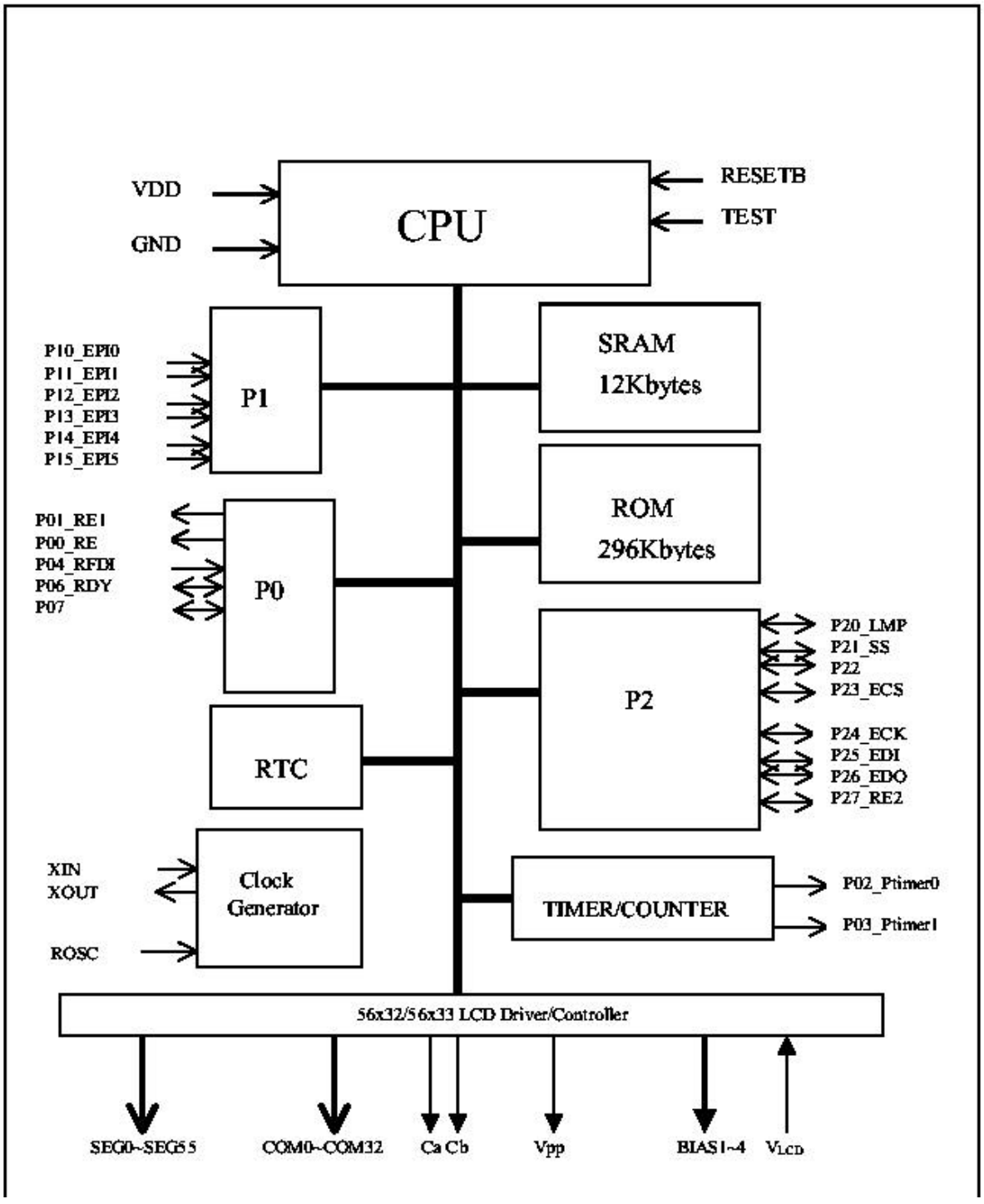
BLOCK DIAGRAM



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***PIN FUNCTION* (128-pin LQFP)**

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SEG 32 ~ SEG 55	49	P	Power Source
COM 31 ~ COM 16	50 ~ 73	Output	LCD segment output
COM 32	74 ~ 89	Output	LCD common output
BIAS 1 ~ BIAS 4	90	Output	LCD common output (for ICON)
V_{LCD}	91 ~ 94	Output	LCD bias voltage output
V_{PP}	95	Input	LCD voltage supply
Cb	96	Output	V_{RO}*2
Ca	97	Output	LCD pumping capacitor
P14 _ EPI4	98	Output	LCD pumping capacitor
P15 _ EPI5	99	Input	EPI4 , Battery low detect
P20 _ LMP	100	Input	EPI5 , Battery low detect
P21 _ SS	101	I / O	General I/O or Lamp output
P22	102	I / O	General I/O , SS output pin for Serial I/O or UART serial output
P23 _ ECS	103	I / O	General I/O or PLL _ LE
P24 _ ECK	104	I / O	General I/O for EEPROM CS
P25 _ EDI	105	I / O	General I/O , for EEPROM CK & PLL CK
P26 _ EDO	106	I / O	General I/O for EEPROM DI & PLL DATA
P27 _ RE2	107	I / O	General I/O for EEPROM DO
P06 _ RDY	108	I / O	RF control signal 2 output (RF enable) or MISO input pin for Serial I/O
P01 _ RE1	109	I / O	General I/O or RDY input pin for Serial I/O ; EPI6 or UART Serial Input
P00 _ RE	110	Output	RF control signal 2 output (RF enable) or MISO input pin for Serial I/O
P04 _ RFDI	111	Output	RF control signal output or SCK output pin for SIO
P07	112	Input	RF signal data input
P10 _ EPI0 ~	113	I / O	General I/O port , Input port for EPI7 or PWM signal output
P13 _ EPI3	114 - 117	Input	4-bit input port for External interrupt and general input
RESETB	118	Input	System reset signal input ; low active
GND	119	P	Ground
XIN	120	Input	Crystal input
XOUT	121	Output	Crystal output
VDD	122	P	Power source
ROSC	123	Input	Resistor for ring oscillator
P02 _ Ptimer0	124	I / O	General I/O port or output from ptimer0
P03 _ Ptimer1	125	I / O	General I/O port or output from ptimer1
768KO	126	Output	76.8KHz clock output for FLEX decoder or PWM Enable control signal
TEST	127	Input	Test pin. High active
COM0	128	Output	LCD common output

APPLICATION DIAGRAM

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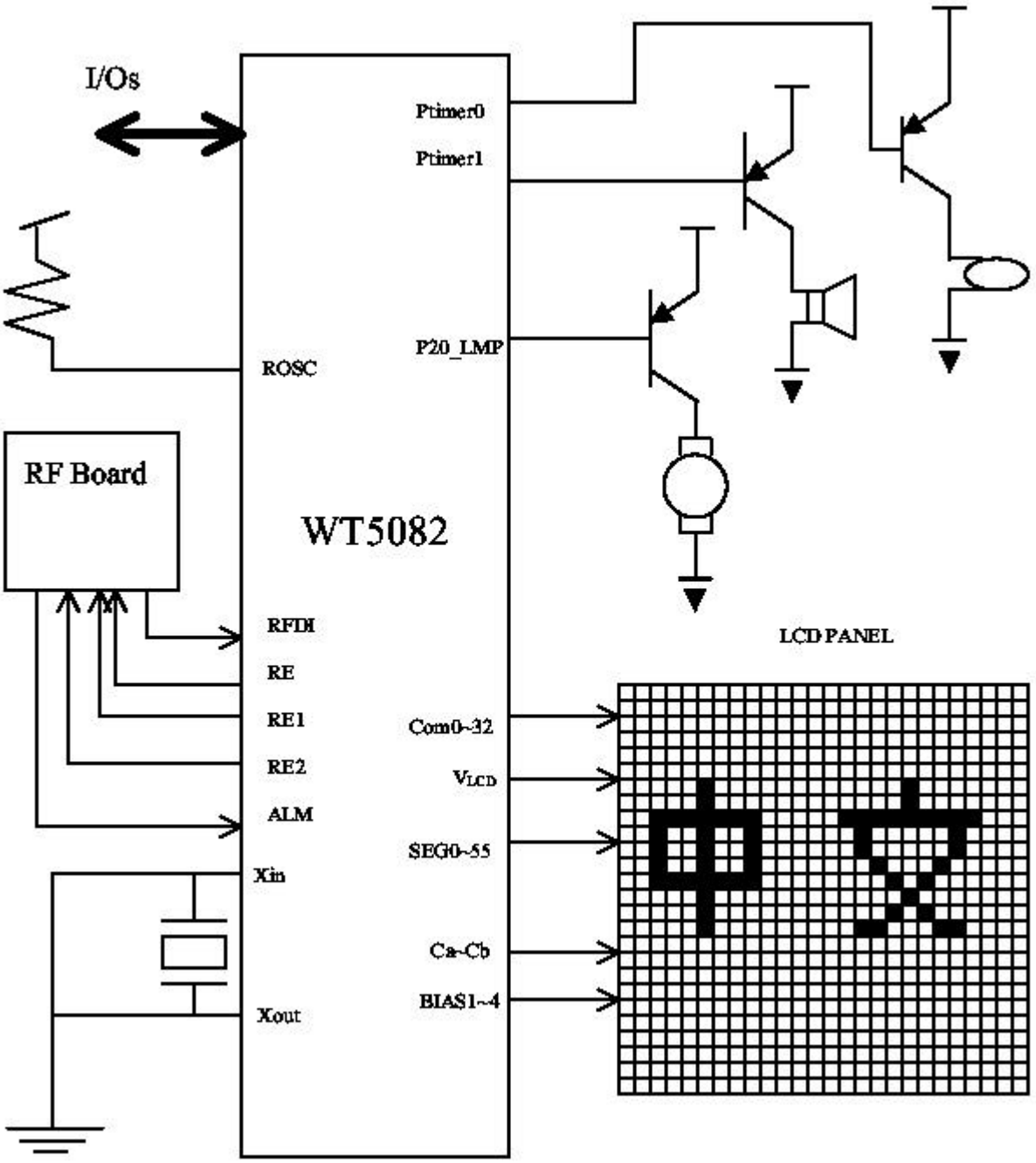

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SECTION 1. MEMORY CONFIGRATION

(MEMORY MAP & INTERNAL MEMORY CONFIGRUATION)

CPU MEMORY ADDRESS	FUNCTION	ADDRESS SPACE (bytes)
$0000 - $004F	PORT / REGISTERS	80
$0050 - $00FF	INTERNAL SRAM	176
$0100 - $01FF	6502STACK	256
$0200 - $2EFF	SRAM	11K
$2F19 - $3F18	Reserved	3K
$3F19 - $3FF8	LCD Display SRAM Buffer	224
$3FF9 - $3FFF	LCD Icon SRAM Buffer	7
$4000 - $5FFF	Font ROM Window1	8K
$6000 - $7FFF	Font ROM Window2	8K
$8000 - $FFF1	PROGRAM ROM	~ 32K
$FFFA - $FFFF	INTERRUPT ECTOR	6

Vector address	Vector type
$FFFA - $FFFB	NMI vector
$FFFC - $FFFD	Reset vector
$FFFE - $FFFF	IRQ vector

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SECTION 2. TABLE OF SPECIAL REGISTERS

ADDR	NAME	Read Write	Bit number							
			7	6	5	4	3	2	1	0
00H	Port P0 DIR **P0DIR**	R / W	P07D	P06D	—	—	P03D	P02D		
01H	Port P0 CFG **P0CFG**	R / W	P07C	P06C	—	P04C	P03C	P02C	P01C	P00C
02H	Port P0 Data **P0DAT**	R / W	P07	P06	—	P04	P03	P02	—	—
03H	Port P1 CFG **P1CFG**	R / W	—	—	P15C	P14C	P13C	P12C	P11C	P10C
04H	Port P1 Data **P1DAT**	R	—	—	P15	P14	P13	P12	P11	P10
05H	Port P2 Direction **P2DIR**	R / W	P27D	P26D	P25D	P24D	P23D	P22D	P21D	P20D
06H	Port P2 configuration **P2CFG**	R / W	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
07H	Port P2 Data **P2DAT**	R / W	—	P26	P25	P24	P23	P22	P21	P20
08H	Whtchdog Timer Control **WDTCTL**	R / W	WEN	—	—	—	—	—	WCK1	WCK0
09H	Port Timer0 Control **PT0CTL**	R / W	EPT0	—	PT0S	OPT0	—		PTS01	PTS00
0AH	Port Timer0 Preload Data **PTIME0**	W	PT07	PT06	PT05	PT04	PT03	PT02	PT01	PT00
0BH	Port Timer0 Count value **TIMER0**	R	T07	T06	T05	T04	T03	T02	T01	T00
0CH	Port Timer1Control **PT1CTL**	R / W	EPT1	—	PT1S	OPT1	—	—	PTS11	PTS10
0DH	Port Timer1 Preload Data **PTIME1**	W	PT17	PT16	PT15	PT14	PT13	PT12	PT11	PT10
0EH	Port Timer1 Count value **TIMER1**	R	T17	T16	T15	T14	T13	T12	T11	T10
0FH	Cpu Halt register **HALT**	W	×	×	×	×	×	×	×	×

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ADDR	NAME	Read Write	Bit number							
			7	6	5	4	3	2	1	0
10H	Time Base Timer Control **BTCTL**	R / W	EBT	—	—	—	—	—	BTS1	BTS0
11H	Time Base Timer Preload data **BTIME**	W	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0
12H	Time Base Counter Value **TIMERB**	R	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
13H	RTC timer control **RTCCTL**	R / W	—	—	RT11	RT10	—	—	RT01	RT00
14H	RTC Hour register **Hour**	R / W	SET	0	—	H4	H3	H2	H1	H0
15H	RTC Minute register **Minute**	R / W	—	—	M5	M4	M3	M2	M1	M0
16H	RTC Minute register **Second**	R / W	—	—	S5	S4	S3	S2	S1	S0
17H	IRQ Interrupt Mask **IRQMK**	R / W	—	MRTC	MSIO	MRT1	MRT0	MBT	MPT1	MPT0
18H	IRQ Interrupt Status **IRQSR**	R	FEP1	FRTC	FSIO	FRT1	FRT0	FBT	FPT1	FPT0
19H	EPI Interrupt Mask **EPIMK**	R / W	EEP17	EEP16	EEP15	EEP14	EEP13	EEP12	EEP11	EEP10
1AH	EPI Interrupt Status **EPISR**	R	EP17	EP16	EP15	EP14	EP13	EP12	EP11	EP10
1BH	Inverse EPI signal **IEP1**	R / W	IEP17	IEP16	IEP15	IEP14	IEP13	IEP12	IEP11	IEP10
1CH	P_decoder Interrupt Mask **PDIMK**	R / W	EPD17	EPD16	EPD15	EPD14	EPD13	EPD12	EPD11	EPD10
1DH	P_decoder Interrupt Status **PDISR**	R	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10
1EH	Expand ROM Window0 Address **ROMWinADR0**	R / W	—	—	—	W0A4	W0A3	W0A2	W0A1	W0A0
1FH	Expand ROM Window1 Address **ROMWinADR1**	R / W	—	—	—	W1A4	W1A3	W1A2	W1A1	W1A0

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ADDR	NAME	Read Write	Bit number							
			7	6	5	4	3	2	1	0
20H	P_decoder Control **PDCTL**	R / W	OverRange	LostSync	ErrorFlag	0	EPDMA	REON	PDEOM	PDON
21H	P_decoder Receive Data **PDDR**	R	PDD7	PDD6	PDD5	PDD4	PDD3	PDD2	PDD1	PDD(
22H	P_decoder DMA mode Address pointer (low byte) **PDDRpH**	R	PDA7	PDA6	PDA5	PDA4	PDA3	PDA2	PDA1	PDA(
23H	PDDR DMA mode Address pointer (high byte and Base Address) **MPDDRp**	R / W	—	—	PDBA3	PDBA2	PDBA1	PDBA0	PDA9	PDA8
24H	PDDRp pointer mask **MPDDRp**	R / W	MCL	ADCL	—	—	MPDA9	MPDA8	MPDA7	MPDA
25H	P_decoder EOM mark **PDEOM**	R / W	EOM7	EOM6	EOM5	EOM4	EOM3	EOM2	EOM1	EOM(
26H	LCD Dis[play Control **LCDCTL**	R / W	—	LCDPMP	LCDDC	LCDI	FRQS3	FRQS2	FRQS1	FRQS
27H	Serial I/O Control **SIOCTL**	R / W	SIOE	—	—	—	—	—	—	SCK(
28H	SIO Data Buffer 0 **SIOB0**	R / W	SIOB07	SIOB06	SIOB05	SIOB04	SIOB03	SIOB02	SIOB01	SIOB(
29H	SIO Data Buffer 1 **SIOB1**	R / W	SIOB15	SIOB14	SIOB13	SIOB12	SIOB11	SIOB10	SIOB9	SIOB8
2AH	SIO Data Buffer 2 **SIOB2**	R / W	SIOB23	SIOB22	SIOB21	SIOB20	SIOB19	SIOB18	SIOB17	SIOB1
2BH	SIO Data Buffer 3 **SIOB3**	R / W	SIOB31	SIOB30	SIOB29	SIOB28	SIOB27	SIOB26	SIOB25	SIOB2
2CH	UART Control **UARTCTL**	R / W	EUART	—	RX_FULL	TX_Empty	—	—	—	UART_T
2DH	PWM Control **PWMCTL**	R / W	EPWM	—	PWM_TX	ClrPadr	Plndex3	Plndex2	Plndex1	Plndex
2EH	PWM Data Buffer **PWMB**	R / W	PWMB7	PWMB6	PWMB5	PWMB4	PWMB3	PWMB2	PWMB1	PWMB
2FH	System Clock Control **CKCTL**	R / W	PLL4	PLL3	PLL2	PLL1	PLL0	CK2	CK1	CK0

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ADDR	NAME	Read Write	Bit number							
			7	6	5	4	3	2	1	0
30H	P_DECODER CONFIGURATION **PDCONF0**	R / W	A00	A01	A02	A03	A04	A05	A06	A07
31H	P_DECODER CONFIGURATION **PDCONF1**	R / W	A08	A09	A10	A11	A12	A13	A14	A15
32H	P_DECODER CONFIGURATION **PDCONF2**	R / W	A16	A17	FA0	FA1	FA2	FCA1	FCA0	DSA
33H	P_DECODER CONFIGURATION **PDCONF3**	R / W	B00	B01	B02	B03	B04	B05	B06	B07
34H	P_DECODER CONFIGURATION **PDCONF4**	R / W	B08	B09	B10	B11	B12	B13	B14	B15
35H	P_DECODER CONFIGURATION **PDCONF5**	R / W	B16	B17	FB0	FB1	FB2	FCB1	FCB0	DSB
36H	P_DECODER CONFIGURATION **PDCONF6**	R / W	C00	C01	C02	C03	C04	C05	C06	C07
37H	P_DECODER CONFIGURATION **PDCONF7**	R / W	C08	C09	C10	C11	C12	C13	C14	C15
38H	P_DECODER CONFIGURATION **PDCONF8**	R / W	C16	C17	FC0	FC1	FC2	FCC1	FCC0	DSC
39H	P_DECODER CONFIGURATION **PDCONF9**	R / W	D00	D01	D02	D03	D04	D05	D06	D07
3AH	P_DECODER CONFIGURATION **PDCONF10**	R / W	D08	D09	D10	D11	D12	D13	D14	D15
3BH	P_DECODER CONFIGURATION **PDCONF11**	R / W	D16	D17	FD0	FD1	FD2	FCD1	FCD0	DSD
3CH	P_DECODER CONFIGURATION **PDCONF12**	R / W	E00	E01	E02	E03	E04	E05	E06	E07
3DH	P_DECODER CONFIGURATION **PDCONF13**	R / W	E08	E09	E10	E11	E12	E13	E14	E15
3EH	P_DECODER CONFIGURATION **PDCONF14**	R / W	E16	E17	FE0	FE1	FE2	FCE1	FCE0	DSE
3FH	P_DECODER CONFIGURATION **PDCONF15**	R / W	F00	F01	F02	F03	F04	F05	F06	F07

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ADDR	NAME	Read Write	Bit number							
			7	6	5	4	3	2	1	0
40H	P_DECODER CONFIGURATION **PDCONF16**	R / W	F08	F09	F10	F11	F12	F13	F14	F15
41H	P_DECODER CONFIGURATION **PDCONF17**	R / W	F16	F17	FF0	FF1	FF2	FCF1	FCF0	DSF
42H	P_DECODER CONFIGURATION **PDCONF18**	R / W	MF0	MF1	MF2	MF3	MF4	MF5	MF6	MF7
43H	P_DECODER CONFIGURATION **PDCONF19**	R / W	MF8	MF9	MF10	MF11	MF12	MF13	MF14	MF15
44H	P_DECODER CONFIGURATION **PDCONF20**	R / W	MF16	MF17	×00	×01	×02	×03	×04	×05
45H	P_DECODER CONFIGURATION **PDCONF21**	R / W	×06	×07	×08	0	0	×11	×12	×13
46H	P_DECODER CONFIGURATION **PDCONF22**	R / W	×14	×15	×16	×17	×18	×19	×20	×21
47H	P_DECODER CONFIGURATION **PDCONF23**	R / W	×22	×23	×24	×25	×26	×27	×28	×29
48H	P_DECODER CONFIGURATION **PDCONF24**	R / W	×30	×31	×32	×33	×34	1	1	1
49H	P_DECODER CONFIGURATION **PDCONF25**	R / W	×38	×39	×40	×41	×42	×43	×44	×45
4AH	P_DECODER CONFIGURATION **PDCONF26**	R / W	×46	×47	×48	×49	×50	×51	×52	×53
4BH ~ 4EH	Reserved									
4FH	P_Decoder Status (for Test) **PSTAT**	For Test only								

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SECTION 3. INPUT / OUTPUT PORTS

The WT5082 consists of three parallel ports, namely P0 , P1 and P2. And, these entire ports can be served for multiple purposes depend on the port configuration. All port are reset to input mode.

SECTION 3.1 PORT P0

The Port P0 is a 7 bits input and output port. Its functions are listed below and controlled by individual register. The EPI function is enabled when it is set as input.

Port		Function
P00 _ RE	Output	RF control signal output or SCK output pin for serial I/O
P01 _ RE1	Output	RF control signal 1 output (quick charge) or MOSI output pin for serial I/O
P02 _ Ptimer0	I/O	General output port or output from ptimer0
P03 _ Ptimer1	I/O	General output port or output from ptimer1
P04 _ RFDI	Input	RF signal data input
P06	I/O	General I/O or EPI6
P07	I/O	General I/O or EPI7

P0DIR (Port P0 Direction Register) **:** reset value 0xFF

Address	00H / R_W							
Bit no	7	6	5	4	3	2	1	0
	P07D	P06D	—	—	P03D	P02D	—	—

P0CFG (Port P0 Configuration Register) **:** reset value 0x00

Address	01H / R_W							
Bit no	7	6	5	4	3	2	1	0
	P07C	P06C	—	P04C	P03C	P02C	P01C	P00C

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P0DAT (Port P0 Data Register) **:** reset value 0x00

Address	02H / R_W							
Bit no	7	6	5	4	3	2	1	0
	P07	P06	—	P04	P03	P02	—	—

P00 , P01 is used for output only with RF control signal or Serial I/O.
User can set SIOE to enable P00 , P01 works with Serial I/O function.

SIOE	P00C / P01C	Function of Port P00 / P01
0	0	RE control output with Push-pull
0	1	RF control output with open drain
1	0	Serial I/O output with Push-pull
1	1	Serial I/O output with open drain

P02 , P03 is used for input and output with general output or Ptimer output.
User can set EPT0 , EPT1 to enable P02 , P03 works with Ptimer output.

P02D / P03D	OPT0 / OPT1	P02C / P03C	Function of Port P02 / P03
0	0	0	General output with Push-pull
0	0	1	General output with open drain
0	1	0	Ptimer output with Push-pull
0	1	1	Ptimer output with open drain
1	0	0	General input without pull-up
1	0	1	General input with pull-up

P04 is input only for RF signal Input.

P04C	Function of Port P04
0	Input without pull-up
1	Input with pull-up

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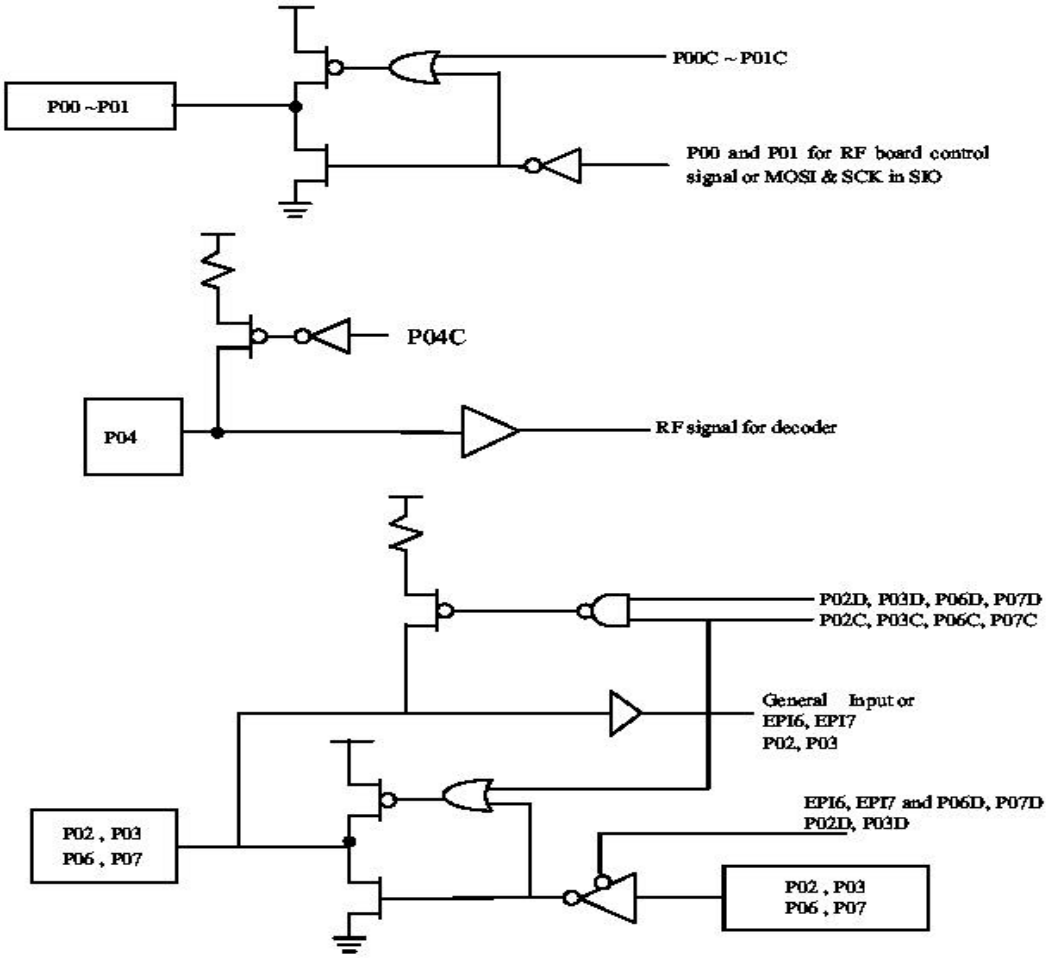
P06 , P07 is used to multi-function with general I/O and EPI input.
Set EPI6 , EPI7 can make P06 , P06 works with EPI interrupt.
Disable EPI6 , EPI7 , it works with a general I/O port.

EPI6 / EPI7	P06D / P07D	P06C / P07C	Function of Port P06 / P07
0	0	0	General output with Push-pull
0	0	1	General output with open drain
0	1	0	General input without pull-up
0	1	1	General input with pull-up
1	1	0	EPI input without pull-up
1	1	1	EPI input with pull-up



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SECTION 3.2.1 PORT P1 (External interrupt input port)

The P10 ~ P15 is served as an External Port Interrupt Function, and its configuration can be programmed by **P1CFG.**

P1CFG (Port P1 configuration Register) **:** reset value 0x00

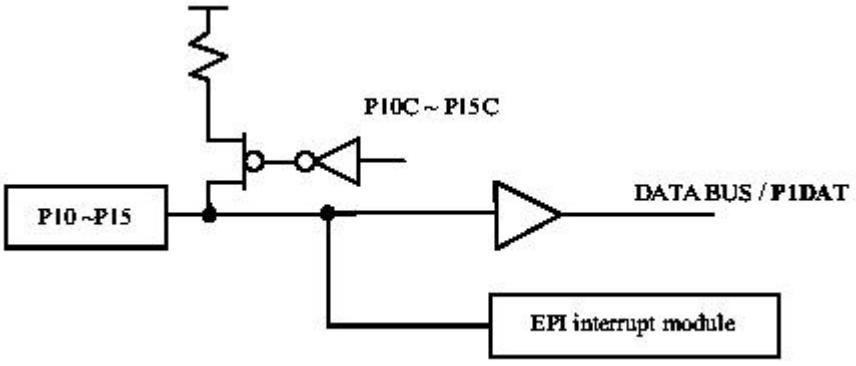
Address	03H / R_W							
Bit no	7	6	5	4	3	2	1	0
	—	—	P15C	P14C	P13C	P12C	P11C	P10C

P10C ~ P15C	Function of Port P10C ~ P15C
0	Input without pull-up
1	Input with pull-up

P1DAT (Port P1 data Register) **:** reset value 0x00

Address	04H / R_W							
Bit no	7	6	5	4	3	2	1	0
	—	—	P15	P14	P13	P12	P11	P10

P15 is also connect to NMI interrupt input when EPDI7 enable and EPI5 disable. P14 is used for Battery low detect. User can connect P14 with RF borad ALM signal, it will automatically detect ALM when RE active.



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SECTION 3.3 PORT P2 (general input and output port)

The Port.P2 is used for general I/O.

User can program it to communicate with EEPROM or Flex Decoder. Its direction can be set by **P2DIR.**

Out can be with or without open-drain by setting **PWCFG.** And Input can be with or without pull-up in the same way.

P2DAT (Port Data Register) **:** reset value 0x00

Address	07H / R_W							
Bit no	7	6	5	4	3	2	1	0
	—	P26	P25	P24	P23	P22	P21	P20

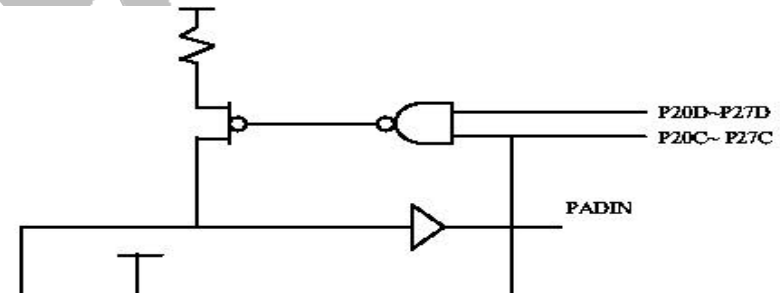
P2DIR (Port P2 direction Register) **:** reset value 0xFF

Address	05H / R_W							
Bit no	7	6	5	4	3	2	1	0
	P27D	P26D	P25D	P24D	P23D	P22D	P21D	P20D

P2CFG (Port P2 configuration Register) **:** reset value 0xFF

Address	06H / R_W							
Bit no	7	6	5	4	3	2	1	0
	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C

P2Xd	P2xC	Function of Port P06 / P07
0	0	Output with Push-pull
0	1	Output with open drain
1	0	Input without pull-up
1	1	Input with pull-up



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SECTION 4. CPU AND RELATIVE MODULES

The WT5082 includes one 6502 CPU module , and this section describes some 6502 functions that relative t the WT5082 application.

SECTION 4.1 CPU HALT CONTROL

HALT (CPU HALT Control register) **:** reset value 0x00

Address	0FH / W							
bit no	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—

Any write operation except interrupt routine to this address will stop the clock source of the CPU module , and any

interrupt call will restart the CPU clock source.

SECTION 4.2 CPU CLOCK SOURCE (Φ)

CKCTL (System Clock Control register) **:** reset value 0x00

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Address	2FH / R_W							
bit no	7	6	5	4	3	2	1	0
	PLL4	PLL3	PLL2	PLL1	PLL0	CK2	CK1	CK0

Where the **CKCTL** register defines the clock source of the 6502 CPU module

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CPU clock sources selection (Φ)

CK2	CK1	CK0	CPU clock source (Φ)
0	0	0	f_{XT}(76.8K)
0	0	1	f_{XT} / 2 (38.4K)
0	1	0	f_{XT} * 2 (153.6K)
0	1	1	f_{XT} * 4 (307.2K)
1	0	0	f_M (up to 2M)

Before you switch CPU Clock source to f_M, you must set PLL0 ~ 4 first. You can select PLL output frequency by following table. User can choose Ring OSC by select PLL4 ~ PLL0 equal to 0. And other value set to PLL4 ~ PLL0 will work with PLL.

PLL output clock table

PLL4	PLL3	PLL2	PLL1	PLL0	Hz
0	0	0	0	0	RingOSC
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	
		.			
1	1	1	1	1	

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1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

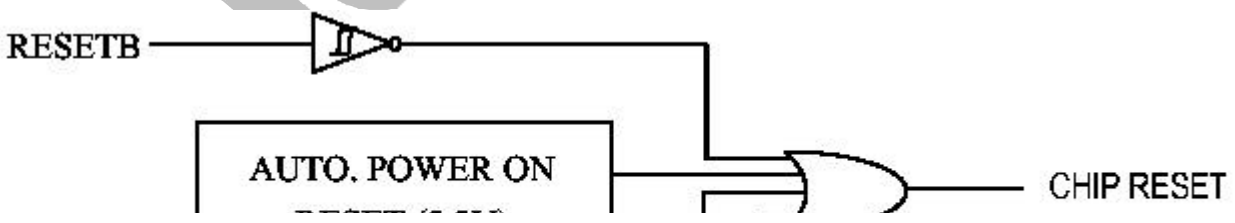
SECTON 4.3 CHIP RESET

The CPU module can be reset from four sources, namely the external RESETB pin, the automatic 2.2 voltage power on
reset module, the watchdog timer reset and the 2.0V low power reset.

The RESETB pin is the only external reset source, and it is connected with a Schmidt trigger input gate to improve the noise figure by the Schmidt trigger. Whenever the RESETB pin is pulled to low, the reset operation is active until this pin is changed to high.

The automatic power on reset module is an internal 2.2V voltage detector module, and it generates a power on reset pulse when the power is under the voltage threshold value. The watchdog timer reset is generated when the watchdog time threshold value is reached. The programming and the function of watchdog timer are introduced on the next section. The low power reset will automatically detect VDD. When VDD is under 2.0V, it will generate reset signal to chip reset.
It normally works with 30℃.

CHIP RESET SOURCE DIAGRAM



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SECTION 4.4 WATCHDOG TIMER

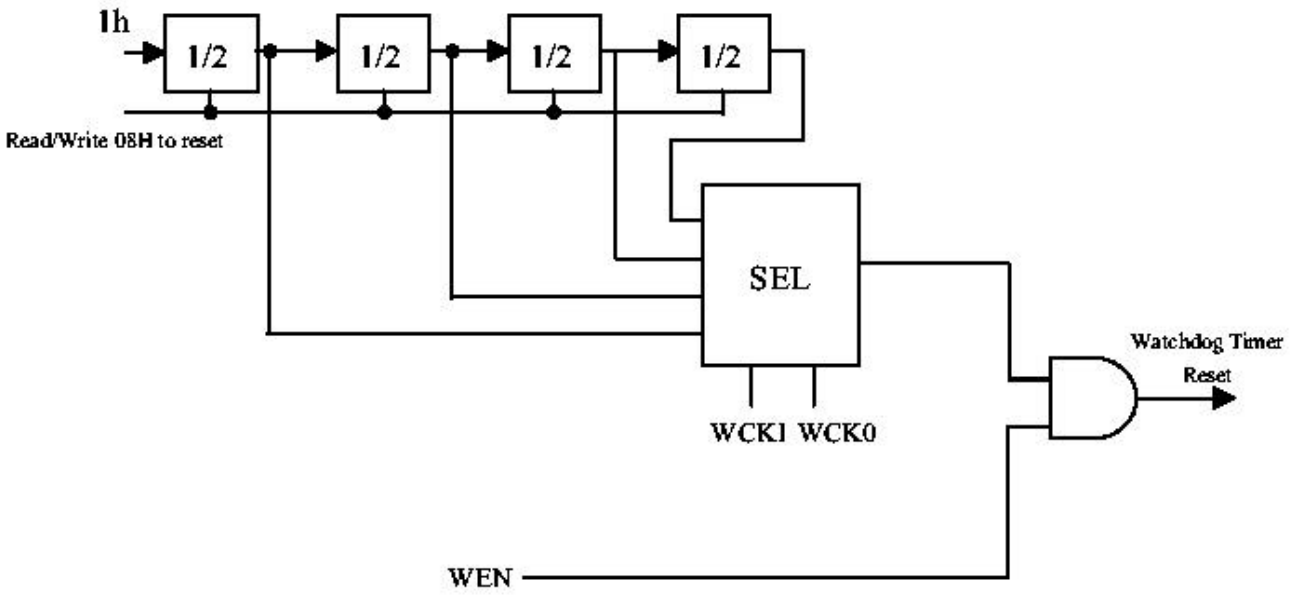
The watchdog timer is controlled by the **WEN**-bit of the **WDTCTL** register, and its clock source is from f_{WTCK} (the watchdog timer clock). Frequencies of this clock are defined by the **WCK1** and **WCK0** of **WDTCTL** register. Whenever the CPU accesses the **WDTCTL** register, the watchdog timer / counter will be reset to zero.

WDTCTL (Watchdog Timer Control register) **:** reset value 0x00

Address	08H / R_W							
bit no	7	6	5	4	3	2	1	0
	WEN	—	—	—	—	—	WCK1	WCK0

WCK1	WCK0	Watchdog timer active cycle
0	0	1 second
0	1	2 second
1	0	4 second

1	1	8 second



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SECTON 4.5 TIMER MODULE (PTIMER 0 / 1 , TIME BASE , RTC 0 / 1)

There are 5 timer modules in WT5082M, namely ptimer 0, ptimer1, time base timer and the real time clock 0/1 (RTC).

The **PTIMER 0** and **1** generate the IRQ interrupt to CPU when the timer is reloaded after the counting value reaches zero.

User programming the preload timer values into the **PTIME0** and **PTIME1** registers, and then enable these timer modules. The clock source of these two timers is selected from PTS11, PTS10, PTS01 and PTS00 of **PT0CTL** or **PT1CTL** register. Both two timers also can serve as the counter function, and the counter value can be obtained from the **TIMER0** and the **TIMER1** registers.

PT0CTL (PORT TIMER 0 CONTROL register) **:** reset value 0x00

Address	09H / R_W							
bit no	7	6	5	4	3	2	1	0
	EPT0	—	PT0S	OPT0	—	—	PTS01	PTS00

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PTIME0 (PORT TIMER 0 PRELOAD DATA) **:** reset value 0x00

Address	0AH / W							
bit no	7	6	5	4	3	2	1	0
	PT07	PT06	PT05	PT04	PT03	PT02	PT01	PT00

TIMER0 (PORT TIMER 0 COUNTER VALUE) **:** reset value 0x00

Address	0BH / R							
bit no	7	6	5	4	3	2	1	0
	T07	T06	T05	T04	T03	T02	T01	T00

TIMER0 (PORT TIMER 0 COUNTER VALUE) **:** reset value 0x00

Address	0CH / R_W							
bit no	7	6	5	4	3	2	1	0
	EPT1	—	PT1S	OPT1	—	—	PTS11	PTS10

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PTIME1 (PORT TIMER 1 PRELOAD DATA) **:** reset value 0x00

Address	0DH / R							
bit no	7	6	5	4	3	2	1	0
	PT17	PT16	PT15	PT14	PT13	PT12	PT11	PT10

TIMER1 (PORT TIMER 1 COUNTER VALUE) **:** reset value 0x00

Address	0EH / R							
bit no	7	6	5	4	3	2	1	0
	T17	T16	T15	T14	T13	T12	T11	T10

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The **PTOCTL** and **PT1CTL** registers control the port timer 0 and timer 1 for enabling or not. The **PTS11, PTS10, PTS01, PTS00** data bits of **PT0CTL** and **PT1CTL** registers define the clock source of the PTIME0 and PTIME1 clock counter. The **PT0S, PT1S** registers define the output waveform is normal or inverse.

EPT1	EPT0	Function
1	X	Enable Port Timer 1 (PTIME 1)
0	X	Disable Port Timer 1 (PTIME 1)
X	1	Enable Port Timer 0 (PTIME 0)
X	0	Disable Port Timer 0 (PTIME 0)

When Disable Ptimer.0 and Ptimer.1, It will output High

PT1S	PT0S	Function
1	X	Inverse Output Waveform (PTIME1)
0	X	Normal Output Waveform (PTIME1)
X	1	Inverse Output Waveform (PTIME0)
X	0	Normal Output Waveform (PTIME0)

OPT1	OPT0	Function
1	X	Enable P03 output with Ptimer1
0	X	Disable P03 output with Ptimer1
X	1	Enable P02 output with Ptimer0
X	0	Disable P02 output with Ptimer0

PTS01	PTS00	PTIME0 clock source (when fp = 32.768khz & f_{XT} = 76.8khz)
0	0	f_{XT} (76.8k)
0	1	f_{XT} * 2 (153.6k)
1	0	f_{PTIME1} (clock from PTIME1)

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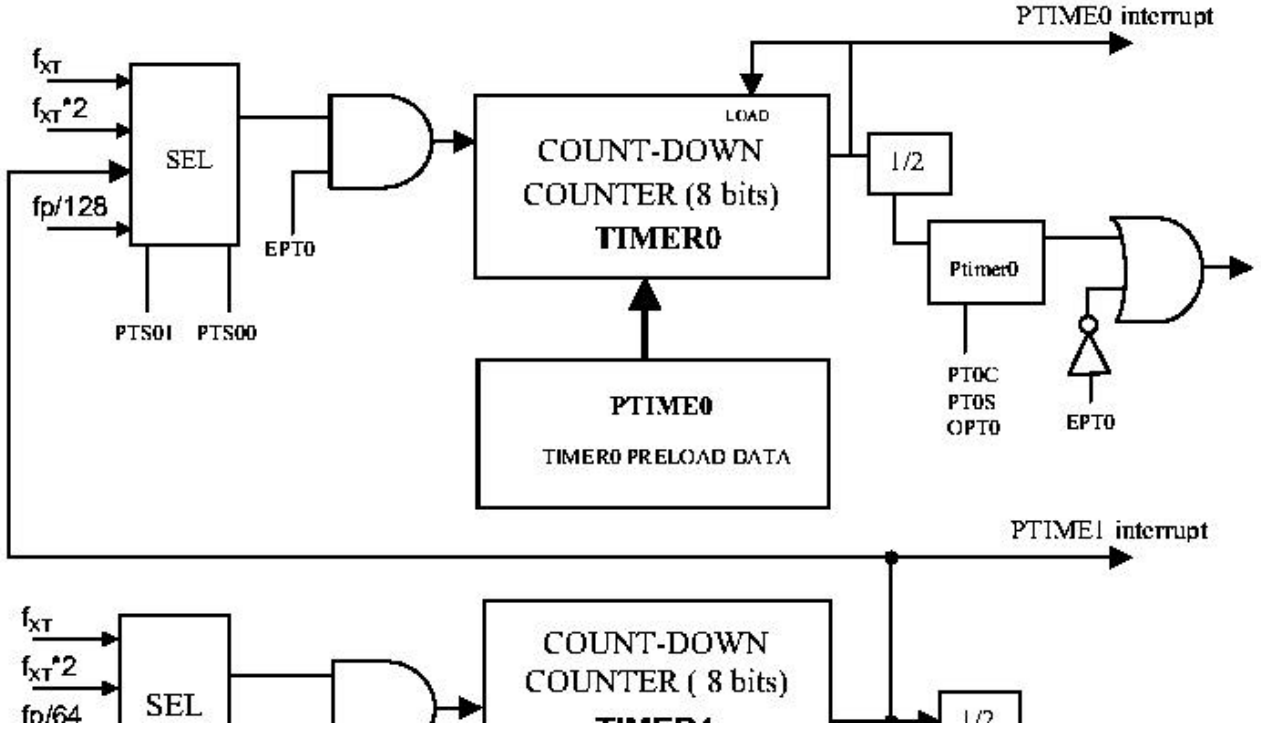
1	1	Fp / 2^7 (256hz)

PTS11	PTS10	PTIME1 clock source (when fp = 32.768khz & f_{XT} = 76.8khz)
0	0	f_{XT} (76.8k)
0	1	f_{XT} * 2 (307.2k)
1	0	fp / 2^6 (512hz)
1	1	fp / 2^7 (256hz)



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The Time base timer , RTC timer 0, and the RTC timer 1 are controlled by the **BTCTL** and the **RTCCTL** registers. The **EBT** of **BTCTL** enables the Time base timer and the **BTS1** and **BTS0** bits define the clock source of the time base timer. While the reload timer value is given at the **TIMERB** register, the counter value of the time base timer can be obtained from the **BTIME** register. The **RT11** and **RT10** bits of the **RTCCTL** register define the RTC1 interrupt clock source, and the **RT01** and **RT00** bits define the RTC0 interrupt source.

For convenience sake, we also provide **Hour, Minute,** and **Second** register to display time. User can program **Hour, Minute,** and **Second.** We suggest that user write " 0 " to the " SET " bit of the Hour register before programming. The RTC time is counting unless the " SET " bit is " 1 ". And there is an IRQ interrupt per minute to cpu in order to refresh Date, Month, and
Year in system application. See more detail in Section4.6.

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BTCTL (Time base timer control register) **:** reset value 0x00

Address	10H / R_W							
bit no	7	6	5	4	3	2	1	0
	EBT	—	—	—	—	—	BTS1	BTS0

BTIME (Time base timer preload data) **:** reset value 0x00

Address	11H / W							
bit no	7	6	5	4	3	2	1	0
	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0

TIMERB (Time base counter value) **:** reset value 0x00

Address	12H / R							
bit no	7	6	5	4	3	2	1	0
	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

RTCCTL (RTC timer control) **:** reset value 0x00

Address	13H / R_W							
bit no	7	6	5	4	3	2	1	0
	—	—	RT11	RT10	—	—	RT01	RT00

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EBT	BTS1	BTS0	Function / Clock source
0	—	—	Time base timer is disable
1	X	X	Time base timer is enable
X	0	0	fp / 2^5 (1024hz)
X	0	1	fp / 2^7 (256hz)
X	1	0	fp / 2^9 (64hz)

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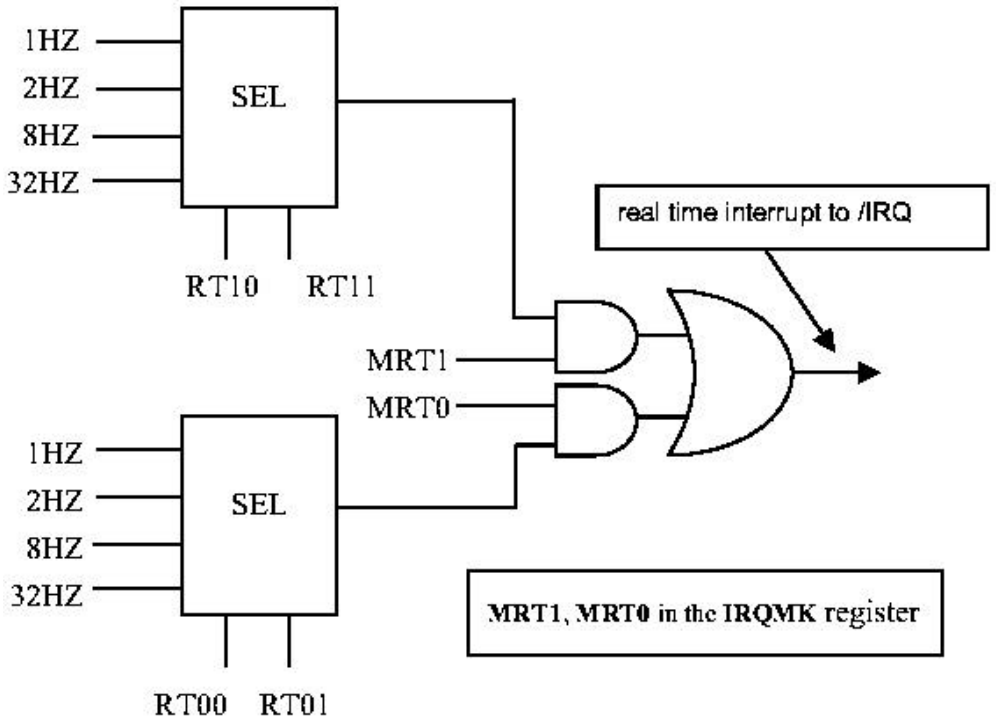
X	1	1	fp / 2^{11} (16hz)

RT11 / RT01	RT10 / RT00	Clock source
0	0	1hz
0	1	2hz
1	0	8hz
1	1	32hz



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Hour (RTC Hour register) **:** reset value 0x00

Address	14H / R_W							
bit no	7	6	5	4	3	2	1	0
	SET	—	—	H4	H3	H2	H1	H0

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Minute (RTC Minute register) **:** reset value 0x00

Address	15H / R_W							
bit no	7	6	5	4	3	2	1	0
	—	—	M5	M4	M3	M2	M1	M0

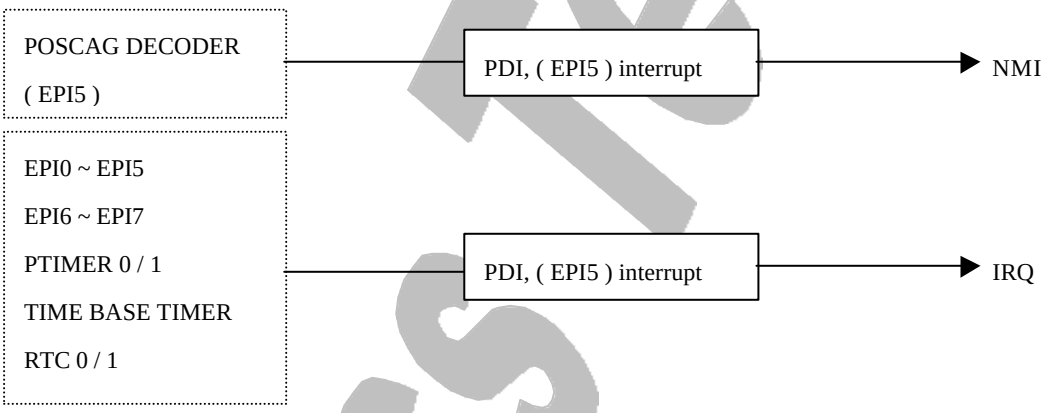
Second (RTC Second register) **:** reset value 0x00

Address	16H / R_W							
bit no	7	6	5	4	3	2	1	0
	—	—	S5	S4	S3	S2	S1	S0

SECTION 4.6 INTERRUPT SOURCE

The NMI interrupt source is connected with P_DECODER module, and the IRQ interrupt source is connected with the other timer & external interrupt input.

SOURCE of CPU / NMI and / IRQ DIAGRAM



NMI & IRQ Interrupt vector address

Vector Address	Interrupt Source
FFFAH , FFFBH	NMI interrupt

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FFFCH , FFFDH	Reset
FFFEH , FFFFH	IRQ

Interrupt mask registers :

IRQMK (IRQ interrupt mask register) **:** reset value 0x00

Address	17H / R_W							
bit no	7	6	5	4	3	2	1	0
	—	MRTC	MSIO	MRT1	MRT0	MBT	MPT1	MPT0

EPIMK (EPI interrupt mask register) **:** reset value 0x00

Address	19H / R_W							
bit no	7	6	5	4	3	2	1	0
	EEPI7	EEPI6	EEPI5	EEPI4	EEPI3	EEPI2	EEPI1	EEPI0

PDIMK (P-decoder Interrupt Mask register) **:** reset value 0x00

Address	1CH / R_W							
bit no	7	6	5	4	3	2	1	0
	EPDI7	EPDI6	EPDI5	EPDI4	EPDI3	EPDI2	EPDI1	EPDI0

(NOTE) PDECODER interrupt connect with the NMI interrupt of CPU

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Interrupt status registers :

IRQSR (IRQ interrupt status register) **:** reset value 0x00, reset after read

Address	18H / R

bit no	7	6	5	4	3	2	1	0
	FEPI	FRTC	FSIO	FRT1	FRT0	FBT	FPT1	FPT0

(NOTE) Any read operation to **IRQSR** will clear all **IRQSR** data bits (except FEPI).

FEPI will be reset when **EPISR** is cleared as zero.

EPISR (EPI interrupt status register) **:** reset value 0x00, reset after read

Address	1AH / R							
bit no	7	6	5	4	3	2	1	0
	EPI7	EPI6	EPI5	EPI4	EPI3	EPI2	EPI1	EPI0

(NOTE) Any read operation to **EPISR** will clear all EPISR data bits.

And EPI5 is also connect to NMI when EPDI7 enable and EEPI5 disable

PDISR (P-Decoder interrupt status register) **:** reset value 0x00, reset after read

Address	1DH / R							
bit no	7	6	5	4	3	2	1	0
	PDI7	PDI6	PDI5	PDI4	PDI3	PDI2	PDI1	PDI0

(NOTE) Any read operation to **PDISR** will clear PDI0 – PDI7

INTERRUPT DEFINITION :

IRQ Interrupt (PTIMER 0/1, Time Base timer, EPI, RTC 0/1, Per Minute)

The CPU IRQ interrupt is generated by the EPI input (External Port Interrupt, can be used as key wakeup interrupt), time base timer, port timer 0/1, and the RTC clock interrupt.

The P10-PI7 pins service two basic functions: the External Port Interrupt (EPI) input pins and the general-purpose input pins. **EPI.4** is default used for ALM and it will automatically detect battery voltage when RE active and **EPI.5** is also connect to

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NMI interrupt input when EEPI5 diable and EPDI7 enable. The other EPI function is enabled and a falling edge is detected at one of the enabled EPI pin input, the **EPIx**-bit in the **EPISR** register is set and if the

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EEPIx-bit of **EPIMK** register is enabled, one IRQ interrupt is generated to 6502.

Each EPI input pin can be enabled or disabled by the corresponding **EEPIx**-bit in the **EPIMK** register, and the usage of the EPI function does not affect the input function of port P 1, user can get the EPI pin status from the **EPISR** data register.

IRQSR (IRQ interrupt status register) , clear after read

FEPI	FRTC	FSIIO	FRT1	FRT0	FBT	FPT1	FPT0	Interrupt status
X	X	X	X	X	X	X	**1**	Ptimer 0 interrupt
X	X	X	X	X	X	**1**	X	Ptime 1 interrupt
X	X	X	X	X	**1**	X	X	Time base timer interrupt
X	X	X	X	**1**	X	X	X	PTC 0 interrupt
X	X	X	**1**	X	X	X	X	RTC 1 interrupt
X	X	**1**	X	X	X	X	X	There are SIO interrupt
X	**1**	X	X	X	X	X	X	RTC rer Minute interrupt
1	X	X	X	X	X	X	X	There are EPI interrupt

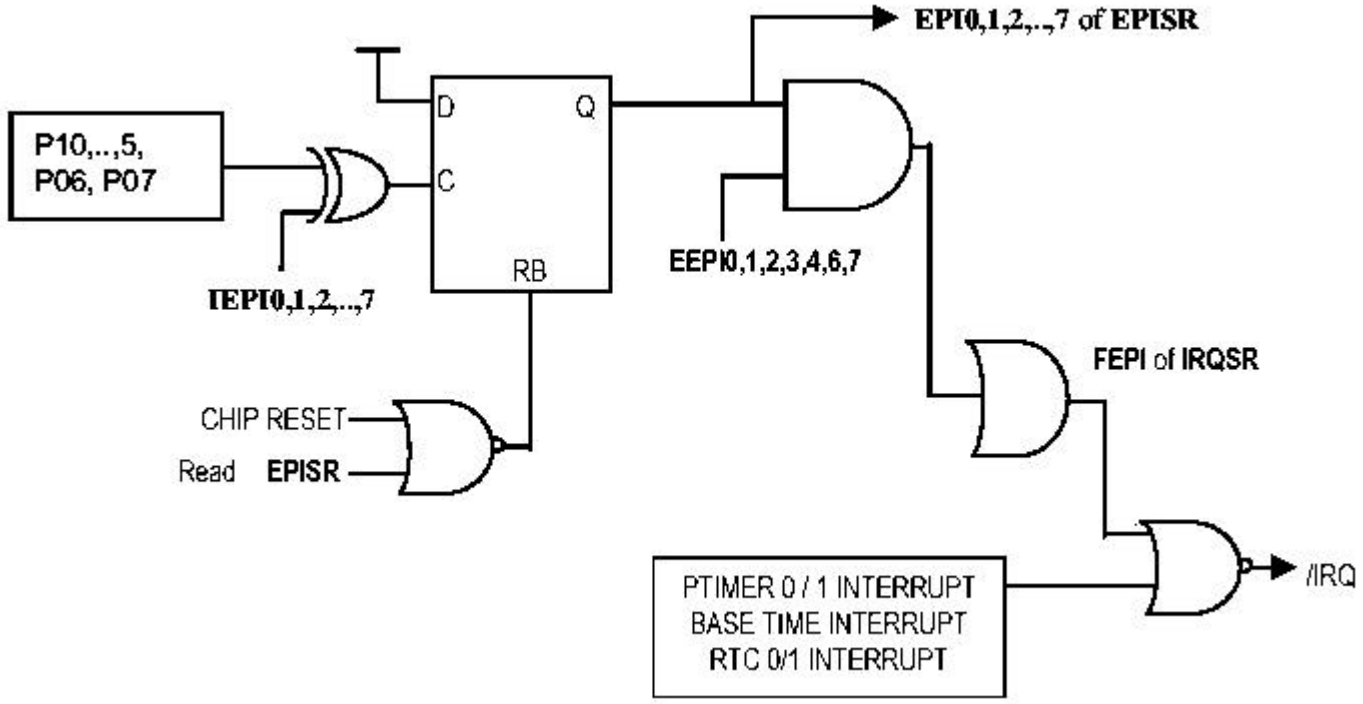
(note **:** when FEPI is set , ref to the EPISR to get the status of EPI)

IRQMK (IRQ interrupt mask register) , status

MRTC	MSIO	MRT1	MRT0	MBT	MPT1	MPT0	Interrupt status
X	X	X	X	X	X	**1**	Enable Ptimer 0 interrupt
X	X	X	X	X	**1**	X	Enable Ptimer 1 interrupt
X	X	X	X	**1**	X	X	Enable Time base timer interrupt
X	X	X	**1**	X	X	X	Enable RTC 0 interrupt
X	X	**1**	X	X	X	X	Enable RTC 1 interrupt
X	**1**	X	X	X	X	X	Enable SIO interrupt
1	X	X	X	X	X	X	Enable RTC / min interrupt

(note **:** the interrupt mask of EPI is defined at the EPIMK register)

EPI (External Port Interrupt and RTC Interrupt)



The **EPIMK** register controls the external port interrupt function is acted or not. Set 0 to the **EPIEx** bit of **EPIMK** register disables the EPI function.

The **IEPI** register can invert the input EPIx signal value, when the **IEPIx** bit is set as 0, the rising edge of the P1x / EPIx pin will generates an EPI interrupt. In the other case, the **IEPIx** bit is set as 1, the EPI interrupt is generated when there is a falling edge change of the P1x / EPIx pin input. Becarefully EPI.5 is also connect with NMI interrupt input when EEPI5 disable and EPDI7 enable.

EPIMK (EPI interrupt Mask register) **:** reset value 0x00

Address	19H / R_W							
bit no	7	6	5	4	3	2	1	0
	EEPI7	EEPI6	EEPI5	EEPI4	EEPI3	EEPI2	EEPI1	EEPI0

EEPI7 – EEPI0 (External Port Interrupt Enable)

EEPIx	P1 x / EP x (External Port Interrupt) pin
0	Disable
1	Enable

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IEPI (Interrupt EPI signal register) **:** reset value 0x00

Address	1BH / R_W							
bit no	7	6	5	4	3	2	1	0
	IEPI7	IEPI6	IEPI5	IEEPI4	IEPI3	IEPI2	IEPI1	IEPI0

IEPI7 – IEPI0 (Invert EPI input, only for Port P1)

IEPIx	P1x active EPI function clock edge
0	Normal (rising edge active)
1	Invert (falling edge active)

EPISR (EPI status register) **:** reset value 0x00, reset after read

Address	1AH / R							
bit no	7	6	5	4	3	2	1	0
	EPI7	EPI6	EPI5	EEPI4	EPI3	EPI2	EPI1	EPI0

IEPI7 – IEPI0 (Invert EPI input, only for Port P1)

IEPIx	P1x active EPI function clock edge
0	Normal (rising edge active)
1	Invert (falling edge active)

(Note : EPI5 is connect with NMI interrupt when EEPI5 disable and EPDI7 enable.

And EPI4 is work with batter low detect, it will automatically detect ALM when RE active)

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P-DECODER Interrupt (PDI)

The / NMI interrupt is exclusively used to service the POCSAG code decoder module (PDI interrupt / P-DECODER Interrupt), and the interrupt is generated when there is any status change of POCSAG code decoder such as receiver address, message and out of range indicator or DMA buffer overflow. The interrupt status can be obtained from the **PDISR** register, and the P-DECODER based on the internal status of decoder updates this register then interrupts the CPU module when there is any status changed. This **PDISR** register is a read only data register, and when there is any change of the **PDISR** register, the **PDIMK** register enables or disables the interrupt operation to the CPU module. The EPDMA-bit of the **PDCTL** register enables the P-decoder with the CPU interface mode into the DMA mode, for more details information please refer to the " POCSAG CODE DECODER " section.

PDISR (P-DECODER & EPI Interrupt) status

PDI7	PDI6	PDI5	PDI4	PDI3	PDI2	PDI1	PDI0	Interrupt status of P-DECODER
X	X	X	X	X	X	X	**1**	Address ID matched
X	X	X	X	X	X	**1**	X	End of message codeword receive
X	X	X	X	X	**1**	X	X	Over Range
X	X	X	X	**1**	X	X	X	Synchronize with POSCAG code
X	X	X	**1**	X	X	X	X	Send message codeword data
X	X	**1**	X	X	X	X	X	Incoming POCSAG in SC frame
X	**1**	X	X	X	X	X	X	DMA Buffer Overflow
1	X	X	X	X	X	X	X	External interrupt form Port15

PDIMK (P-DECODER Interrupt Mask register)

EPDI7	EPDI6	EPDI5	EPDI4	EPDI3	EPDI2	EPDI1	EPDI0	Interrupt status of P-DECODER
X	X	X	X	X	X	X	**1**	Enable PDI0 interrupt
X	X	X	X	X	X	**1**	X	Enable PDI1 interrupt
X	X	X	X	X	**1**	X	X	Enable PDI2 interrupt
X	X	X	X	**1**	X	X	X	Enable PDI3 interrupt
X	X	X	**1**	X	X	X	X	Enable PDI4 interrupt
X	X	**1**	X	X	X	X	X	Enable PDI5 interrupt
X	**1**	X	X	X	X	X	X	Enable PDI6 interrupt
1	X	X	X	X	X	X	X	Enable PDI7 interrupt

SECTION 5. POCSAG CODE DECODER

The POCSAG code decoder (P-DECODER) module is fully compatible with the CCIR Radio Paging Code Number 1, it can support 512 bps, 1200bps and 2400bps data speed base on one single crystal. The WT5082 architecture allows for the numeric, alphanumeric, and tone only pager application.

SECTION 5.1 P DECODER FEATURE

- Fully compatible with CCIR Radio-paging Code No. 1 (POCSAG standard).
- Single crystal support 512, 1200 and 2400 baud rate (76.SkHz crystal)
- Support 6 RIC addresses and 6 independent frame numbers.
- Support partial address match facility for address F (up to 260k addresses are provided).
- 3 RF power saving control lines (PLL, quick charge, and enable).
- Support alphanumeric, numeric or tone only pages application.
- Build in data filter (16-times over-sampling) and data bit clock recovery.
- Interrupt 6502 CPU when there are any status change
- Communicate with 6502 CPU base on memory I/O map method.
- Provide 2-bit random error correction and 3 bits random error detection in all code words.
- Synchronize / over range indication.
- DMA or interrupt mode to send the received message data to 6502 CPU.

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PDCONFx (P-DECODER configuration registers) **:** reset value 0x00

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ADDR	NAME	Read Write	Bit number							
			7	6	5	4	3	2	1	0
0030H	**PDCONF0**	R / W	A00	A01	A02	A03	A04	A05	A06	A07
0031H	**PDCONF1**	R / W	A08	A09	A10	A11	A12	A13	A14	A15
0032H	**PDCONF2**	R / W	A16	A17	FA0	FA1	FA2	FCA1	FCA0	DSA
0033H	**PDCONF3**	R / W	B00	B01	B02	B03	B04	B05	B06	B07
0034H	**PDCONF4**	R / W	B08	B09	B10	B11	B12	B13	B14	B15
0035H	**PDCONF5**	R / W	B16	B17	FB0	FB1	FB2	FCB1	FCB0	DSB
0036H	**PDCONF6**	R / W	C00	C01	C02	C03	C04	C05	C06	C07
0037H	**PDCONF7**	R / W	C08	C09	C10	C11	C12	C13	C14	C15
0038H	**PDCONF8**	R / W	C16	C17	FC0	FC1	FC2	FCC1	FCC0	DSC
0039H	**PDCONF9**	R / W	D00	D01	D02	D03	D04	D05	D06	D07
003AH	**PDCONF10**	R / W	D08	D09	D10	D11	D12	D13	D14	D15
003BH	**PDCONF11**	R / W	D16	D17	FD0	FD1	FD2	FCD1	FCD0	DSD
003CH	**PDCONF12**	R / W	E00	E01	E02	E03	E04	E05	E06	E07
003DH	**PDCONF13**	R / W	E08	E09	E10	E11	E12	E13	E14	E15
003EH	**PDCONF14**	R / W	E16	E17	FE0			FCE1	FCE0	DSE
003FH	**PDCONF15**	R / W	F00	F01	F02	F03	F04	F05	F06	F07
0040H	**PDCONF16**	R / W	F08	F09	F10	F11	F12	F13	F14	F15
0041H	**PDCONF17**	R / W	F16	F17	FF0	FF1	FF2	FCF1	FCF0	DSF
0042H	**PDCONF18**	R / W	MF0	MF1	MF2	MF3	MF4	MF5	MF6	MF7
0043H	**PDCONF19**	R / W	MF8	MF9	MF10	MF11	MF12	MF13	MF14	MF15
0044H	**PDCONF20**	R / W	MF16	MF17	X00	X01	X02	X03	X04	X05
0045H	**PDCONF21**	R / W	X06	X07	X08	0	0	X11	X12	X13
0046H	**PDCONF22**	R / W	X14	X15	X16	X17	X18	X19	X20	X21
0047H	**PDCONF23**	R / W	X22	X23	X24	X25	X26	X27	X28	X29
0048H	**PDCONF24**	R / W	X30	X31	X32	X33	X34	1	1	1
0049H	**PDCONF25**	R / W	X38	X39	X40	X41	X42	X43	X44	X45
004AH	**PDCONF26**	R / W	X46	X47	X48	X49	X50	X51	X52	X53

SECTION 5.2 RELATIVE REGISTERS

PDCTL (P-DECODER control register) **:** reset value 0x00

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Address	20H / R_W							
bit no	7	6	5	4	3	2	1	0
	OverRange	LostSync	ErrorFlag	0	EPDMA	REON	PDEOM	PDON

EPDMA	REON	PDEOM	PDON	Ennable function
X	X	X	**1**	Enable P-Decoder
X	X	**1**	X	Enable P-Decoder EOM mode
X	**1**	X	X	Force RE pin ON
1	X	X	X	Enable P-Decoder DMA mode

The following 3 bits is read only and will reset to 0 when address match :

Function bit status	0	1
OverRange	In POCSAG sync status	Lost sync with POCSAG
LostSync (OverRange = 1)	Never Sync with S.C.	Ever Sync with S.C.
ErrorFlag (X34 = 1)	No error	CW have error

PS. LostSync will reset after reading

PDIMK (P-DECODER interrupt mask register) **:** reset value 0x00

Address	1CH / R_W							
bit no	7	6	5	4	3	2	1	0
PDIMK	EPDI7	EPDI6	EPDI5	EPDI4	EPDI3	EPDI2	EPDI1	EPDI0

PDISR (P-DECODER interrupt status register) **:** reset value 0x00, reset after read

Address	1DH / R							
bit no	7	6	5	4	3	2	1	0
PDISR	PDI7	PDI6	PDI5	PDI4	PDI3	PDI2	PDI1	PDI0

PDDR (P-DECODER receive data register) **:** reset value 0x00

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Address	21H / R							
bit no	7	6	5	4	3	2	1	0
PDDR	PDD7	PDD6	PDD5	PDD4	PDD3	PDD2	PDD1	PDD0

PDDRp (PDDR DMA mode address pointer / low byte) **:** reset value 0x00

Address	22H / R							
bit no	7	6	5	4	3	2	1	0
PDDRp	PDA7	PDA6	PDA5	PDA4	PDA3	PDA2	PDA1	PDA0

PDDRpH (PDDR DMA mode address pointer / high byte / Base address) **:** reset value 0x00

Address	23H / R_W							
bit no	7	6	5	4	3	2	1	0
PDDRpH	—	—	PDBA3	PDBA2	PDBA1	PDBA0	PDA9	PDA8

Note **:** PDA8, PDA9 is read only , others are R/W.

MPDDRp (PDDRp mask register) **:** reset value 0x00

Address	24H / R_W							
bit no	7	6	5	4	3	2	1	0
MPDDRp	MCL	ADCL	—	—	MPDA9	MPDA8	MPDA7	MPDA6

PDEOM (P-DECODER EOM (End of Message) mark register) **:** reset value 0x00

Address	25H / R_W							
bit no	7	6	5	4	3	2	1	0
PDEOM	EOM7	EOM6	EOM5	EOM4	EOM3	EOM2	EOM1	EOM0

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ABSOLUTE MAXIMUM RATINGS (VSS = 0 V)

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	VDD	-0.5 ~ +3.6	V
Input Voltage Range	Vin	-0.5 ~ VDD + 0.5	V
Operating Temperature	Tor	0 ~ +70	℃
Storage Temperature	Tstg	-50 ~ +150	℃

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POCSAG DECODER MODULE (P-DECODER)

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SECTION 5.3 CPU INTERFACE

The CPU module configures the P-DECODER by the **PDCONF0 ~ PDCONF26** registers, and enables or turn on the P-DECODER by the **PDON** bit of **PDCTL** register. When there is any status changed of the P-DECODER, the P-DECODER interrupts the CPU module and sets the interrupt flag bits in the **PDISR** register. The received POCSAG codeword data can be obtained from the **PDDR** registers.

After the P-DECODER is turned on, the RE1 and RE2 pins are acted as the RF power saving control output ports and the P-DEOCDER waits for the incoming POCSAG code signal from the RFDI input pin.

P-DECODER interrupts CPU

When the P-DECODER is turned on and enabled, the P-DECODER starts to receive the incoming POCSAG codeword data. If there is any status changed, the P-DECODER set the **PDIx** bits of **PDISR** register, and then interrupts the CPU module. Whenever any one of the RIC addresses, that set in the **PDCONFx** registers, are matched with the incoming POCSAG address codeword, the P-DECODER interrupts the CPU module and starts to send the received codeword data by the **PDDR** registers. The **PDIMK** register is used to control the P-decoder interrupt operation, either enable or disable.

PDISR (P-DECODER) status

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PDI7	PDI6	PDI5	PDI4	PDI3	PDI2	PDI1	PDI0	Interrupt status of P-DECODER
X	X	X	X	X	X	X	**1**	Address ID matched
X	X	X	X	X	X	**1**	X	End of message codeword receive
X	X	X	X	X	**1**	X	X	Over Range
X	X	X	X	**1**	X	X	X	Synchronize with POSCAG code
X	X	X	**1**	X	X	X	X	Send message codeword data
X	X	**1**	X	X	X	X	X	Incoming POCSAG in SC frame
X	**1**	X	X	X	X	X	X	DMA Buffer Overflow
1	X	X	X	X	X	X	X	Battery removed

PDIMK (P-DECODER Interrupt Mask register)

EPDI7	EPDI6	EPDI5	EPDI4	EPDI3	EPDI2	EPDI1	EPDI0	Enable function
X	X	X	X	X	X	X	**1**	Enable PDI0 interrupt
X	X	X	X	X	X	**1**	X	Enable PDI1 interrupt
X	X	X	X	X	**1**	X	X	Enable PDI2 interrupt
X	X	X	X	**1**	X	X	X	Enable PDI3 interrupt
X	X	X	**1**	X	X	X	X	Enable PDI4 interrupt
X	X	**1**	X	X	X	X	X	Enable PDI5 interrupt
X	**1**	X	X	X	X	X	X	Enable PDI6 interrupt
1	X	X	X	X	X	X	X	Enable PDI7 interrupt

Data DMA mode of P-DECODER

The P-DECODER receives the incoming message codeword data of the matched RIC address, and transfers them to the CPU module by either interrupt mode or the DMA mode. In the interrupt mode,

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the CPU enables the PDDR active interrupt by setting the EPDI4 of the **PDISR** register. While CPU receives this interrupt, it can obtain the incoming message codeword data at the **PDDR** register. The **EPDMA** bit of the **PDCTL** register enables the P-DECODER data DMA mode. In this mode, the P-DECODER automatically transfers the incoming message codeword data into the data RAM module that addressed by the PDDR address pointer, which is read only and defined at the **PDDRp & PDDRpH** register. The PDDR address pointer register automatically increases by 1 after each PDDR data write operation. The 6502 CPU module can get the last data address pointer by accessing this register (**PDBAx & PDDRp & PDDRpH**). We use **MPDDRp** to descide one page size. **PDBAx** (x = 0-3) in **PDDRpH** to indicate which page is used. Before using DMA mode, set **PDBAx** to an available memory address. We strongly suggest that do not set **PDBAx** as "0000 " (zero page).

Page 0 PDBAx = 0000,

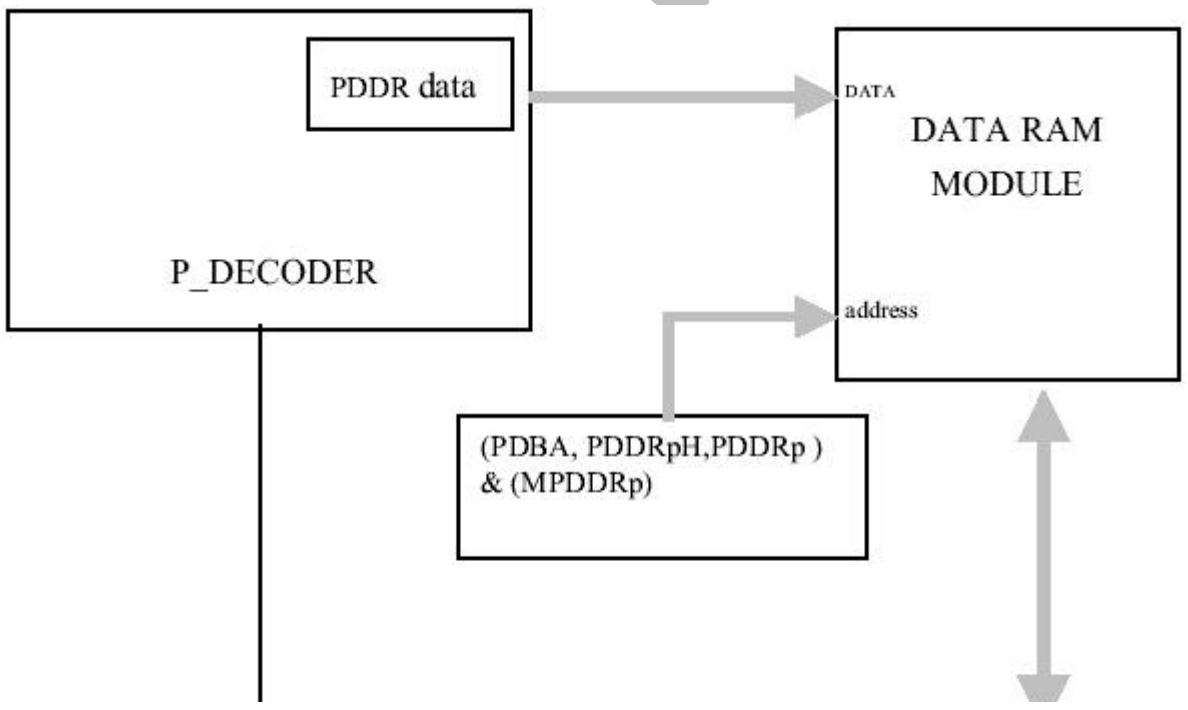
Page 1 PDBAx = 0001,

……

Page15 PDBAx = 1111,

PDDR address pointer = { PDBAx, PDA9, PDA8, **….** , PDA1, PDA0 }

P-DECODER data DMA mode



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In the P DECODER data DMA mode, the memory address is defined at the **PDDRp** and **PDDRpH** register, and it can define 14-bit memory address. The **MPDDRp** register can mask the address output of the **PDDRp** and **PDDRpH** register, and by using the **MPDDRp** register the updated memory area can be limited at one sub-area of memory. If **PDDRpH** is being mask, PDA9 ~ PDA6 can be written to change different address. For example, when the **MPPDRp** equals to 0x0FH, then PDA9 ~ PDA6 can be witten. The **PDDRpH** register is set as 0x04H, and **PDDRp** register is set as 0x80H then the DMA memory address will be limited at 0480H to 04BFH area. If **PDDRp** register is set as 0x40H then DMA memory address will limited at 0440H to 047FH area. If **MPPDRp** equals to 0x0CH, then only PDA9 and PDA8 can be written, PDA7 and PDA6 are read only. So if **PDDRpH** register is set as 0x04H, and **PDDRp** register can't be set then the DMA memory address will be limited at 0400H to 04FFH area. User can set the **MCL** bit of **MPDDRp** to clear **PDDRp** and **PDDRpH** after each cpu reading, or set the **ADCL** bit of **MDDRp** to clear automatically **PDDRp** and **PDDRpH** when P_decoder address is matched.

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MPDAx	Data memory address bus
1	0 (PDAx is read / write)
0	Enable PDAx (PDAx is read only)

(note**:** X is between 9 ~ 6)

MPDDRp	**Data memory address bus**
0x0F	**64**
0x0E	**128**
0x0C	**256**
0x08	**512**
0x00	**1024**

RECEIVED MESSAGE DATA FORMAT (PDDR REGISTER)

When the incoming POCSAG address codeword matches one of the internal RICs, the P-DECODER interrupts the CPU module and stores the incoming codeword data into the **PDDR** register. There are 3 different formats in the **PDDR** register data words, the start word, the message word and the EOM (end of message) mark byte. The start word contains the matched address ID, address codeword data and the FC code. The message word contains the received message codeword data and error flag. The data format of message word can be the package data format or the direct shift format. The package data format can be 4 or 7 bits per byte, which is set by the **X00 — X07, X38 — X53** of **PDCONFx** register. The EOM mark byte is sent while end of the message codeword. The EOM mark byte is defined at

PDEOM register and is enabled when the **PDEOM** bit of **PDCTL** register is enabled.

Start Word (3 bytes)	Message Word (2 to 5 bytes) x N	EOM Mark Byte (note)

(note: EOM mark byte is enabled when the PDEOM of PDCTL register is set as 1)

* POCSAG Address codeword Format:

Bit 1	Bit2 …bit19	Bit20	Bit21	Bit22 …bit31	Bit32
0	A0, A1 … A17	FC0	FC1	CRC Code	Parity

(Start word Format):

Total 3 PDDR data byte

bit no	0	1	2	3	4	5	6	7
PDDR (1)	1	ID0	ID1	ID2	A0	A1	A2	A3
PDDR (2)	A4	A5	A6	A7	A8	A9	A10	A11
PDDR (3)	A12	A13	A14	A15	A16	A17	FC0	FC1

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Address ID Code Bits : (ID0, ID1, and ID2)

ID2	ID1	ID0	Address (RIC) Match
0	0	0	A
0	0	1	B

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0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F

(Message word format: Direct shift mode)

The **FCx0/FCxl** bit of **PDCONFx** register defines the message word whether is acted as the "direct shift" format or the "data package" format. While in the direct shift format, i.e., **FCx0/FCxl** equal to 1, the message word shifts out message codeword data as P-DECODER received and corrected them, and it hasn't any data package.

* POCSAG message codeword format

bit 1	Bit2 …bit21	Bit22 …bit31	Bit32
1	MA00 … MA19	CRC	Parity

Message word (3 PDDR data bytes)

Bit no	0	1	2	3	4	5	6	7
PDDR (1)	X	Error	0	0	MA00	MA01	MA02	MA03
PDDR (2)	MA04	MA05	MA06	MA07	MA08	MA09	MA10	MA11
PDDR (3)	MA12	MA13	MA14	MA15	MA16	MA17	MA18	MA19

(Message word format : Data packaging mode)

Each POCSAG message codeword contain 20 bits message code, the P-DECODER divides each 4 / 7 bits into some message bytes for shift out to microprocessor. User can define different package methods by using different FC code (FC code is given in POCSAG address codeword),

and each different address also can define different message codeword format.

* Message codeword format selection in different address

FCA 1 / FCB 1 / FCC 1 FCD 1 / FCE 1 / FCF 1	FCA 0 / FCB 0 / FCC 0 FCD 0 / FCE 0 / FCF 0	Data Package mode
0	0	Data package mode (Depend on FC)
0	1	4 bits data package method
1	0	7 bits data package method
1	1	Direct shift Mode

Note: Please comfirm the FCx0 equal FC0, and FCxl equal FC1

* Message Codeword data packaging method (define in X00 - X07, X38 - X53) While FCx0 and FCxl are equal with

0, the different address have different data package format, it depends on table.

Address	FC1 = 0 FC0 = 0	FC1 = 0 FC0 = 1	FC1 = 1 FC0 = 0	FC1 = 1 FC0 = 1	Data Package Method
Address	X00	X01	X02	X03	
B	X04	X05	X06	X07	
C	X38	X39	X40	X41	
D	X42	X43	X44	X45	
E	X46	X47	X48	X49	
F	X50	X51	X52	X53	
	0	0	0	0	4 bits
	1	1	1	1	7 bits

Example of Data Packaging Method: 7 bit and 4 bits packaging method

* POCSAG message codeword Format

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bit 1	Bit2 …bit21	Bit22 …bit31	Bit32
1	MA00 … MA19	CRC	Parity
1	MB00 … MB19	CRC	Parity

* 7 Bits Packaging Method Output

Message word 1 (2 PDDR data bytes)

Bit no	0	1	2	3	4	5	6	7
PDDR (1)	MA00	MA01	MA02	MA03	MA04	MA05	MA06	Error
PDDR (2)	MA07	MA08	MA09	MA10	MA11	MA12	MA13	Error

Message word 2 (3 PDDR data bytes)

Bit no	0	1	2	3	4	5	6	7
PDDR (1)	MA14	MA15	MA16	MA17	MA18	MA19	MB00	Error
PDDR (2)	MB01	MB02	MB03	MB04	MB05	MB06	MB07	Error
PDDR (3)	MB08	MB09	MB10	MB11	MB12	MB13	MB14	Error

* 4 Bits Packaging Method Output

Message word 1 (5 PDDR data bytes)

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Bit no	0	1	2	3	4	5	6	7
PDDR (1)	MA00	MA01	MA02	MA03	0	0	0	Error
PDDR (2)	MA04	MA05	MA06	MA07	0	0	0	Error
PDDR (3)	MA08	MA09	MA10	MA11	0	0	0	Error
PDDR (4)	MA12	MA13	MA14	MA15	0	0	0	Error
PDDR (5)	MA16	MA17	MA18	MA19	0	0	0	Error

Message word 2 (5 PDDR data bytes)

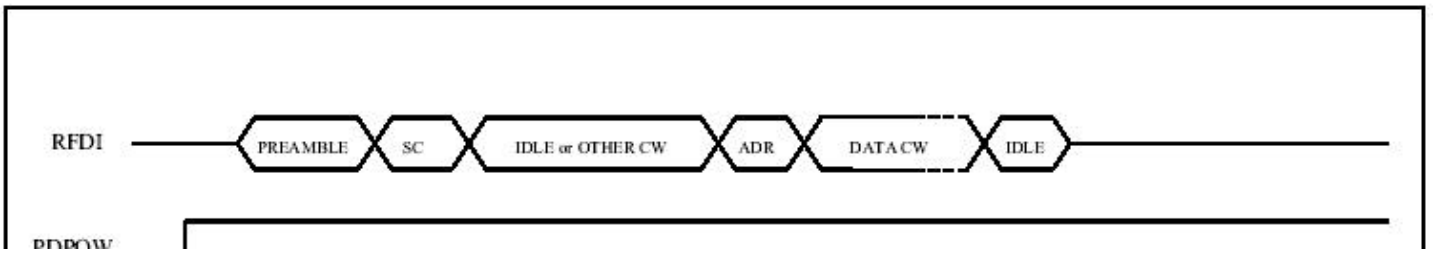
Bit no	0	1	2	3	4	5	6	7
PDDR (1)	MB00	MB01	MB02	MB03	0	0	0	Error
PDDR (2)	MB04	MB05	MB06	MB07	0	0	0	Error
PDDR (3)	MB08	MB09	MB10	MB11	0	0	0	Error
PDDR (4)	MB12	MB13	MB14	MB15	0	0	0	Error
PDDR (5)	MB16	MB17	MB18	MB19	0	0	0	Error

(EOM mark byte Format) :

Total 1 PDDR data byte

Bit no	7	6	5	4	3	2	1	0
	EOM7	EOM6	EOM5	EOM4	EOM3	EOM2	EOM1	EOM0

The **EOM** (End of Message) mark data format is defined at the **PDEOM** register, and this byte is sent out only when the **PDEOM** bit of **PDCTL** register is set as 1.



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SECTION 5.4 CONFIGURATION REGISTERS

There are total 27 configuration registers of the POCSAG code decoder, and the data bits consist of 6 RIC addresses, 6

address frame, 6 disable address ID flag, 18 address F mask bits, and 33 special function bits. The CPU module uses the

memory map method to program this registers, after the **PDON** bit of the **PDCTL** register is turned on that P-DECODER

depends on these data bits to start operation.

(NOTE) The P_DECODER c0nfigurati0n registers carl be accessed ONLY when the P_DECODER module is off.

(PDON=0)

Address ID Bits Definition

The P-DECODER supply 6 POCSAG RIC addresses and 6 user frames. Each frame number can be independently programmed, that is, six addresses IDs can be in a same frame location or not. User can disable any one of 6 RIC addresses by setting the **Disable address ID bits.**

* Address ID Bits

A00 – A17	Address A ID Bits
B00 – B17	Address B ID Bits
C00 – C17	Address C ID Bits
D00 – D17	Address D ID Bits
E00 – E17	Address E ID Bits
F00 – F17	Address F ID Bits

* Frame Number Bits

FA0 – FA2	Frame number of Address A
FB0 – FB2	Frame number of Address B
FC0 – FC2	Frame number of Address C
FD0 – FD2	Frame number of Address D

FE0 – FE2	Frame number of Address E
FF0 – FF2	Frame number of Address F

(Address Definition and POCSAG Code)

* POCSAG Address codeword Format:

Bit 1	Bit2 …bit19	Bit20	Bit21	Bit22 …bit31	Bit32
0	Address-Code	FC0	FC1	CRC Code	Parity

* The Relation between POCSAG Address-Code and the EEPROM Address-Code

POCSAG Code Bit number	2	3	4	5	6	…	19
PDCONFx address bit name	A00	A01	A02	A03	A04	…	A17
	B00	B01	B02	B03	B04	…	B17
	C00	C01	C02	C03	C04	…	C17
	D00	D01	D02	D03	D04	…	D17
	E00	E01	E02	E03	E04	…	E17
	F00	F01	F02	F03	F04	…	F17

* Frame Number definition

FA0 / FB0 / FC0 / FD0 / FE0 / FF0 /	FA1 / FB1 / FC1 / FD1 / FE1 / FF1 /	FA2 / FB2 / FC2 / FD2 / FE2 / FF2 /	Frame Number
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

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1	0	1	5
1	1	0	6
1	1	1	7

Disable Address ID Bits (DA / DSB / DSC / DSD / DSE / DSF)

User defines the any one of following bit to disable any address ID code.

* Disable Address ID Bits

DSA	1 Disable Address A ID Code 0 Enable
DSB	1 Disable Address B ID Code 0 Enable
DSC	1 Disable Address C ID Code 0 Enable
DSD	1 Disable Address D ID Code 0 Enable
DSE	1 Disable Address E ID Code 0 Enable
DSF	1 Disable Address F ID Code 0 Enable

Address F Mask Bits : Mask Address F RIC Pattern Match
(MF0 / MF1 / MF2 / MF3 / MF4 / MF5 / MF6 / MF7 / MF8 / MF9 / MF10 / MF11 / MF12 / MF13 / MF14 / MF15)

Normal each RIC pattern contains 18 bits, while the P-DECODER can match a sub-set of RIC in address F for a specific application.

Mask Bits	Address F RIC Code	
MF0	1 RIC Mask F0	0 RIC Mask F0
MF1	1 RIC Mask F1	0 RIC Mask F1
MF2	1 RIC Mask F2	0 RIC Mask F2
MF3	1 RIC Mask F3	0 RIC Mask F3

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MF4	1 RIC Mask F4	0 RIC Mask F4
MF5 ---- MF15	1 RIC Mask F5 / F6 / F7 / F8 / F9 / F10 / F11 / F12 / F13 / F14 / F15)	0 RIC Mask F5 / F6 / F7 / F8 / F9 / F10 / F11 / F12 / F13 / F14 / F15)
MF16	1 RIC Mask F16	0 RIC Mask F16
MF17	1 RIC Mask F17	0 RIC Mask F17

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Output Data Format Function selection (FCx1 / FCx0 , X00-07 and X38-53)

* Message codeword format selection in different address

FCA1 / FCB1 / FCC1 FCD1 / FCE1 / FCF1	FCA0 / FCB0 / FCC0 FCD0 / FCE0 / FCF0	Data Package mode
0	0	Data package mode (Depend on FC)
0	1	4 bits data package method
1	0	7 bits data package method
1	1	Direct shift Mode

* Message Codeword data packaging method (define in X00 – X07 , X38 – X53)

While FCx0 and FCx1 are equal with 0, the different address have different address have different data package

format, it depends on table

Address	FC1 = 0 FC0 = 0	FC1 = 0 FC0 = 1	FC1 = 1 FC0 = 0	FC1 = 1 FC0 = 1	Data Package Method
Address	X00	X01	X02	X03	
B	X04	X05	X06	X07	
C	X38	X39	X40	X41	
D	X42	X43	X44	X45	
E	X46	X47	X48	X49	
F	X50	X51	X52	X53	
	0	0	0	0	4 bits
	1	1	1	1	7 bits

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Message Error Flag Type Select (X08)

User uses this data bit to force the P-DECODER sends out message codeword data with bit 7 as " BCH can' t recover this codeword " or " BCH Algorithm ever correct this codeword ".

X08	Bit 7 of Message codeword Data Selection
0	BCH Algorithm can' t recover this codeword
1	BCH Algorithm ever correct this codeword

Disable Frame Number Match (X11)

Turn off the frame number match of RIC address. When the frame number match function is disabled, the P-DECODER always turns on the RF board after it synchronizes with POCSAG. It only matches the RIC addresses and it doesn' t care the frame number that defined in the **PDCONFx** registers.

X11	Frame Number Match
0	Normal
1	Disable Frame Number Match

Error Correction Mode Selection (X12)

The P-DECODER can correct 2 bits random error or 4 bits burst error per codeword, user can select one of these, as application need.

X12	Codeword error correction mode selection
0	2 Bit Random Error Correction Mode
1	4 Bit Burst Error Correction Mode

RE / RE1 / RE2 active state (X13)

X13	Active State

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0	**High**
1	**Low**

Select message codeword error correct method of address (X14)

X14	Error Correction Method
0	**2 bit random or 4 bits burst mode (X14)**
1	**1 bit error correct and 2 bits error detection**

RE1 active width (X15 / X16)

X15	X16	RE1 active width (per baud rate)
0	**0**	**1 Bit**
0	**1**	**4 Bit**
1	**0**	**RE Preactive Width – 1**
1	**1**	**Active on every sync. Codeword Cycle**

Reverse RFDI input (X 17)

X17	RF – DI data input
0	**Normal**
1	**Reverse Data Input**

Random error bits accept rate in preamble pattern (X18 / X19)

Define how many random bits error can be accepted in preamble pattern recognition within 32 bits.

X18	X19	Accept error bits each 32 bits
0	**0**	**4 (N ormal)**
0	**1**	**6**
1	**0**	**8**
1	**1**	**5**

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Baud rate selection option bits (X20 / X21)

X20	X21	Connected Crystal	Baud Rate
0	1	76.8k	512
1	0	76.8k	1200
1	1	76.8k	2400

Message codeword stop receive condition (X22)

X22	Stop Message Receive Condition
0	Continue Receive Message, don' t care error condition of message codeword or address codeword
1	Stop Receive Message when 2 Continue Message Codeword error or One Address Codeword error

RE pre-active width (X23 / X24 / X25 / X26 / X27)

X23	X24	X25	X26	X27	Pre-active width (per Baud Rate)
0	0	0	0	0	1
0	0	0	0	1	3
0	0	0	1	0	5
0	1	1	1	0	29
1	0	0	0	0	33
1	0	0	0	1	35
1	1	1	0	1	59
1	1	1	1	0	61

RE2 Preactive width (X28 / X29 / X30 / X31 / X32 / X33)

Pre-active time of RE2 output pin

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X28	X29	X30	X31	X32	X33	Bits
0	0	0	0	0	0	don' t use
0	0	0	0	0	1	2
0	0	0	0	1	0	4
0	0	1	1	1	1	30
0	1	0	0	0	0	32
0	1	0	0	0	1	34
1	0	1	1	1	1	94
1	1	0	0	0	0	96
1	1	0	0	0	1	98
1	1	1	1	1	1	126

Data Output Form (X34)

X34	Data Output Form
0	No operation with **PDDR**
1	Operation **PDDR** with follow description

When X32 = 1, data package in 4 bits, output data will become

	Original	After transfer
" 0 "	0x00	0x30
" 1 "	0x01	0x31
" 2 "	0x02	0x32
" 3 "	0x03	0x33
" 4 "	0x04	0x34
" 5 "	0x05	0x35
" 6 "	0x06	0x36

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“ 7 ”	0x07	0x37
“ 8 ”	0x08	0x38
“ 9 ”	0x09	0x39
“ A ”	0x0A	0x41
“ B ”	0x0B	0x42
“ C ”	0x0C	0x43
“ D ”	0x0D	0x44
“ E ”	0x0E	0x45
“ ”	0x0F	0x20

No matter data package is 7 bits or 4 bits , Register **PDDR** bit 7 equals error flag.

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SECTION 6. LCD DRIVER

The LCD driver module supports 56×33 (with icon line), or a maximum of 1848 dots. The bias of the LCD driver is 1/5 and the duty is 1/32 or 1/33. To obtain a good quality of LCD display, an internal charge pump voltage generator is included.

LCDCTL (LCD display control register) **:** reset value 0x00

Address	26H / R_W							
bit no	7	6	5	4	3	2	1	0
	—	LCDPMP	LCDC	LCDI	FRQS3	FRQS2	FRQS1	FRQS0

FRQS3	FRQS2	FRQS1	FRQS0	Output fo (f_{XT}= 76.8khz)
0	0	0	0	f_{XT}(76.8khz)
0	0	0	1	f_{XT}/ 2(38.4khz)
0	0	1	0	f_{XT}/ 3(25.6khz)
0	0	1	1	f_{XT}/ 4(19.2khz)
0	1	0	0	f_{XT}/ 5(15.36khz)
0	1	0	1	f_{XT}/ 6(12.8khz)
0	1	1	0	f_{XT}/ 7(10.97khz)
0	1	1	1	f_{XT}/ 8(9.6khz)
1	0	0	0	f_{XT}/ 9(8.53khz)

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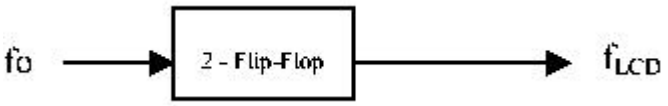
1	0	0	1	f_{XT} / 10 (7.68khz)
1	0	1	0	f_{XT} / 11 (6.98khz)
1	0	1	1	f_{XT} / 12 (6.4khz)
1	1	0	0	f_{XT} / 13 (5.9khz)
1	1	0	1	f_{XT} / 14 (5.485khz)
1	1	1	0	f_{XT} / 15 (5.12khz)
1	1	1	1	f_{XT} / 16 (4.8khz)

Note : The actual frame frequency to the LCD is $f_{LCD,}$ and equals to fo/4



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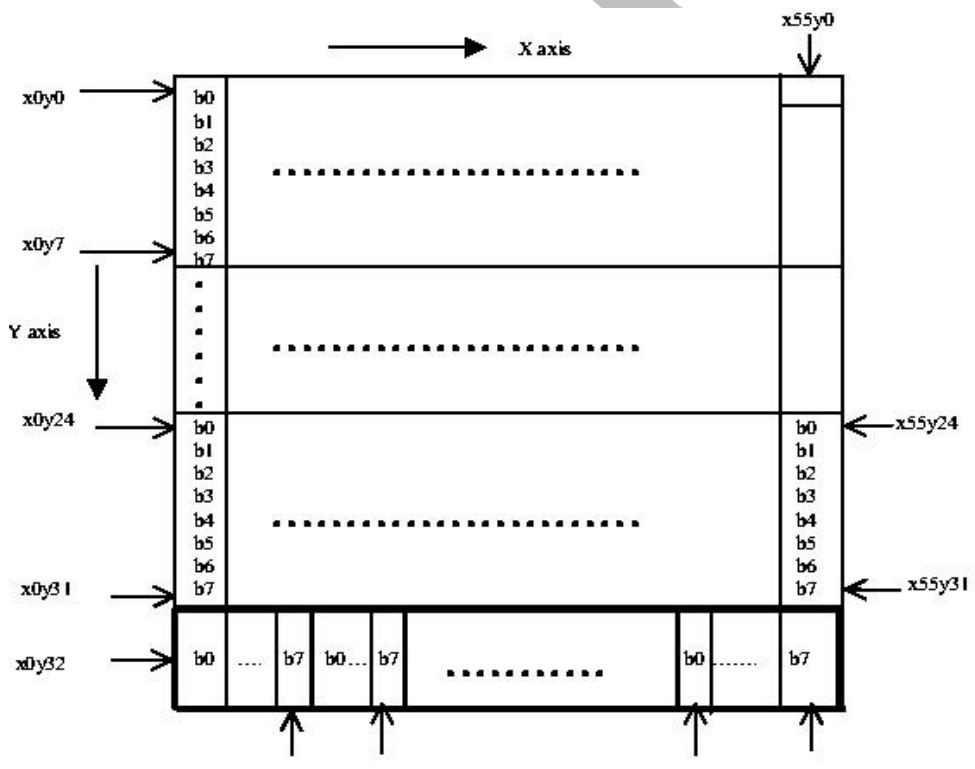
LCDPMP	LCDC	LCDI	Function
—	0	—	Disable LCD display
—	1	0	Enable LCD display without icon line
—	1	1	Enable LCD display with icon line
0	—	—	LCD voltage pumping OFF
1	—	—	LCD voltage pumping ON

LCD Display RAM Memory Mapping



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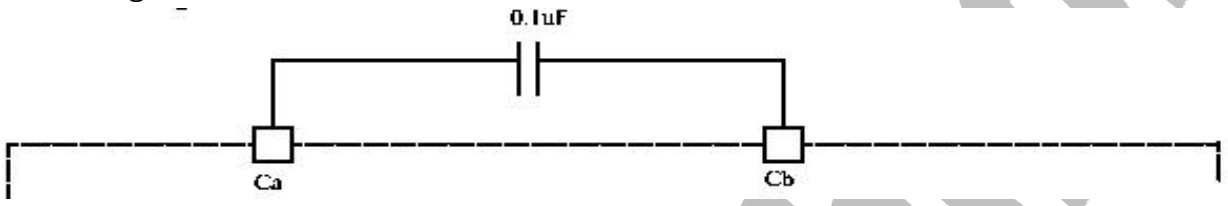
Connecting Configurations of LCD Bias

✧ **Voltage Doubler**



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SECTION 7. Serial I/O Interface

SOCTL (Serial I/O control register) **:** reset value 0x00

Address	27H / R_W							
bit no	7	6	5	4	3	2	1	0
	SIOE	—	—	—	—	—	—	SCKO

When **SIOE** is set, the **P00_RE, P01_RE1,** and **P27_RE2** will become the **SCK, MOSI,** and **MISO** port function. It also enables the **768KO** pin to send 76.8KHz clock. User must use the **P21_SS,** and **P06_RDY** pin to recognize whether it is in sending or receiving mode when communicates with flex decoder. When it is ready, set **SCKO** and a 76.8kHz clock of 32bits will send out. The data in **SIOB0-3** will be send synchronized with **SCK** by **MOSI** pin. And **SIOB0-3** will also receive data from flex decoder at the same time by **MISO** pin. So wt5082 uses the same address for different register to input and output. When it is finished, it generates a IRQ interrupt to CPU by **FSIO** in **IRQSR**, user can mask this interrupt by **MSIO** in **IRQMK.**

SIOB0 (Serial I/O sending data Buffer 0 register) **:** reset value 0x00

Address	28H / R_W							
bit no	7	6	5	4	3	2	1	0
	SIOB07	SIOB06	SIOB05	SIOB04	SIOB03	SIOB02	SIOB01	SIOB00

SIOB1 (Serial I/O sending data Buffer 1 register) **:** reset value 0x00

Address	29H / R_W

bit no	7	6	5	4	3	2	1	0
	SIOB15	SIOB14	SIOB13	SIOB12	SIOB11	SIOB10	SIOB09	SIOB08

SIOB2 (Serial I/O sending data Buffer 2 register) **:** reset value 0x00

Address	2AH / R_W							
bit no	7	6	5	4	3	2	1	0
	SIOB23	SIOB22	SIOB21	SIOB20	SIOB19	SIOB18	SIOB17	SIOB16

SIOB3 (Serial I/O sending data Buffer 3 register) **:** reset value 0x00

Address	2BH / R_W							
bit no	7	6	5	4	3	2	1	0
	SIOB31	SIOB30	SIOB29	SIOB28	SIOB27	SIOB26	SIOB25	SIOB24

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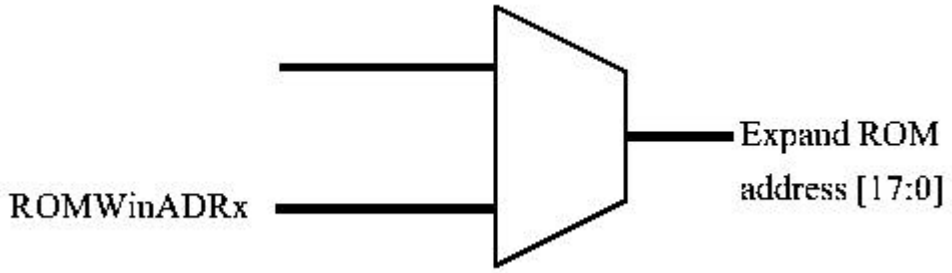
SECTION 8. Expanded ROM

This chip has embedded extra-large ROM, and we use virtual memory bank to access expanded ROM. The virtual memory bank is set **ROMW in ADRx** as high byte and 6502 address [12 0] as low byte. ROMWinADR0 use in Data Memory 0 from $4000 ~ $5FFF, ROMWinADR1 uses in Data Memory 1 from $6000 ~ $7FFF.



For example, when the ROMWinADR0 equal to $06 and 6502 address equal $55AA, it will access expand rom with address $D5AA

ROMWinADR0 (Expand ROM Window0 address register): reset value 0x00

Address	1EH / R_W

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bit no	7	6	5	4	3	2	1	0
	—	—	—	W0A4	W0A3	W0A2	W0A1	W0A0

ROMWinADR1 (Expand ROM Windowl address register): reset value 0x00

Address	1FH / R_W							
bit no	7	6	5	4	3	2	1	0
	—	—	—	W1A4	W1A3	W1A2	W1A1	W1A0

Configuration of ROM

256Kbytes Character ROM

32Kbytes Program ROM

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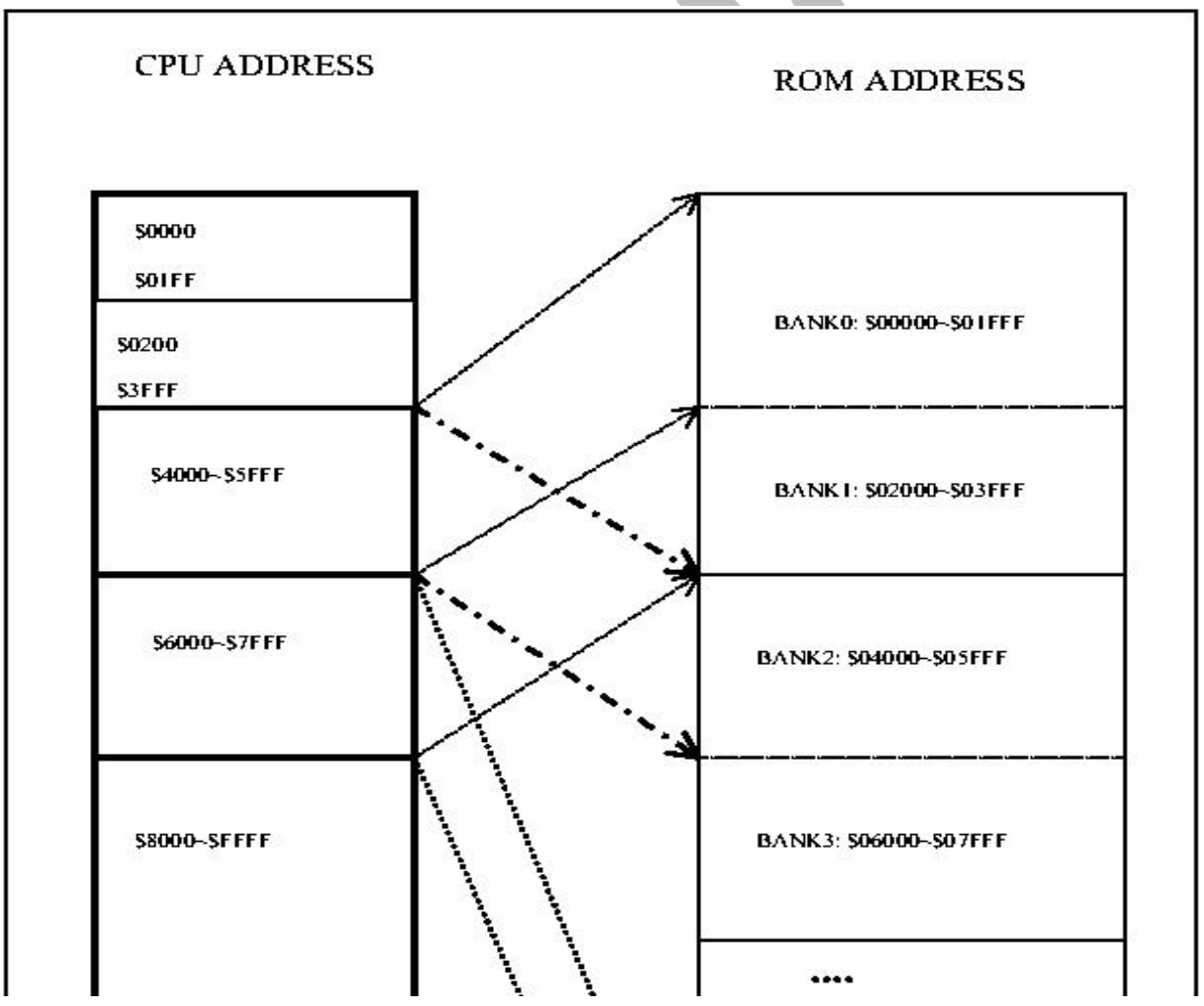

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Section 9. UART

To supply communication of PC and wt5082, UART function is supplied. Set **EUART** to enable UART function active, and P21 will switch as data out and P06 will switch as data in. The baud rate of UART is 9600 baud rate. The UART Data Buffer **UARTD** is active when **EUART** is enabled. When ready sending data out with UART, user must set **UART_TX** to start UART data out. **EPI6** is used to interrupt cpu after receiving data and sending data, user can check **RX_Full** and **TX_Empty** to verify if Receive Buffer is Full or Transmit Buffer is Empty.

UARTCTL (UART control register):reset value 0x00

Address	2CH / R_W							
bit no	7	6	5	4	3	2	1	0
	EUART	—	**RX_Full**	**TX_Empty**	—	—	—	**UART_TX**

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RX_FULL	TX_EMPTY	Status
X	1	TX_Buffer is Empty
1	X	RX Buffer is Full

UARTD (Serial I/O Buffer and UART Data buffer register): reset value 0x00

Address	28H / R_W							
bit no	7	6	5	4	3	2	1	0
	SIOB07 / UARTD 7	**SIOB06 / UARTD 6**	**SIOB05 / UARTD5**	**SIOB04 / UARTD4**	**SIOB03 / UARTD 3**	**SIOB02 / UARTD 2**	**SIOB01 / UARTD 1**	**SIOB00 / UARTD0**

UARTD is active only when **EUART** equals High

Section 10. PWM

The PWM function is control by **PWMCTL** register, user can set **EPWM** to enable PWM function internal clock and function, and switch **P07** as PWM signal output, Port **768KO** as output for enable control. And **EPI7** is used to end of PWM transmission.

PWMCTL (PWM Control register): reset value 0x00

Address	2DH / R_W							
bit no	7	6	5	4	3	2	1	0
	EPWM	—	PWM_TX	ClrPAdr	PIndex3	PIndex2	PIndex1	PIndex0

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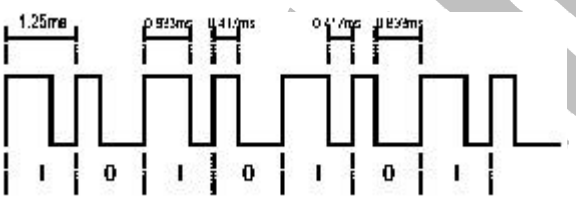
User can set **EPWM** to enable PWM circuit clock, The PWM function output is a 800 baud rate PWM signal. There are

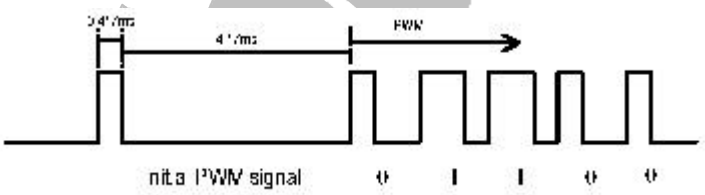
16 bytes register to store pattern. When writing **PWMB** register once, the internal address of **PWMBx** will increase automatically. User can set **ClrPAdr** to reset internal address of **PWMBx** to initial address and remember initial address

is 0x0F.

Plndex is descided how many bytes will send out to Port P07. When **PIndex** equals to 0x04, It will shift data from PB4x to PB0x and LSB first. User can set **PWM_TX** to start sending PWM signal, and **PWM_TX** will reset automatically till the end of PWM signal. And Port **768KO** will be preactive to high 3 bits and delay 2 bits to low till end of PWM signal. Before send user program data from PWMBx, wt5082 will send Initial PWM pattern about 4.587ms first.



PWM signal timing pattern



Initial PWM signal timing pattern

v.0.97

PWMB (PWM Data Buffer register): reset value 0x00

Address	2EH / R_W							
bit no	7	6	5	4	3	2	1	0
	PWMBx7	PWMBx6	PWMBx5	PWMBx4	PWMBx3	PWMBx2	PWMBx1	PWMBx0

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PAdr3	PAdr2	PAdr1	PAdr0	PWMB7	PWMB6	PWMB5	PWMB4	PWMB3	PWMB2	PWMB1	PWMB0
0	0	0	0	PB07	PB06	PB05	PB04	PB03	PB02	PB01	PB00
0	0	0	1	PB17	PB16	PB15	PB14	PB13	PB12	PB11	PB10
0	0	1	0	PB27	PB26	PB25	PB24	PB23	PB22	PB21	PB20
0	0	1	1	PB37	PB36	PB35	PB34	PB33	PB32	PB31	PB30
0	1	0	0	PB47	PB46	PB45	PB44	PB43	PB42	PB41	PB40
0	1	0	1	PB57	PB56	PB55	PB54	PB53	PB52	PB51	PB50
0	1	1	0	PB67	PB66	PB65	PB64	PB63	PB62	PB61	PB60
0	1	1	1	PB77	PB76	PB75	PB74	PB73	PB72	PB71	PB70
1	0	0	0	PB87	PB86	PB85	PB84	PB83	PB82	PB81	PB80
1	0	0	1	PB97	PB96	PB95	PB94	PB93	PB92	PB91	PB90
1	0	1	0	PBA7	PBA6	PBA5	PBA4	PBA3	PBA2	PBA1	PBA0
1	0	1	1	PBB7	PBB6	PBB5	PBB4	PBB3	PBB2	PBB1	PBB0
1	1	0	0	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
1	1	0	1	PBD7	PBD6	PBD5	PBD4	PBD3	PBD2	PBD1	PBD0
1	1	1	0	PBE7	PBE6	PBE5	PBE4	PBE3	PBE2	PBE1	PBE0
1	1	1	1	PBF7	PBF6	PBF5	PBF4	PBF3	PBF2	PBF1	PBF0

APPENDIX.A ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (VSS = 0 V)

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	VDD	-0.5 ~ +3.6	V
Input Voltage Range	Vin	-0.5 ~ VDD + 0.5	V
Operating	Tor	0 ~ +70	℃

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Temperature			
Storage Temperature	Tstg	-50 ~ +150	℃

ELECTRICAL CHARACTERISTICS (VSS = 0 V , Topr = 0 to 70℃)

PARAMETER	SYMBOL	Min	Typ.	Max	Unit	CONDITIONS
Operating Voltage	VDD	2.4	—	3.6	V	
Operating Current	I_{OP}		—	60	uA	1MHz @ 3.0V
Standby Current	I_{STB}			5	uA	VDD = 3.0V
OSC Frequency	F_{OSC}		1.0	2.0	MH	VDD = 3.0V
Input High Level	V_{IH}	2.7			V	VDD = 3.0V
Input Low Level	V_{IL}			0.3	V	VDD = 3.0V
Output Current P0 & P2	Ioh		1.0		mA	VDD = 3.0V , Voh = 2.7V
Output Current P0 & P2	Iol	1.0	68		mA	VDD = 3.0V , Vol = 0.5V
CPU Clock	F_{CPU}	0.0		2.0	MH	@ 3.0V

APPENDIX.B LCD DISPLAY SRAM MAPPING

* LCD Display ($3F19)

BYTE-ROW # 1

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	b7	b6	b5	b4	b3	b2	b1	b0
D00 ($3F19) :	x0y7	x0y6	x0y5	x0y4	x0y3	x0y2	x0y1	x0y0
D01 ($3F1A) :	x1y7	x1y6	x1y5	x1y4	x1y3	x1y2	x1y1	x1y0
D02 ($3F1B) :	x2y7	x2y6	x2y5	x2y4	x2y3	x2y2	x2y1	x2y0
D03 ($3F1C) :	x3y7	x3y6	x3y5	x3y4	x3y3	x3y2	x3y1	x3y0
D04 ($3F1D) :	x4y7	x4y6	x4y5	x4y4	x4y3	x4y2	x4y1	x4y0
D05 ($3F1E) :	x5y7	x5y6	x5y5	x5y4	x5y3	x5y2	x5y1	x5y0
D06 ($3F1F) :	x6y7	x6y6	x6y5	x6y4	x6y3	x6y2	x6y1	x6y0
D07 ($3F20) :	x7y7	x7y6	x7y5	x7y4	x7y3	x7y2	x7y1	x7y0
D08 ($3F21) :	x8y7	x8y6	x8y5	x8y4	x8y3	x8y2	x8y1	x8y0
D09 ($3F22) :	x9y7	x9y6	x9y5	x9y4	x9y3	x9y2	x9y1	x9y0
D0A ($3F23) :	x10y7	x10y6	x10y5	x10y4	x10y3	x10y2	x10y1	x10y0
D0B ($3F24) :	x11y7	x11y6	x11y5	x11y4	x11y3	x11y2	x11y1	x11y0
D0C ($3F25) :	x12y7	x12y6	x12y5	x12y4	x12y3	x12y2	x12y1	x12y0
D0D ($3F26) :	x13y7	x13y6	x13y5	x13y4	x13y3	x13y2	x13y1	x13y0
D0E ($3F27) :	x14y7	x14y6	x14y5	x14y4	x14y3	x14y2	x14y1	x14y0
D0F ($3F28) :	x15y7	x15y6	x15y5	x15y4	x15y3	x15y2	x15y1	x15y0
D10 ($3F29) :	x16y7	x16y6	x16y5	x16y4	x16y3	x16y2	x16y1	x16y0
D11 ($3F2A) :	x17y7	x17y6	x17y5	x17y4	x17y3	x17y2	x17y1	x17y0
D12 ($3F2B) :	x18y7	x18y6	x18y5	x18y4	x18y3	x18y2	x18y1	x18y0
D13 ($3F2C) :	x19y7	x19y6	x19y5	x19y4	x19y3	x19y2	x19y1	x19y0
D14 ($3F2D) :	x20y7	x20y6	x20y5	x20y4	x20y3	x20y2	x20y1	x20y0
D15 ($3F2E) :	x21y7	x21y6	x21y5	x21y4	x21y3	x21y2	x21y1	x21y0
D16 ($3F2F) :	x22y7	x22y6	x22y5	x22y4	x22y3	x22y2	x22y1	x22y0
D17 ($3F30) :	x23y7	x23y6	x23y5	x23y4	x23y3	x23y2	x23y1	x23y0
D18 ($3F31) :	x24y7	x24y6	x24y5	x24y4	x24y3	x24y2	x24y1	x24y0
D19 ($3F32) :	x25y7	x25y6	x25y5	x25y4	x25y3	x25y2	x25y1	x25y0
D1A ($3F33) :	x26y7	x26y6	x26y5	x26y4	x26y3	x26y2	x26y1	x26y0
D1B ($3F34) :	x27y7	x27y6	x27y5	x27y4	x27y3	x27y2	x27y1	x27y0
D1C ($3F35) :	x28y7	x28y6	x28y5	x28y4	x28y3	x28y2	x28y1	x28y0
D1D ($3F36) :	x29y7	x29y6	x29y5	x29y4	x29y3	x29y2	x29y1	x29y0
D1E ($3F37) :	x30y7	x30y6	x30y5	x30y4	x30y3	x30y2	x30y1	x30y0
D1F ($3F38) :	x31y7	x31y6	x31y5	x31y4	x31y3	x31y2	x31y1	x31y0

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D20 ($3F39) :	x32y7	x32y6	x32y5	x32y4	x32y3	x32y2	x32y1	x32y0
D21 ($3F3A) :	x33y7	x33y6	x33y5	x33y4	x33y3	x33y2	x33y1	x33y0
D22 ($3F3B) :	x34y7	x34y6	x34y5	x34y4	x34y3	x34y2	x34y1	x34y0
D23 ($3F3C) :	x35y7	x35y6	x35y5	x35y4	x35y3	x35y2	x35y1	x35y0
D24 ($3F3D) :	x36y7	x36y6	x36y5	x36y4	x36y3	x36y2	x36y1	x36y0
D25 ($3F3E) :	x37y7	x37y6	x37y5	x37y4	x37y3	x37y2	x37y1	x37y0
D26 ($3F3F) :	x38y7	x38y6	x38y5	x38y4	x38y3	x38y2	x38y1	x38y0
D27 ($3F40) :	x39y7	x39y6	x39y5	x39y4	x39y3	x39y2	x39y1	x39y0
D28 ($3F41) :	x40y7	x40y6	x40y5	x40y4	x40y3	x40y2	x40y1	x40y0
D29 ($3F42) :	x41y7	x41y6	x41y5	x41y4	x41y3	x41y2	x41y1	x41y0
D2A ($3F43) :	x42y7	x42y6	x42y5	x42y4	x42y3	x42y2	x42y1	x42y0
D2B ($3F44) :	x43y7	x43y6	x43y5	x43y4	x43y3	x43y2	x43y1	x43y0
D2C ($3F45) :	x44y7	x44y6	x44y5	x44y4	x44y3	x44y2	x44y1	x44y0
D2D ($3F46) :	x45y7	x45y6	x45y5	x45y4	x45y3	x45y2	x45y1	x45y0
D2E ($3F47) :	x46y7	x46y6	x46y5	x46y4	x46y3	x46y2	x46y1	x46y0
D2F ($3F48) :	x47y7	x47y6	x47y5	x47y4	x47y3	x47y2	x47y1	x47y0
D30 ($3F49) :	x48y7	x48y6	x48y5	x48y4	x48y3	x48y2	x48y1	x48y0
D31 ($3F4A) :	x49y7	x49y6	x49y5	x49y4	x49y3	x49y2	x49y1	x49y0
D32 ($3F4B) :	x50y7	x50y6	x50y5	x50y4	x50y3	x50y2	x50y1	x50y0
D33 ($3F4C) :	x51y7	x51y6	x51y5	x51y4	x51y3	x51y2	x51y1	x51y0
D34 ($3F4D) :	x52y7	x52y6	x52y5	x52y4	x52y3	x52y2	x52y1	x52y0
D35 ($3F4E) :	x53y7	x53y6	x53y5	x53y4	x53y3	x53y2	x53y1	x53y0
D36 ($3F4F) :	x54y7	x54y6	x54y5	x54y4	x54y3	x54y2	x54y1	x54y0
D37 ($3F50) :	x55y7	x55y6	x55y5	x55y4	x55y3	x55y2	x55y1	x55y0

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BYTE-ROW # 2

	b7	b6	b5	b4	b3	b2	b1	b0
D38 ($3F51) :	x0y15	x0y14	x0y13	x0y12	x0y11	x0y10	x0y9	x0y8
D39 ($3F52) :	x1y15	x1y14	x1y13	x1y12	x1y11	x1y10	x1y9	x1y8
D3A ($3F53) :	x2y15	x2y14	x2y13	x2y12	x2y11	x2y10	x2y9	x2y8
D3B ($3F54) :	x3y15	x3y14	x3y13	x3y12	x3y11	x3y10	x3y9	x3y8
D3C ($3F55) :	x4y15	x4y14	x4y13	x4y12	x4y11	x4y10	x4y9	x4y8
D3D ($3F56) :	x5y15	x5y14	x5y13	x5y12	x5y11	x5y10	x5y9	x5y8
D3E ($3F57) :	x6y15	x6y14	x6y13	x6y12	x6y11	x6y10	x6y9	x6y8
D3F ($3F58) :	x7y15	x7y14	x7y13	x7y12	x7y11	x7y10	x7y9	x7y8
D40 ($3F59) :	x8y15	x8y14	x8y13	x8y12	x8y11	x8y10	x8y9	x8y8
D41 ($3F5A) :	x9y15	x9y14	x9y13	x9y12	x9y11	x9y10	x9y9	x9y8
D42 ($3F5B) :	x10y15	x10y14	x10y13	x10y12	x10y11	x10y10	x10y9	x10y8
D43 ($3F5C) :	x11y15	x11y14	x11y13	x11y12	x11y11	x11y10	x11y9	x11y8
D44 ($3F5D) :	x12y15	x12y14	x12y13	x12y12	x12y11	x12y10	x12y9	x12y8
D45 ($3F5E) :	x13y15	x13y14	x13y13	x13y12	x13y11	x13y10	x13y9	x13y8
D46 ($3F5F) :	x14y15	x14y14	x14y13	x14y12	x14y11	x14y10	x14y9	x14y8
D47 ($3F60) :	x15y15	x15y14	x15y13	x15y12	x15y11	x15y10	x15y9	x15y8
D48 ($3F61) :	x16y15	x16y14	x16y13	x16y12	x16y11	x16y10	x16y9	x16y8
D49 ($3F62) :	x17y15	x17y14	x17y13	x17y12	x17y11	x17y10	x17y9	x17y8
D4A ($3F63) :	x18y15	x18y14	x18y13	x18y12	x18y11	x18y10	x18y9	x18y8
D4B ($3F64) :	x19y15	x19y14	x19y13	x19y12	x19y11	x19y10	x19y9	x19y8
D4C ($3F65) :	x20y15	x20y14	x20y13	x20y12	x20y11	x20y10	x20y9	x20y8
D4D ($3F66) :	x21y15	x21y14	x21y13	x21y12	x21y11	x21y10	x21y9	x21y8
D4E ($3F67) :	x22y15	x22y14	x22y13	x22y12	x22y11	x22y10	x22y9	x22y8
D4F ($3F68) :	x23y15	x23y14	x23y13	x23y12	x23y11	x23y10	x23y9	x23y8

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D57 ($3F70) :	x31y15	x31y14	x31y13	x31y12	x31y11	x31y10	x31y9	x31y8
D58 ($3F71) :	x32y15	x32y14	x32y13	x32y12	x32y11	x32y10	x32y9	x32y8
D59 ($3F72) :	x33y15	x33y14	x33y13	x33y12	x33y11	x33y10	x33y9	x33y8
D5A ($3F73) :	x34y15	x34y14	x34y13	x34y12	x34y11	x34y10	x34y9	x34y8
D5B ($3F74) :	x35y15	x35y14	x35y13	x35y12	x35y11	x35y10	x35y9	x35y8
D5C ($3F75) :	x36y15	x36y14	x36y13	x36y12	x36y11	x36y10	x36y9	x36y8
D5D ($3F76) :	x37y15	x37y14	x37y13	x37y12	x37y11	x37y10	x37y9	x37y8
D5E ($3F77) :	x38y15	x38y14	x38y13	x38y12	x38y11	x38y10	x38y9	x38y8
D5F ($3F78) :	x39y15	x39y14	x39y13	x39y12	x39y11	x39y10	x39y9	x39y8
D60 ($3F79) :	x40y15	x40y14	x40y13	x40y12	x40y11	x40y10	x40y9	x40y8
D61 ($3F7A) :	x41y15	x41y14	x41y13	x41y12	x41y11	x41y10	x41y9	x41y8
D62 ($3F7B) :	x42y15	x42y14	x42y13	x42y12	x42y11	x42y10	x42y9	x42y8
D63 ($3F7C) :	x43y15	x43y14	x43y13	x43y12	x43y11	x43y10	x43y9	x43y8
D64 ($3F7D) :	x44y15	x44y14	x44y13	x44y12	x44y11	x44y10	x44y9	x44y8
D65 ($3F7E) :	x45y15	x45y14	x45y13	x45y12	x45y11	x45y10	x45y9	x45y8
D66 ($3F7F) :	x46y15	x46y14	x46y13	x46y12	x46y11	x46y10	x46y9	x46y8
D67 ($3F80) :	x47y15	x47y14	x47y13	x47y12	x47y11	x47y10	x47y9	x47y8
D68 ($3F81) :	x48y15	x48y14	x48y13	x48y12	x48y11	x48y10	x48y9	x48y8
D69 ($3F82) :	x49y15	x49y14	x49y13	x49y12	x49y11	x49y10	x49y9	x49y8
D6A ($3F83) :	x50y15	x50y14	x50y13	x50y12	x50y11	x50y10	x50y9	x50y8
D6B ($3F84) :	x51y15	x51y14	x51y13	x51y12	x51y11	x51y10	x51y9	x51y8
D6C ($3F85) :	x52y15	x52y14	x52y13	x52y12	x52y11	x52y10	x52y9	x52y8
D6D ($3F86) :	x53y15	x53y14	x53y13	x53y12	x53y11	x53y10	x53y9	x53y8
D6E ($3F87) :	x54y15	x54y14	x54y13	x54y12	x54y11	x54y10	x54y9	x54y8
D6F ($3F88) :	x55y15	x55y14	x55y13	x55y12	x55y11	x55y10	x55y9	x55y8

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BYTE-ROW # 3

D70	($3F89) :	x0y23	x0y22	x0y21	x0y20	x0y19	x0y18	x0y17	x0y16
D71	($3F8A) :	x1y23	x1y22	x1y21	x1y20	x1y19	x1y18	x1y17	x1y16
D72	($3F8B) :	x2y23	x2y22	x2y21	x2y20	x2y19	x2y18	x2y17	x2y16
D73	($3F8C) :	x3y23	x3y22	x3y21	x3y20	x3y19	x3y18	x3y17	x3y16
D74	($3F8D) :	x4y23	x4y22	x4y21	x4y20	x4y19	x4y18	x4y17	x4y16
D75	($3F8E) :	x5y23	x5y22	x5y21	x5y20	x5y19	x5y18	x5y17	x5y16
D76	($3F8F) :	x6y23	x6y22	x6y21	x6y20	x6y19	x6y18	x6y17	x6y16
D77	($3F90) :	x7y23	x7y22	x7y21	x7y20	x7y19	x7y18	x7y17	x7y16
D78	($3F91) :	x8y23	x8y22	x8y21	x8y20	x8y19	x8y18	x8y17	x8y16
D79	($3F92) :	x9y23	x9y22	x9y21	x9y20	x9y19	x9y18	x9y17	x9y16
D7A	($3F93) :	x10y23	x10y22	x10y21	x10y20	x10y19	x10y18	x10y17	x10y16
D7B	($3F94) :	x11y23	x11y22	x11y21	x11y20	x11y19	x11y18	x11y17	x11y16
D7C	($3F95) :	x12y23	x12y22	x12y21	x12y20	x12y19	x12y18	x12y17	x12y16
D7D	($3F96) :	x13y23	x13y22	x13y21	x13y20	x13y19	x13y18	x13y17	x13y16
D7E	($3F97) :	x14y23	x14y22	x14y21	x14y20	x14y19	x14y18	x14y17	x14y16
D7F	($3F98) :	x15y23	x15y22	x15y21	x15y20	x15y19	x15y18	x15y17	x15y16
D80	($3F99) :	x16y23	x16y22	x16y21	x16y20	x16y19	x16y18	x16y17	x16y16
D81	($3F9A) :	x17y23	x17y22	x17y21	x17y20	x17y19	x17y18	x17y17	x17y16
D82	($3F9B) :	x18y23	x18y22	x18y21	x18y20	x18y19	x18y18	x18y17	x18y16
D83	($3F9C) :	x19y23	x19y22	x19y21	x19y20	x19y19	x19y18	x19y17	x19y16
D84	($3F9D) :	x20y23	x20y22	x20y21	x20y20	x20y19	x20y18	x20y17	x20y16
D85	($3F9E) :	x21y23	x21y22	x21y21	x21y20	x21y19	x21y18	x21y17	x21y16
D86	($3F9F) :	x22y23	x22y22	x22y21	x22y20	x22y19	x22y18	x22y17	x22y16
D87	($3FA0) :	x23y23	x23y22	x23y21	x23y20	x23y19	x23y18	x23y17	x23y16
D88	($3FA1) :	x24y23	x24y22	x24y21	x24y20	x24y19	x24y18	x24y17	x24y16
D89	($3FA2) :	x25y23	x25y22	x25y21	x25y20	x25y19	x25y18	x25y17	x25y16
D8A	($3FA3) :	x26y23	x26y22	x26y21	x26y20	x26y19	x26y18	x26y17	x26y16
D8B	($3FA4) :	x27y23	x27y22	x27y21	x27y20	x27y19	x27y18	x27y17	x27y16
D8C	($3FA5) :	x28y23	x28y22	x28y21	x28y20	x28y19	x28y18	x28y17	x28y16
D8D	($3FA6) :	x29y23	x29y22	x29y21	x29y20	x29y19	x29y18	x29y17	x29y16
D8E	($3FA7) :	x30y23	x30y22	x30y21	x30y20	x30y19	x30y18	x30y17	x30y16
D8F	($3FA8) :	x31y23	x31y22	x31y21	x31y20	x31y19	x31y18	x31y17	x31y16

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D90	($3FA9) :	x32y23	x32y22	x32y21	x32y20	x32y19	x32y18	x32y17	x32y16
D91	($3FAA) :	x33y23	x33y22	x33y21	x33y20	x33y19	x33y18	x33y17	x33y16
D92	($3FAB) :	x34y23	x34y22	x34y21	x34y20	x34y19	x34y18	x34y17	x34y16
D93	($3FAC) :	x35y23	x35y22	x35y21	x35y20	x35y19	x35y18	x35y17	x35y16
D94	($3FAD) :	x36y23	x36y22	x36y21	x36y20	x36y19	x36y18	x36y17	x36y16
D95	($3FAE) :	x37y23	x37y22	x37y21	x37y20	x37y19	x37y18	x37y17	x37y16
D96	($3FAF) :	x38y23	x38y22	x38y21	x38y20	x38y19	x38y18	x38y17	x38y16
D97	($3FB0) :	x39y23	x39y22	x39y21	x39y20	x39y19	x39y18	x39y17	x39y16
D98	($3FB1) :	x40y23	x40y22	x40y21	x40y20	x40y19	x40y18	x40y17	x40y16
D99	($3FB2) :	x41y23	x41y22	x41y21	x41y20	x41y19	x41y18	x41y17	x41y16
D9A	($3FB3) :	x42y23	x42y22	x42y21	x42y20	x42y19	x42y18	x42y17	x42y16
D9B	($3FB4) :	x43y23	x43y22	x43y21	x43y20	x43y19	x43y18	x43y17	x43y16
D9C	($3FB5) :	x44y23	x44y22	x44y21	x44y20	x44y19	x44y18	x44y17	x44y16
D9D	($3FB6) :	x45y23	x45y22	x45y21	x45y20	x45y19	x45y18	x45y17	x45y16
D9E	($3FB7) :	x46y23	x46y22	x46y21	x46y20	x46y19	x46y18	x46y17	x46y16
D9F	($3FB8) :	x47y23	x47y22	x47y21	x47y20	x47y19	x47y18	x47y17	x47y16
DA0	($3FB9) :	x48y23	x48y22	x48y21	x48y20	x48y19	x48y18	x48y17	x48y16
DA1	($3FBA) :	x49y23	x49y22	x49y21	x49y20	x49y19	x49y18	x49y17	x49y16
DA2	($3FBB) :	x50y23	x50y22	x50y21	x50y20	x50y19	x50y18	x50y17	x50y16
DA3	($3FBC) :	x51y23	x51y22	x51y21	x51y20	x51y19	x51y18	x51y17	x51y16
DA4	($3FBD) :	x52y23	x52y22	x52y21	x52y20	x52y19	x52y18	x52y17	x52y16
DA5	($3FBE) :	x53y23	x53y22	x53y21	x53y20	x53y19	x53y18	x53y17	x53y16
DA6	($3FBF) :	x54y23	x54y22	x54y21	x54y20	x54y19	x54y18	x54y17	x54y16
DA7	($3FC0) :	x55y23	x55y22	x55y21	x55y20	x55y19	x55y18	x55y17	x55y16

BYTE-ROW # 4

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DA8	($ 3FC1) :	x0y31	x0y30	x0y29	x0y28	x0y27	x0y26	x0y25	x0y24
DA9	($ 3FC2) :	x1y31	x1y30	x1y29	x1y28	x1y27	x1y26	x1y25	x1y24
DAA	($ 3FC3) :	x2y31	x2y30	x2y29	x2y28	x2y27	x2y26	x2y25	x2y24
DAB	($ 3FC4) :	x3y31	x3y30	x3y29	x3y28	x3y27	x3y26	x3y25	x3y24
DAC	($ 3FC5) :	x4y31	x4y30	x4y29	x4y28	x4y27	x4y26	x4y25	x4y24
DAD	($ 3FC6) :	x5y31	x5y30	x5y29	x5y28	x5y27	x5y26	x5y25	x5y24
DAE	($ 3FC7) :	x6y31	x6y30	x6y29	x6y28	x6y27	x6y26	x6y25	x6y24
DAF	($ 3FC8) :	x7y31	x7y30	x7y29	x7y28	x7y27	x7y26	x7y25	x7y24
DB0	($ 3FC9) :	x8y31	x8y30	x8y29	x8y28	x8y27	x8y26	x8y25	x8y24
DB1	($ 3FCA) :	x9y31	x9y30	x9y29	x9y28	x9y27	x9y26	x9y25	x9y24
DB2	($ 3FCB) :	x10y31	x10y30	x10y29	x10y28	x10y27	x10y26	x10y25	x10y24
DB3	($ 3FCC) :	x11y31	x11y30	x11y29	x11y28	x11y27	x11y26	x11y25	x11y24
DB4	($ 3FCD) :	x12y31	x12y30	x12y29	x12y28	x12y27	x12y26	x12y25	x12y24
DB5	($ 3FCE) :	x13y31	x13y30	x13y29	x13y28	x13y27	x13y26	x13y25	x13y24
DB6	($ 3FCF) :	x14y31	x14y30	x14y29	x14y28	x14y27	x14y26	x14y25	x14y24
DB7	($ 3FD0) :	x15y31	x15y30	x15y29	x15y28	x15y27	x15y26	x15y25	x15y24
DB8	($ 3FD1) :	x16y31	x16y30	x16y29	x16y28	x16y27	x16y26	x16y25	x16y24
DB9	($ 3FD2) :	x17y31	x17y30	x17y29	x17y28	x17y27	x17y26	x17y25	x17y24
DBA	($ 3FD3) :	x18y31	x18y30	x18y29	x18y28	x18y27	x18y26	x18y25	x18y24
DBB	($ 3FD4) :	x19y31	x19y30	x19y29	x19y28	x19y27	x19y26	x19y25	x19y24
DBC	($ 3FD5) :	x20y31	x20y30	x20y29	x20y28	x20y27	x20y26	x20y25	x20y24
DBD	($ 3FD6) :	x21y31	x21y30	x21y29	x21y28	x21y27	x21y26	x21y25	x21y24
DBE	($ 3FD7) :	x22y31	x22y30	x22y29	x22y28	x22y27	x22y26	x22y25	x22y24
DBF	($ 3FD8) :	x23y31	x23y30	x23y29	x23y28	x23y27	x23y26	x23y25	x23y24
DC0	($ 3FD9) :	x24y31	x24y30	x24y29	x24y28	x24y27	x24y26	x24y25	x24y24
DC1	($ 3FDA) :	x25y31	x25y30	x25y29	x25y28	x25y27	x25y26	x25y25	x25y24
DC2	($ 3FDB) :	x26y31	x26y30	x26y29	x26y28	x26y27	x26y26	x26y25	x26y24
DC3	($ 3FDC) :	x27y31	x27y30	x27y29	x27y28	x27y27	x27y26	x27y25	x27y24
DC4	($ 3FDD) :	x28y31	x28y30	x28y29	x28y28	x28y27	x28y26	x28y25	x28y24
DC5	($ 3FDE) :	x29y31	x29y30	x29y29	x29y28	x29y27	x29y26	x29y25	x29y24
DC6	($ 3FDF) :	x30y31	x30y30	x30y29	x30y28	x30y27	x30y26	x30y25	x30y24
DC7	($ 3FE0) :	x31y31	x31y30	x31y29	x31y28	x31y27	x31y26	x31y25	x31y24
DC8	($ 3FE1) :	x32y31	x32y30	x32y29	x32y28	x32y27	x32y26	x32y25	x32y24
DC9	($ 3FE2) :	x33y31	x33y30	x33y29	x33y28	x33y27	x33y26	x33y25	x33y24

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DCA ($3FE3) :	x34y31	x34y30	x34y29	x34y28	x34y27	x34y26	x34y25	x34y24
DCB ($3FE4) :	x35y31	x35y30	x35y29	x35y28	x35y27	x35y26	x35y25	x35y24
DCC ($3FE5) :	x36y31	x36y30	x36y29	x36y28	x36y27	x36y26	x36y25	x36y24
DCD ($3FE6) :	x37y31	x37y30	x37y29	x37y28	x37y27	x37y26	x37y25	x37y24
DCE ($3FE7) :	x38y31	x38y30	x38y29	x38y28	x38y27	x38y26	x38y25	x38y24
DCF ($3FE8) :	x39y31	x39y30	x39y29	x39y28	x39y27	x39y26	x39y25	x39y24
DD0 ($3FE9) :	x40y31	x40y30	x40y29	x40y28	x40y27	x40y26	x40y25	x40y24
DD1 ($3FEA) :	x41y31	x41y30	x41y29	x41y28	x41y27	x41y26	x41y25	x41y24
DD2 ($3FEB) :	x42y31	x42y30	x42y29	x42y28	x42y27	x42y26	x42y25	x42y24
DD3 ($3FEC) :	x43y31	x43y30	x43y29	x43y28	x43y27	x43y26	x43y25	x43y24
DD4 ($3FED) :	x44y31	x44y30	x44y29	x44y28	x44y27	x44y26	x44y25	x44y24
DD5 ($3FEE) :	x45y31	x45y30	x45y29	x45y28	x45y27	x45y26	x45y25	x45y24
DD6 ($3FEF) :	x46y31	x46y30	x46y29	x46y28	x46y27	x46y26	x46y25	x46y24
DD7 ($3FF0) :	x47y31	x47y30	x47y29	x47y28	x47y27	x47y26	x47y25	x47y24
DD8 ($3FF1) :	x48y31	x48y30	x48y29	x48y28	x48y27	x48y26	x48y25	x48y24
DD9 ($3FF2) :	x49y31	x49y30	x49y29	x49y28	x49y27	x49y26	x49y25	x49y24
DDA ($3FF3) :	x50y31	x50y30	x50y29	x50y28	x50y27	x50y26	x50y25	x50y24
DDB ($3FF4) :	x51y31	x51y30	x51y29	x51y28	x51y27	x51y26	x51y25	x51y24
DDC ($3FF5) :	x52y31	x52y30	x52y29	x52y28	x52y27	x52y26	x52y25	x52y24
DDD ($3FF6) :	x53y31	x53y30	x53y29	x53y28	x53y27	x53y26	x53y25	x53y24
DDE ($3FF7) :	x54y31	x54y30	x54y29	x54y28	x54y27	x54y26	x54y25	x54y24
DDF ($3FF8) :	x55y31	x55y30	x55y29	x55y28	x55y27	x55y26	x55y25	x55y24

BYTE-ROW # 5 (ICON LINE)

DE0 ($3FF9) :	x07y32	x06y32	x05y32	x04y32	x03y32	x02y32	x01y32	x00y32
DE1 ($3FFA) :	x15y32	x14y32	x13y32	x12y32	x11y32	x10y32	x09y32	x08y32
DE2 ($3FFB) :	x23y32	x22y32	x21y32	x20y32	x19y32	x18y32	x17y32	x16y32
DE3 ($3FFC) :	x31y32	x30y32	x29y32	x28y32	x27y32	x26y32	x25y32	x24y32
DE4 ($3FFD) :	x39y32	x38y32	x37y32	x36y32	x35y32	x34y32	x33y32	x32y32
DE5 ($3FFE) :	x47y32	x46y32	x45y32	x44y32	x43y32	x42y32	x41y32	x40y32
DE6 ($3FFF) :	x55y32	x54y32	x53y32	x52y32	x51y32	x250y32	x49y32	x48y32