WT5053

8-bit μC with 4KB ROM and an 8-CH 12-bit A/D Converter

DESCRIPTION

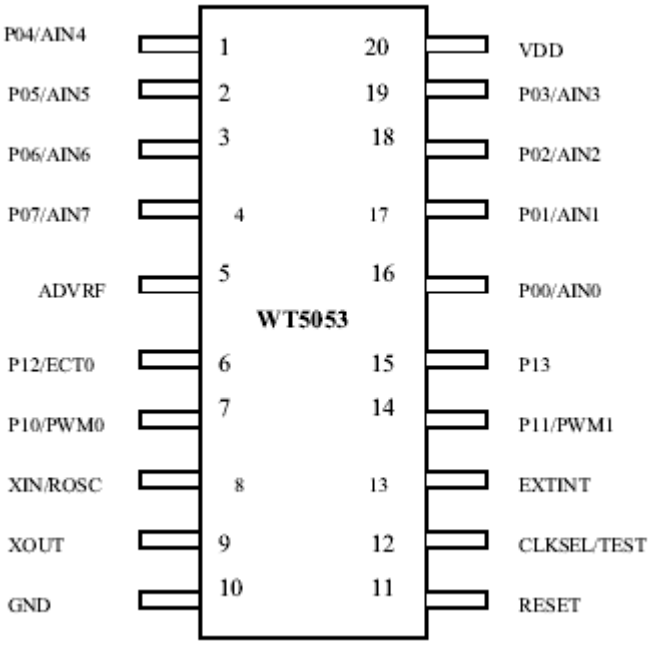
The WT5053 is a high-performance, low-cost, CMOS 8-bit single-chip microcontroller with 4KBytes on-chip ROM and an 8-channel 12-bit analog to digital converter. This chip is suitable for variable applications, especially where analog signal (sensor output) to digital signal conversion is required, including industrial control, consumer, communications, and security products.

This chip has 8-bit CPU, RAM, ROM, I/Os, dual 16-bit timer/counters, interrupt controller, and an 8-channel 12-bit A/D converter. To be suitable for portable battery-powered applications, a power saving function is included.

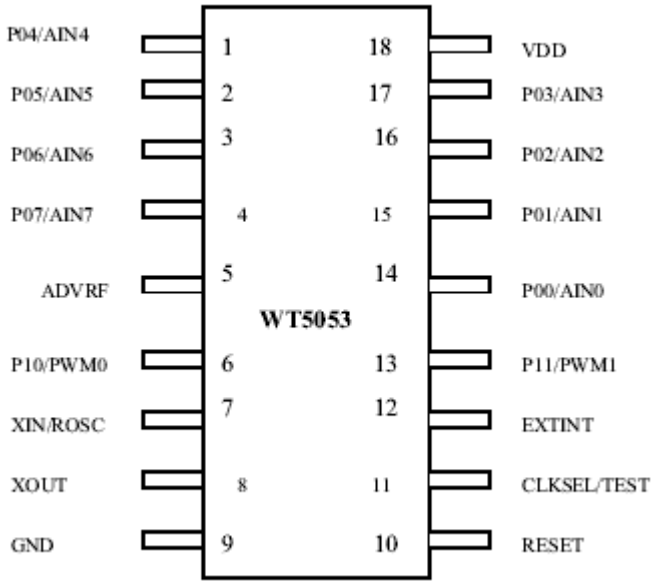
FEATURES

- 8-bit single chip microcontroller with 4Kbytes ROM and 128bytes SRAM
- Wide voltage operating range from 2.4 V to 5.5 V
- On-chip RC oscillator runs at 2MHz and crystal oscillator can run up to 8.0 MHz
- 6 interrupt sources (external: 1; internal:5); all sources have independent latches each multiple interrupt control is available
- I/O port (12 pins)
  - Port PO 8 pins (shared with analog inputs;
  - Port P1 4 pins (20mA sink current)
- Operating current 2mA/4MHz~5V; providing standby mode (OSC is stopped and current consumption < 1 uA~5V)
- Watchdog timer
- Dual PWM
- Dual 16-bit timer/counters
- A/D converter module
  - 8 analog inputs multiplexed into one A/D converter
  - Sample and hold
  - 20 [tS conversion time/per channel
  - 12-bit resolution with +2 LSB accuracy
  - External reference input, AD_{VRF}
- Package: Chip form, or 20/18/16-pin PDIP/SOP

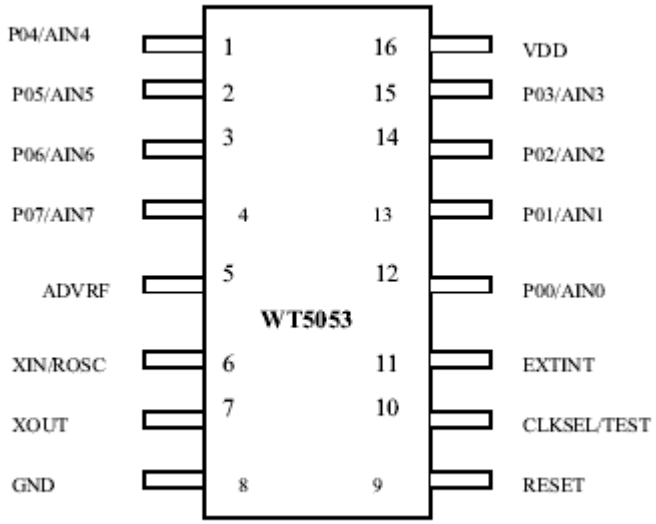
PACKAGE PIN ASSIGNMENT (20-PIN PDIP)



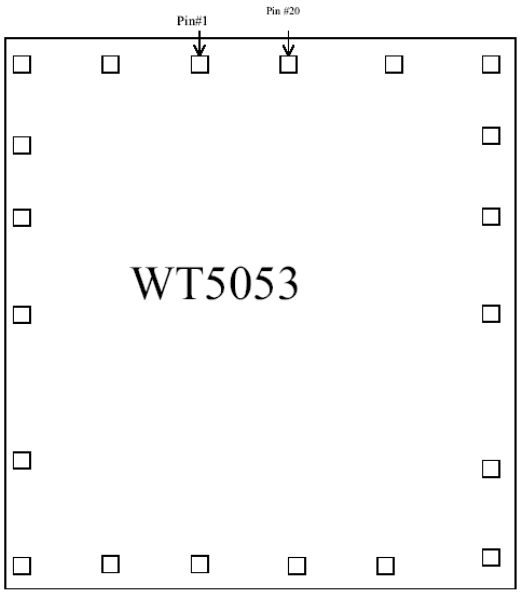
PACKAGE PIN ASSIGNMENT (18-PIN PDIP)



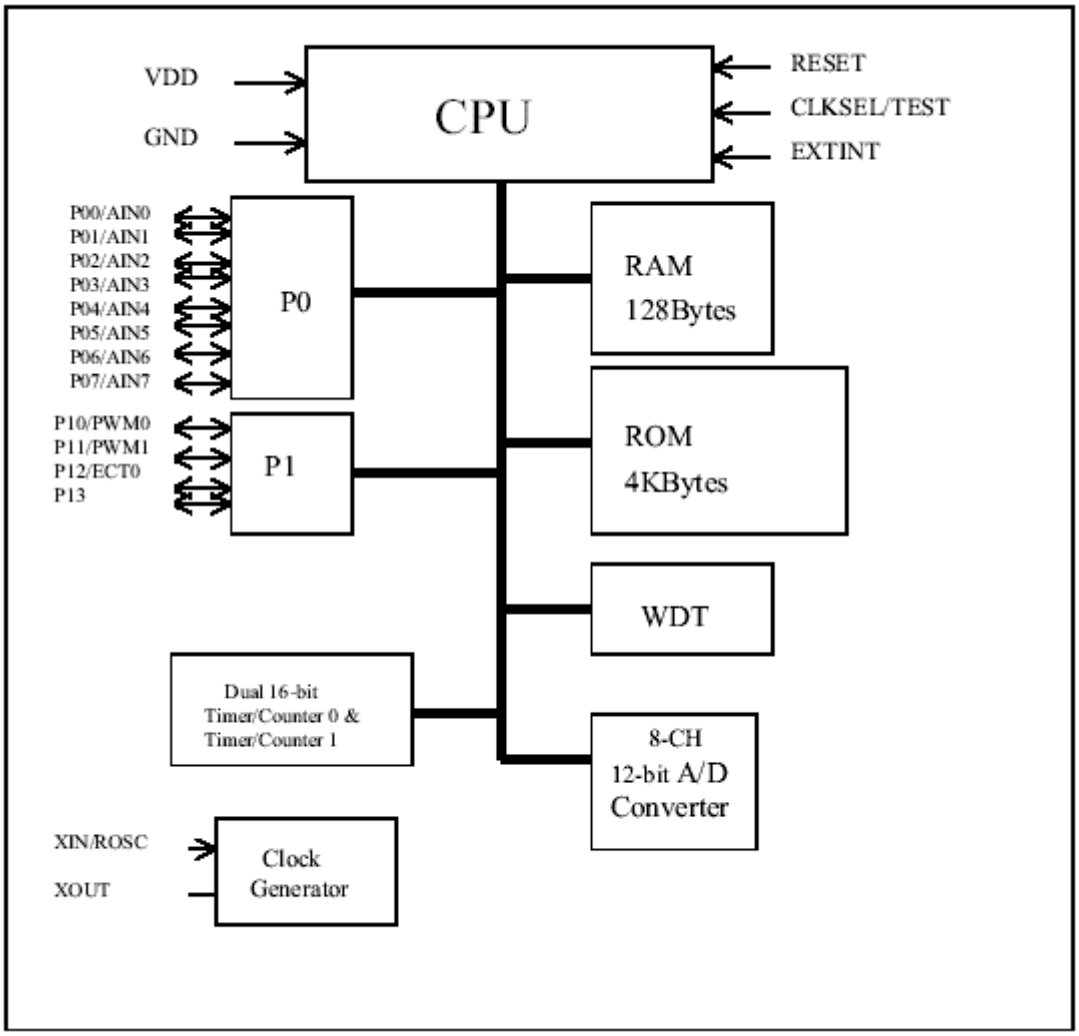
PACKAGE PIN ASSIGNMENT (16-PIN PDIP)



PAD LAYOUT



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	20-pin (18-pin) [16-pin]	In/Out	FUNCTIONS
P00/AIN0 ~ P03/AIN3 P04/AIN4 ~ P07/AIN7	16 ~19 (14~17) [12~15] 1~4 (1~4) [1~4]	I/O	8-bit I/O port; Internal pull-up; o/p: sink 20mA(P04~P07); i/p: external pull-low
P10/PWM0 P11/PWM1 P12/ECT0 P13	7 (6) [X] 14 (13) [X] 6 (X) [X] 15 (X) [X]	I/O	(PWM0 output) (PWM1 output) (External counter input) 4-bit I/O port; internal pull-up; o/p: sink 20mA; i/p: external pull-low
XIN/ROSC	8 (7) [6]	Input	Crystal input/ROSC input
XOUT	9 (8) [7]	Output	Crystal output
RESET	11 (10) [9]	Input	System reset signal input; low active
VDD	20 (18) [16]	Input	Power source
GND	10 (9) [8]	Input	Ground
AD_{VRF}	5 (5) [5]	Input	Reference voltage input to A/D
EXTINT	13 (12) [11]	Input	External interrupt input
CLKSEL/TEST	12 (11) [10]	Input	Clock sources select, connected to VDD for ROSC or to GND for Crystal (Test Pin)

FUNCTION DESCRIPTION

[1] I/O PORTS

The WT5053 has 2 ports (12 pins) each as follows:

- o P00 - P07 ; 8-bit FO port (shared with analog input AIN0-AIN7)
- o P 10 - P 13 ; 4-bit I/O port (shared with PWM0/PWM 1, ECT0)

< 1 > Port P0 (P00 –P07)

Port P0 is an 8-bit bi-directional I/O port and its Data Register and Direction Control Register are located in P0DR ($00) and P0DCR ($26), respectively. All port pins have individually selectable pull-up resistors, and among them, P04-P07 output buffers are designed to have the capability to sink 20mA and thus can drive LED directly.

Port P0 pins are shared with analog inputs (in this case, P0x must be configured as input). When used as digital I/O pins, then P0x is configured as output pin if P0DCRx is set to "1"; otherwise, if P0DCRx is cleared to "0", then P0x is configured as an input pin. For more detail about the P0 port configuration, please refer to Table 1.

Note: When pins of port P0 are used as inputs and externally pulled low, then they will source current if the internal pins are pulled up.

1.1 Port P0 Data Register (P0DR; $00); RJW; Initial value 00H

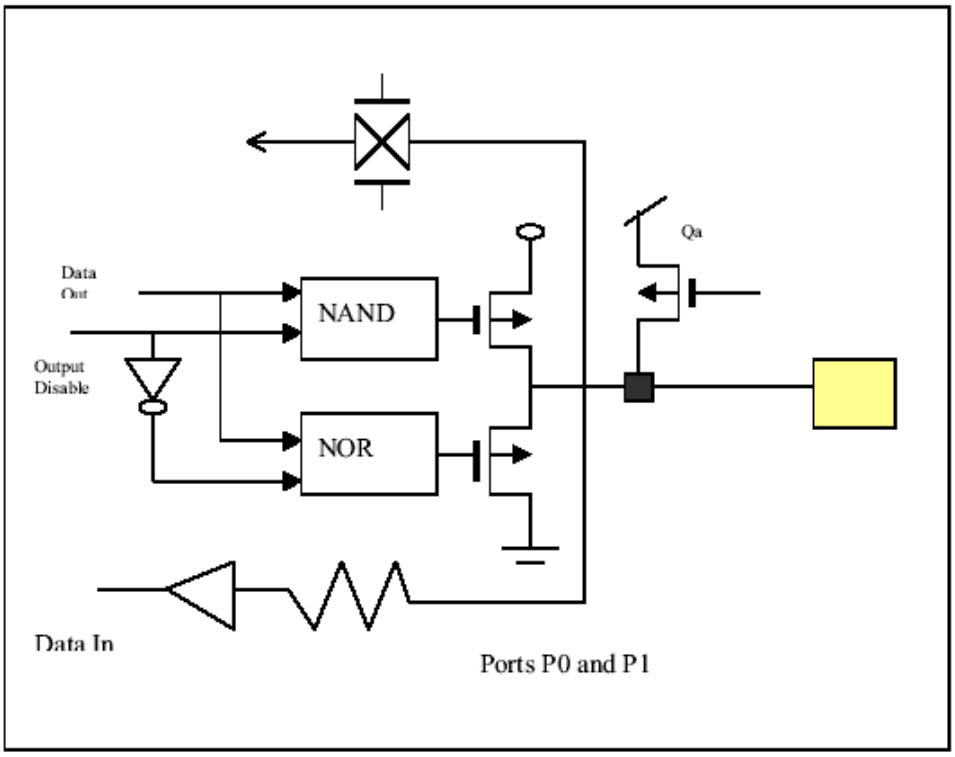
B7	B6	B5	B4	B3	B2	B1	B0
P0DR7	P0DR6	P0DR5	P0DR4	P0DR3	P0DR2	P0DR1	P0DR0

1.2 Port P0 Data Direction Control Register (P0DCR; $26); RJW; Initial value 00H

B7	B6	B5	B4	B3	B2	B1	B0
P0DCR7	P0DCR6	P0DCR5	P0DCR4	P0DCR3	P0DCR2	P0DCR1	P0DCR0

Table 1. Port P0 Configuration

P0DCR0 ~ 7	P0DR0 ~ 7	I/O	Pull-up	Results
0	0	In	No	Tri-state (Hi-Z)
0	1	In	Yes	P00 ~ P07 with pull-up resistor (MOS) (NOTE)
1	0	Output	No	Output “0”
1	1	Output	No	Output “0”



Ports P0 and P1

< 2 > Port P1 (P10 - P13)

Port P1 is an 4-bit bi-directional I/O port and its Data Register and Direction Control Register are located in P1DR ($01) and P1DCR ($27), respectively. All port pins have individually selectable pull-up resistors and all their output buffers are designed to have the capability to sink 20mA and thus can drive LED directly.

When used as digital I/O pins, then P1x is configured as output pin if P1DCRx is set to "1"; otherwise, if P1DCRx is cleared to "0", then P1x is configured as input pin. For more detail about the configuration, please refer to Table 2.

Note: When pins of port P 1 are used as inputs and externally pulled low, then they will source current if the internal pins are pulled up.

2.1 Port P1 Data Register (P1DR; $01); R/W; Initial value x0, R/W; Initial value $x0_H$

B7	B6	B5	B4	B3	B2	B1	B0
--	--	--	--	P1DR3	P1DR2	P1DR1	P1DR0

2.2 Port P 1 Data Direction Control Register (P 1DCR; $27); R/W; Initial value $x0_H$

B7	B6	B5	B4	B3	B2	B1	B0
--	--	--	--	P1DCR3	P1DCR2	P1DCR1	P1DCR0

Table 2: Port P1 Configuration

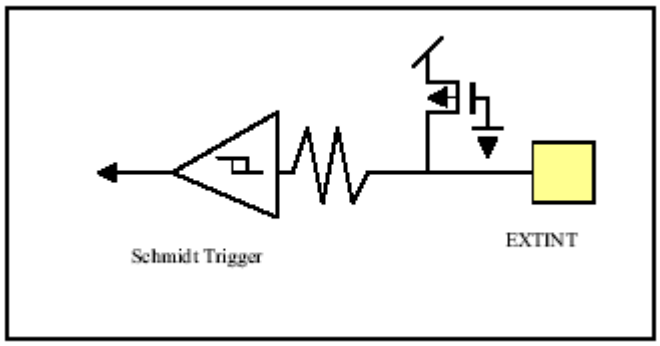
P0DCR0 ~ 7	P0DR0 ~ 7	I/O	Pull-up	Results
0	0	In	No	Tri-state (Hi-Z)
0	1	In	Yes	P10 ~ P17 with pull-up resistor (MOS) (NOTE)
1	0	Output	No	Output “0”
1	1	Output	No	Output “0”

< 3 > PORTSEL ($11); R/W; Initial X0H

B7	B6	B5	B4	B3	B2	B1	B0
--	--	--	--	--	P1LCD	P1PWM1	P1PWM0

B7~B3: Reserved
B2: P1LCD; LCD commons/V_{LCD} or I/Os select; 0: I/Os, 1: LCD commons/ V_{LCD})
B1: P1PWM1; PWM1 or I/O select; 0: I/O, i:PWM1 output
B0: P1PWM0; PWM0 or I/O select; 0: I/O, 1 :PWM0 output

< 4 > EXTINT Input Pads



< 5 > NMI Source

INT 1 from T/C 1

< 6 > INT Sources

- INT0 from T/CO
- INT 1 from T/C 1
- FQL INT
- FQH INT
- A/D conversion completion interrupt
- EXTINT (rising edge)

[2] CLOCK SOURCE

CPU clock from RC oscillator: CLKSEL pin is connected to VDD
CPU clock from Crystal oscillator: CLKSEL pin is connected to GND

[3] TIMER/COUNTERS

CRYC register ($05); Oscillator control
B3-B0:R/W

B7	B6	B5	B4	B3	B2	B1	B0
--	--	--	RES/NORES	WUT1	WUT0	CRYST/PSM	ENAB

B0: ENAB; 0: enable (default), 1: disable
Note: b0 is set to 1 in normal operation, and can be set to 0 to stop the crystal (sleep mode)

B1: CRYST/PSM; 0: crystal starts (default), 1: power saving mode
Note: While crystal is being started (strong current mode), bl is set to 0; once it starts, b 1 can be set to 1 in order to switch the crystal from "strong current mode" to "weak current mode" for power saving

B3: B2: WUT1: WUT0 (set the warm-up time at release of the hold operating mode)

00: 2^{18}/fc …… 65.5 ms (when fc=4MHz)
01: 2^{14}/fc …… 4.1 ms (when fc=4MHz)
10: reserved
00: 2^{6}/fc …… 16 μ s (when fc=4MHz)

B4: RES/NORES; 0: go through reset process, 1: without going through reset process

3.1 Timer/counters interrupt sources

INTC Register ($06); Interrupt control command register; R/W

Read: Read interrupt flag

B7	B6	B5	B4	B3	B2	B1	B0
--	ADCI	FQHINT	EXTINT	T/C1NMI	T/C1INT	T/C0INT	FQLINT

Write: Interrupt enable/disable control

B7	B6	B5	B4	B3	B2	B1	B0	FUNCTION
*	*	*	*	*	*	*	1	Low frequency interrupt enable
*	*	*	*	*	*	*	0	Low frequency interrupt disable & clear
*	*	*	*	*	*	1	*	T/CO INT0 interrupt enable
*	*	*	*	*	*	0	*	T/CO INT0 interrupt disable & clear
*	*	*	*	*	1	*	*	T/C1 INT1 interrupt enable
*	*	*	*	*	0	*	*	T/C1 INT1 interrupt disable & clear
*	*	*	*	1	*	*	*	T/C1 NMI interrupt enable
*	*	*	*	0	*	*	*	T/C1 NMI interrupt disable & clear
*	*	*	1	*	*	*	*	External interrupt (EXTINT)enable
*	*	*	0	*	*	*	*	External interrupt disable & clear
*	*	1	*	*	*	*	*	High frequency interrupt enable
*	*	0	*	*	*	*	*	High frequency interrupt disable & clear
*	1	*	*	*	*	*	*	A/D converter interrupt enable (hold & conversion start)
*	0	*	*	*	*	*	*	A/D converter interrupt disable & clear (sampling start)

3.2 TIMER/COUNTERS

WT5053 has two 16-bit timer/counters, namely T/CO and T/C 1, one low-frequency timer, and one high-frequency timer. Both T/C0 and T/C1 can be used as either a timer or a counter, and T/C 1 has auto-reload capability

IN COUNTER MODE

If T/C0 (T/C1) is used as an internal counter, by loading zero into register T/C0H (T/C1H) and T/C0L (T/C1L), the user can

reset the timer. When the specified timer is activated, the count value can be read from registers T/C0H (T/C 1 H) & T/C0L (T/C1L) by reading registers T/C0H (T/C1H) and then registers T/C0L (T/C1L) will be latched automatically. While writing registers T/C0H (T/C1H) and T/C0L (T/C1L), the register T/C0L (T/C1L) must be written first and then followed by writing T/C0H (T/C1H). To guarantee correct counting, it is not allowed to write ONLY either register T/C0H (T/C1H) or T/C0L (T/C1L).

Registers for loading T/C0 & 1 16 bit data

LDT/C0 ($0A); Write	Load (&latch) T/C0 16-bit data
LDT/C1 ($0D); Write	Load (&latch) T/C1 16-bit data

T/C0 &1 16-bit data locations

	High Byte Data (D15 - D8)	Low Byte Data ($D_7 – D_0$)
T/C0	T/COH ($0B); b7- b0	T/COL ($0C); b7 – b0
T/C1	T/C1H ($0E); b7 ~b0	T/C1L ($0F); b7 ~ b0

TMC Register ($07); Timer control register, Write

B7	B6	B5	B4	B3	B2	B1	B0
T1AUTO	T1TCS2	T1TCS1	T1TCS0	--	T0TCS2	T0TCS1	T0TCS0

B3: reserved

B7: T/C1 Auto-reload selection (can be stop on-the-fly)

"0": disable; "1": enable

B2 ~ B0: T/C0 timer sources and timer/counter mode selection

T/C1 Clock Source Table

T0TCS2	T0TCS1	T0TCS0	Mode	Selected Source
0	0	0	Timer	CPU Clock (T)
0	0	1	Timer	T/4
0	1	0	Timer	T/8
0	1	1	Timer	T/16
1	0	0	Timer	T/32
1	0	1	Timer	T/64
1	1	0	Timer	T/128
1	1	1	Timer	External counter (ETC0)

B6 ~ B4: T/C 1 timer sources and timer/counter mode selection

T/C1 Clock Source Table

T1TCS2	T1TCS1	T1TCS0	Mode	Selected Source
0	0	0	Timer	CPU Clock (T)
0	0	1	Timer	T/4
0	1	0	Timer	T/8
0	1	1	Timer	T/16
1	0	0	Timer	T/32
1	0	1	Timer	T/64
1	1	0	Timer	T/128
1	1	1	Timer	External counter (ETC0)

IN TIMER MODE

In regular timer mode, T/C0 and T/C1 can be re-loaded and always counts down from the value set by the user. If the specified bit is enabled in INTC register ($06) and the timer counts down from the value set by the user toward 0000_H, then once it hits 0000_H and becomes underflow, an interrupt signal will be generated. The value set by the user will be re-loaded to the timer automatically, and, again, the timer counts down from the value set by the user toward 0000_H

T/C1 IN PWM MODE

When the PWM mode is selected, T/C1 incorporated with the output compare registers OCR10 and OCR11 performs a dual 8, 9 or 10-bit, free-running, glitch-free and phase correct PWM with outputs on the P10/PWM0 and P11/PWM1 pins. The PWM output frequency is depends on the resolutions, i.e., 8, 9, or 10-bit, and the OSC frequency, F_{0SC}. Referring to Table 5 for more detail.

In this mode T/C 1 acts as an up/down counter, counting up from 0000_H to MAX and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the 10 least significant bits (for 10-bit PWM case) of OCR10 or OCR11, the P10 (PWM0) / P11 (PWM1) pins are set or cleared according to the setting of the CPA0 or CPB0 bits in the T/C1 control register TCCR10.

Write procedure for PWM operation should be OCR10L ($2B) first, followed by OCR10H ($2A), and then finally TCCR10($10).

TCCR10 ($10); R/W; Initial value 00_H

B7	B6	B5	B4	B3	B2	B1	B0
--	CPA0	--	CPB0	--	--	PWMS1	PWMS0

PWMS1	PWMS0	Description
0	0	PWM function is disable (default)
0	1	T/C 1 is an 8-bit PWM
1	0	T/C 1 is a 9-bit PWM
1	1	T/C 1 is a 1 O-bit PWM

CPA0/CPB0	Results on PWM0/PWM1
0	Up counting and output is cleared when compare match. Down counting and output is set when compare match
1	Down counting and output is cleared when compare match. Up counting and output is set when compare match

Table 5: The relationship between the PWM output frequency and its resolution

PWM Resolution	Timer MAX value	Frequency
8-bit	$00FF	Fosc/512
9-bit	$01FF	Fosc/1024
10-bit	$03FF	Fosc/2048

OCR1 OH ($2A)/OCR 10L($2B); T/C 1 output compare register; RJW; Initial value 00_H

OCR10H	B7(MSB)	B6	B5	B4	B3	B2	B1	B0
OCR10L	B7	B6	B5	B4	B3	B2	B1	B0(LSB)

OCR11H ($2C)/OCR11L ($2D); T/C1 output compare register; R/W; Initial value 00_H

OCR10H	B7(MSB)	B6	B5	B4	B3	B2	B1	B0
OCR10L	B7	B6	B5	B4	B3	B2	B1	B0(LSB)

To avoid the false counting of the PWM pulse in the event of abnormal OCR10/OCR11 write (glitch case), the OCR10/OCRllcontents while being written, are copied to a temporary location and are latched when T/C1 reaches the value MAX.

Note: The value in OCR10/OCRll can NOT be 0000_H or MAX; The minimal value is 0001_H n and the maximal value is MAX-1.

WDTMR register ($12)

Watchdog timer must reset within TWDT seconds; otherwise the system will be reset

B7	B6	B5	B4	B3	B2	B1	B0
FQHS2	FQHS1	FQHS0	WDTCS	WDTEN	WDTS2	WDTS1	WDTS0

B2:B0: Watchdog timer or FQL output frequencies select (f_{WDT})

WDTS2	WDTS1	WDTS0	Output Frequency (f_{WDT}) @ OSC=4MHz
0	0	0	OSC1/217 (0.25Hz)
0	0	1	O8C1/216 (0.5Hz)
0	1	0	OSC1/2is (1.0Hz)
0	1	1	OSC1/214 (2.0Hz)
1	0	0	OSC1/213 (4.0Hz)
1	0	1	OSC1/212 (8.0Hz)
1	1	0	OSC1/2u (16.0Hz)
1	1	1	OSC1/2t~ (32.0Hz)

Where OSC 1=OSC/2^7, so when OSC=4MHz then OSC l=32KHz

B3: WDTEN: Watchdog timer/FQL select; 1: watchdog enable & FQL disable,
0:watchdog disable & FQL enable

B7:B5: FQS2-FQH0; FQH output frequencies select

FQHS2	FQHS1	FQHS0	Output Frequency (f_{WDT}) @ OSC=4MHz
0	0	0	OSC1 (32kHz)
0	0	1	OSC1/2 (16kHz)
0	1	0	OSC1/22 (8kHz)
0	1	1	OSC1/23 (4kHz)
1	0	0	OSC1/24 (2kHz)
1	0	1	OSC1/25 (lkHz)
1	1	0	OSC1/26 (512Hz)
1	1	1	OSC1/2? (256Hz)

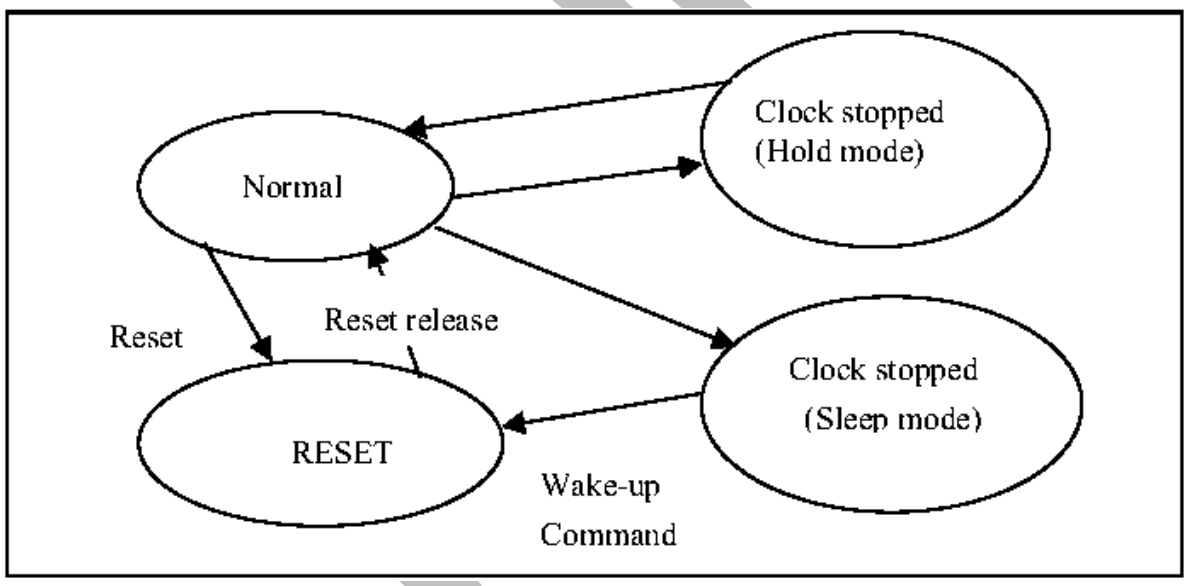
[4] MEMORY

The following figure shows the location of memory mapping

CPU ADDRESS	
$0000-$002D	I/O register
$002E-$007F	Reserved
$0080-$00FF	SRAM & STACK (page0)
$0100-$01FF	Reserved
$0200-$DFFF	Reserved
$F000 $FFFF	Program ROM

[5] CLOCK MODES

For portable battery-powered applications, stand-by mode is required for saving power. In this chip, by writing the SLPST register ($09), user can stop the CPU clock such that CPU goes to stand-by mode.
The wake-up sources can be enable by setting the SLWC register ($08) (there are two sources in this chip, namely PO0 and FQL wake-ups). After receiving a wake-up signal, the CPU is reset.



SLWC register ($08); Sleep/wake-up control register; R/W

B7	B6	B5	B4	B3	B2	B1	B0
*	*	*	*	*	*	P00SC	FQLTBI

b1: P00SC: P00 keyboard state change
0: wake-up disable; 1: wake-up enable
b0: FQLTBI: FQL time base interrupt
0: wake-up disable; 1: wake-up enable

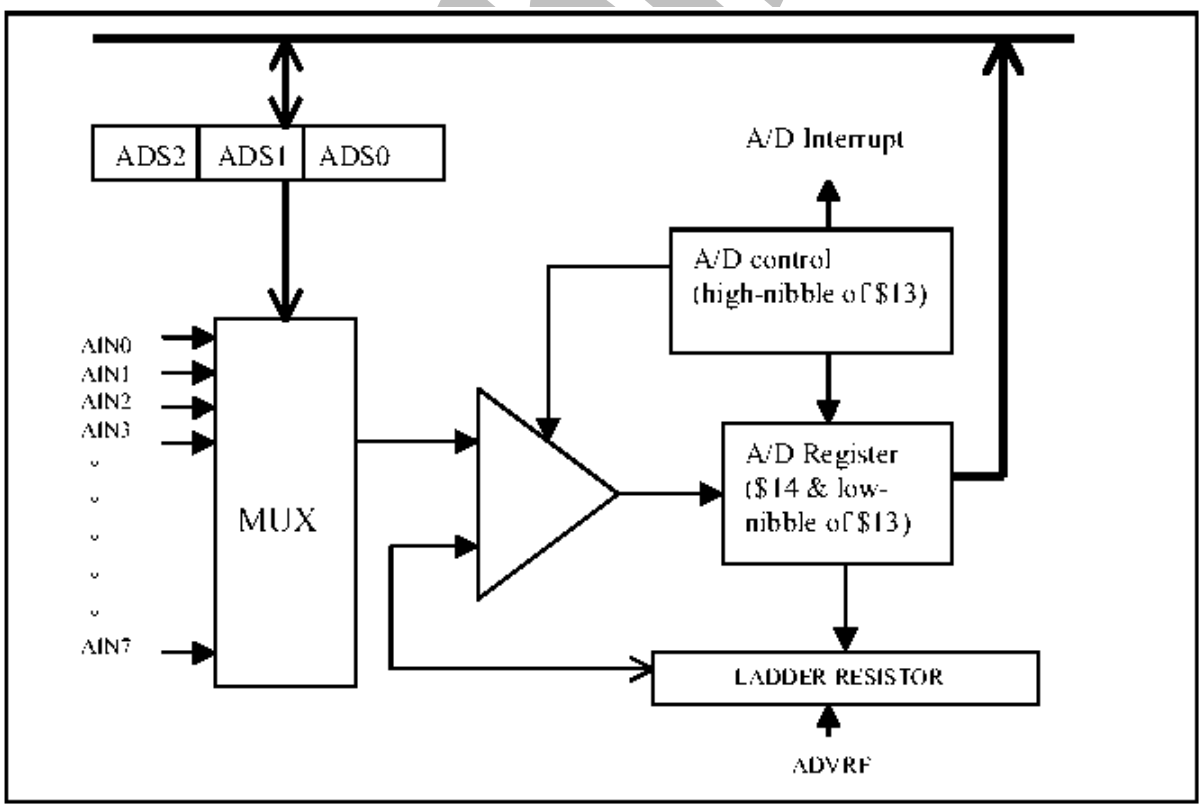
SLPST register ($09), Write
Write: Sleep start

To get into sleep mode, the program should be written as below(two consecutive instructions)

```
STA   08H
STA   09H
```

[6] A/D CONVERTER

A 12-bit successive approximation method is used in this A/D converter, as shown following figure. By multiplexing method, this A/D converter can manage up to eight analog inputs. A/D conversion is started by a write operation to the analog input selection bit in the A/D control register and by selecting the analog voltage input pins. When completed, the A/D interrupt request bit in the interrupt request register is the conversion is set. The result of A/D conversion is stored in the A/D register. During A/D conversion stage, the A/D register must not be read, otherwise incorrect value may be obtained.



ADCR ($13): A/D control register;

b7: A/D On/Off control;

b7=0, A/D Off(default); b7=l, A/D On (write)

b3: b0: High-nibble of A/D data

B7	B6	B5	B4	B3	B2	B1	B0
ADON	CKS1	CKS0	--	B3	B2/ADS2	B1/ADS1	B0/ADS0

CKS1	CKS0	Input Clock Selection
0	0	Φ o/4(when CPU clock is 1MHz, this option is recommended)
0	1	Φ o/8 (when CPU clock is 2MHz, this option is recommended)
1	0	Φ o/16 (when CPU clock is 4 MHz, this option is recommended)
1	1	Φ o/32 (when CPU clock is 8MHz, this option is recommended)

* Φ_0 represents CPU/System clock

ADS2	ADS1	ADS0	Input Selection
0	0	0	AIN0
0	0	1	AIN1
0	1	0	AIN2
0	1	1	AIN3
1	0	0	AIN4
1	0	1	AIN5
1	1	0	AIN6
1	1	1	AIN7

ADR ($14): A/D register; Low Byte of A/D data (D7-D0; note: Dll-D8 in register ADCR ($13))

[7] I/O REGISTER SUMMARY

NAME	ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
P0DR	00	R/W	P0DR7	P0DR6	P0DR5	P0DR4	P0DR3	P0DR2	P0DR1	P0DR0
P1DR	01	R/W	--	--	--	--	P1DR3	P1DR2	P1DR1	P1DR0
Reserved	02	--	--	--	--	--	--	--	--	--
Reserved	03	--	--	--	--	--	--	--	--	--
Reserved	04	--	--	--	--	--	--	--	--	--
CRYC	05	R/W	--	--	--	RES/ NORES	WUT1	WUT0	CRYST/ PSM	ENAB
INTC	06	R/W	--	ADCI	FQHINT	EXTINT	T/C1NM I	T/C1NM I	T/C0IN T	FQLINT
TMC	07	W	T1AUTO	T1TCS2	T1TCS1	T1TCS0	--	T0TCS2	T0TCS1	T0TCS0
SLWC	08	R/W	--	--	--	--	--	--	P00SC	FQLTBI
SLPST	09	W	--	--	--	--	--	--	--	--
LDT/C0	0A	W	--	--	--	--	--	--	--	--
T/C0H	0B	R/W	B7	B6	B5	B4	B3	B2	B1	B0
T/C0L	0C	R/W	B7	B6	B5	B4	B3	B2	B1	B0
LDT/C1	0D	W	--	--	--	--	--	--	--	--
T/C1H	0E	R/W	B7	B6	B5	B4	B3	B2	B1	B0

T/C1L	0F	R/W	B7	B6	B5	B4	B3	B2	B1	B0
TCCR10	10	R/W	--	CPA0	--	CPB0	--	--	PWMS1	PWMS0
PORTSEL	11	R/W	--	--	--	--	--	P1LCD	P1PWM 1	P1PWM 0
WDTMR	12	W	--	--	--	--	WDTEN	WDTS2	WDTS1	WDTS0
ADCR	13	R/W	ADON	CKS1	CKS0	--	B3	B2/ADS 2	B1/ADS 1	B0/ADS 0
ADR	14	R	B7	B6	B5	B4	B3	B2	B1	B0
Reserved	15~25	W	--	--	--	--	--	--	--	--
P0DCR	26	R/W	P0DCR7	P0DCR6	P0DCR5	P0DCR4	P0DCR3	P0DCR2	P0DCR1	P0DCR0
P1DCR	27	R/W	--	--	--	--	--	P0DCR2	P0DCR1	P0DCR0
Reserved	28	--	--	--	--	--	--	--	--	--
Reserved	29	--	--	--	--	--	--	--		--
OCR10H	2A	R/W	B7	B6	B5	B4	B3	B2	B1	B0
OCR10L	2B	R/W	B7	B6	B5	B4	B3	B2	B1	B0
OCR11H	2C	R/W	B7	B6	B5	B4	B3	B2	B1	B0
OCR11L	2D	R/W	B7	B6	B5	B4	B3	B2	B1	B0

[8] ELECTRICAL CHARACTERISTICS

ABS0LUTE MAXIMUM RATINGS (VSS=0V)

PARAMETER	SYMBOL	RATING	UNIT
DC SupplyVoltage	VDD	< +7	V
Input Voltage Range	Vin	-0.5 - VDD+0.5	V
Operating Temperature	Topr	0 ~ +70	ºC
Storage Temperature	Tstg	-50 - +150	ºC

ELECTRICAL CHARACTERISTICS (VSS=0 V, T_{opr} = 0 to 70 ºC

PARAMETER	SYMBOL	Min.	Typ.	Max.	Unit	CONDITIONS
Operating Voltage	VDD	2.4	--	5.5	V	
Operating Current	I_{OP}			2	mA	OSC 4MHz ~ 5.0V
Standby Current	I_{STB}		--	1.0	μA	VDD=5.0V
OSC Frequency	F_{OSC}			8.0	MHz	VDD=5.0V
Input High Level	V_{IH}	4.0 2.5			V	VDD=5.0V VDD=3.0V
Input Low Level	V_{IL}			0. 8 1. 0.5	V	VDD=5.0V VDD=2.0V
P04-P07 & Port 1 Output High I (I/O)	I_{OH}	10			mA	VDD=5.0V Voh=4.0V
P04-P07 & Port 1 Output Sink I (I/O)	I_{OL}	20			mA	VDD=5.0V Vol=0.8V
CPU Clock	F_{CPU}	0.03		8.0	MHz	$F_{CPU}=F_{OSC}$@5.0V

A/D CONVERSION CHARACTERISTICS (Topr = 0 to 70 ºC)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT

Analog Reference Voltage	AD_{VPF}		2.5	--	AV_{DD}	V
Valid Voltage Range	V_{RNG}	AD_{VRF}=5V	0.5		4.0	V
Valid Voltage Range	V_{RNG}	AD_{VRF}=3V	0.5		2.0	V
Analog Input Voltage	AV_{IN}		AV_{SS}		AV_{DD}	V
Analog Supply Current	I_{REF}		--	0.5	1	mA
Input Impedance	Z			230		KΩ
Differential nonlinear error[1]	E_{NL}				±1	LSB
Integral nonlinear error[2]	E_{INL}				±2	LSB
Offset error[3]	E_{OS}				±2	LSB
Absolute Error[4]	E_{ABS}	VDD=5V, V_{SS}=0V AD_{VRF}=5V, AV_{SS}=0V	--		±3	LSB
Conversion Time	T_{CV}		--		30	μS

1. The differential nonlinear error (E_{NL}) is the step width difference of the actual and the ideal transfer curves.
2. The integral nonlinear error (E_{INL}) is the peak difference between the centers of the actual and the ideal transfer curves.
3. The offset error (E_{OS}) is the absolute difference of the straight lines, which fit the actual and the ideal transfer curves
4. The absolute error (E_{ABS}) is the maximum difference between the center of the steps of the actual and the ideal transfer curves for a non-calibrated ADC.