DESCRIPTION

The WT5041 is a high-performance, low-cost, CMOS 8-bit single-chip micro controller with on-chip OP Amp (OPA) for heart rate detect and 128 segments LCD driver. This chip can be used dedicate for applications where heart rate and LCD display are required, for example sports bicycle meter, heart rate meter and heart rate watch.

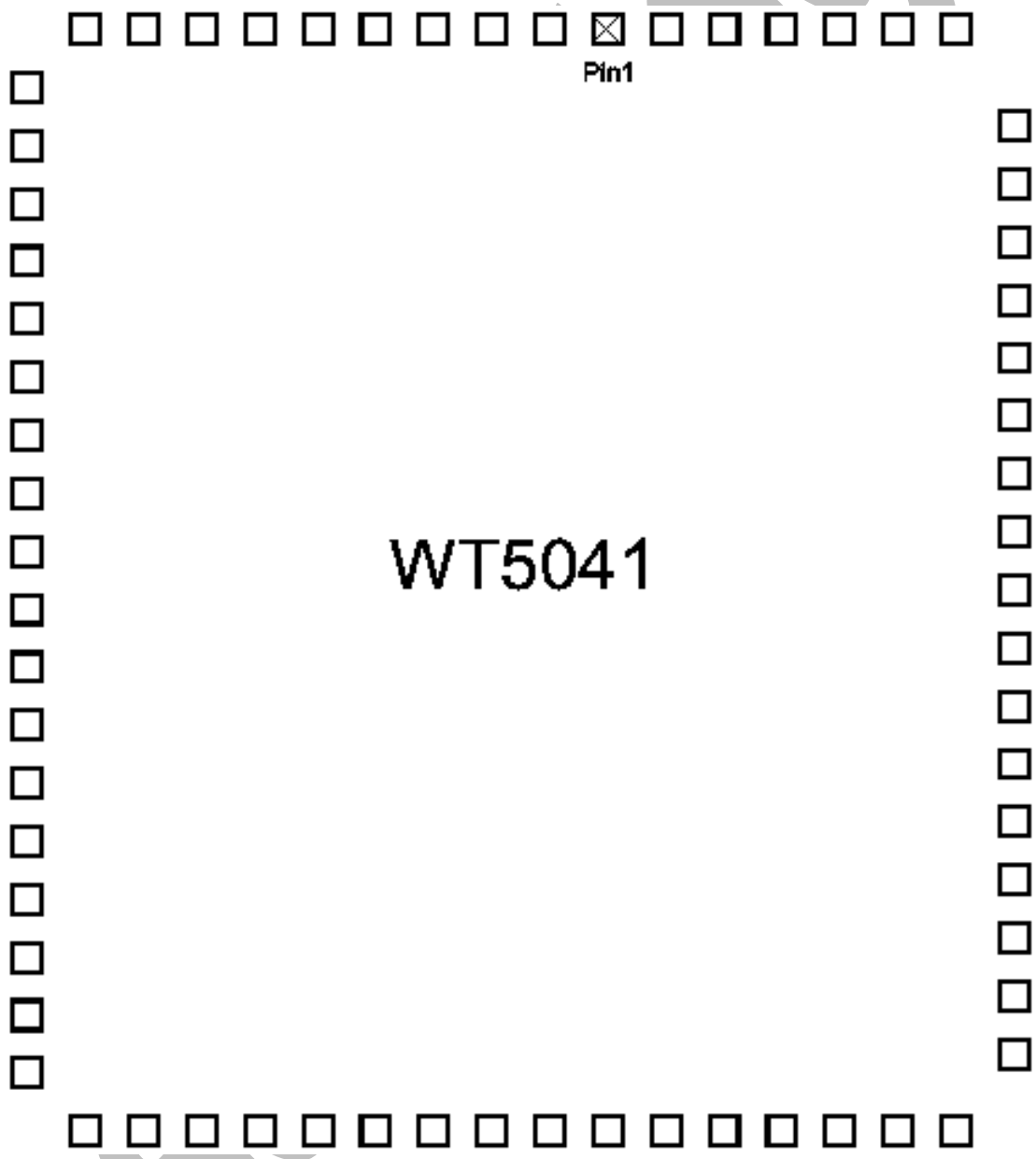
This chip has 8-bit CPU, RAM, ROM, I/Os, one 16-bit timer/counters, dual 8-bit timer interrupt controller, three 8-bit PWM D/A output, resister to frequency converter (RFC), heart rate detect circuits, and a LCD driver. To be suitable for portable battery-powered applications, a power saving function is included.

FEATURES

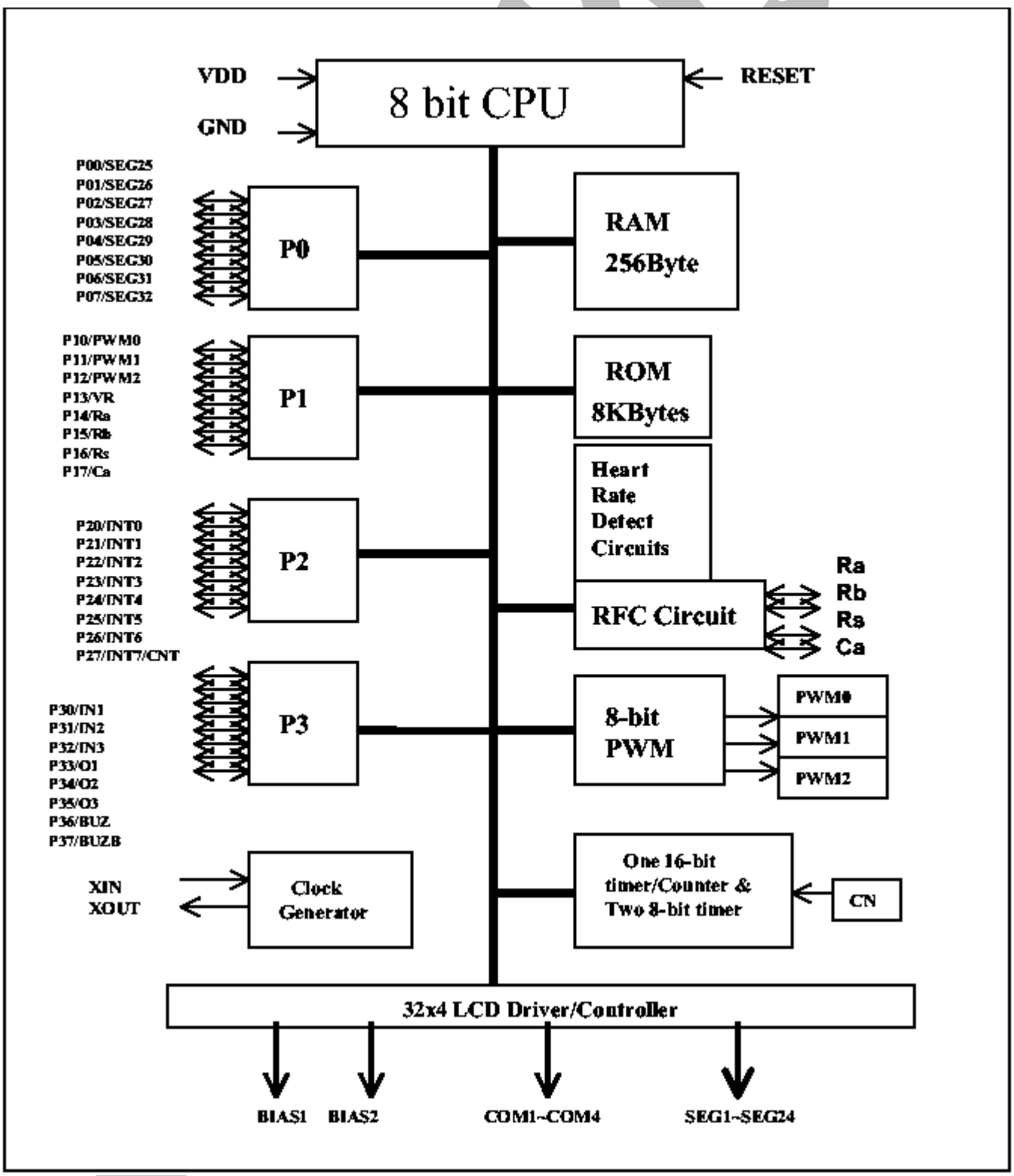
- 8-bit single chip micro controller with 8Kbytes ROM and 256 Bytes SRAM
- Wide voltage operating range from 2.4 V to 5.5 V
- Built-in 32.768KHz OSC circuits.
- 14 interrupt sources, 14 halt mode release sources (warm start), 8 off mode wake up sources (cold start); all sources have independent latches each and multi-control is available.
- I/O port (32 pins)
  - ✧ I/O porto 8 pins (shared with SEG25-SEG32)
  - ✧ I/O port1 1 pin (shared with OP Amp 1 pins)
  - ✧ I/O port1 3 pins (shared with PWM0~2 output)
  - ✧ I/O port1 4 pins (shared with RFC 4 pins)
  - ✧ IlO port2 8 pins (shared with key detect & event counter
  - ✧ I/O port3 6 pins (shared with OP Amp 6 pins)
  - ✧ I/O port3 2 pins (shared with BUZ/BUZB output)

  ~ Providing standby mode
- Key wake up function
- Build-in heart rate detect circuits and one 16-bit counter
- Build-in RFC circuit and one 16-bit counter for thermistor and humidity sensor use.
- Dual 8-bit timer & one 16-bit timedcounters
- 3 Channel 8-bit PWM output
- LCD driver
  - LCD direct drive (max. 16-digit display at 1/4 duty)
  - 1/4, 1/3, 1/2 duties and 1/2, 1/3 biases can be selected by software programming
  - 1/4, 1/3, 1/2 duties and 1/2, 1/3 biases can be selected by software programming
- LCD segments SEG25~32 can be used as 8 I/O pins by software programming
- Real-time emulator
- Package: Die form

PAD LAYOUT



BLOCK DIAGRAM



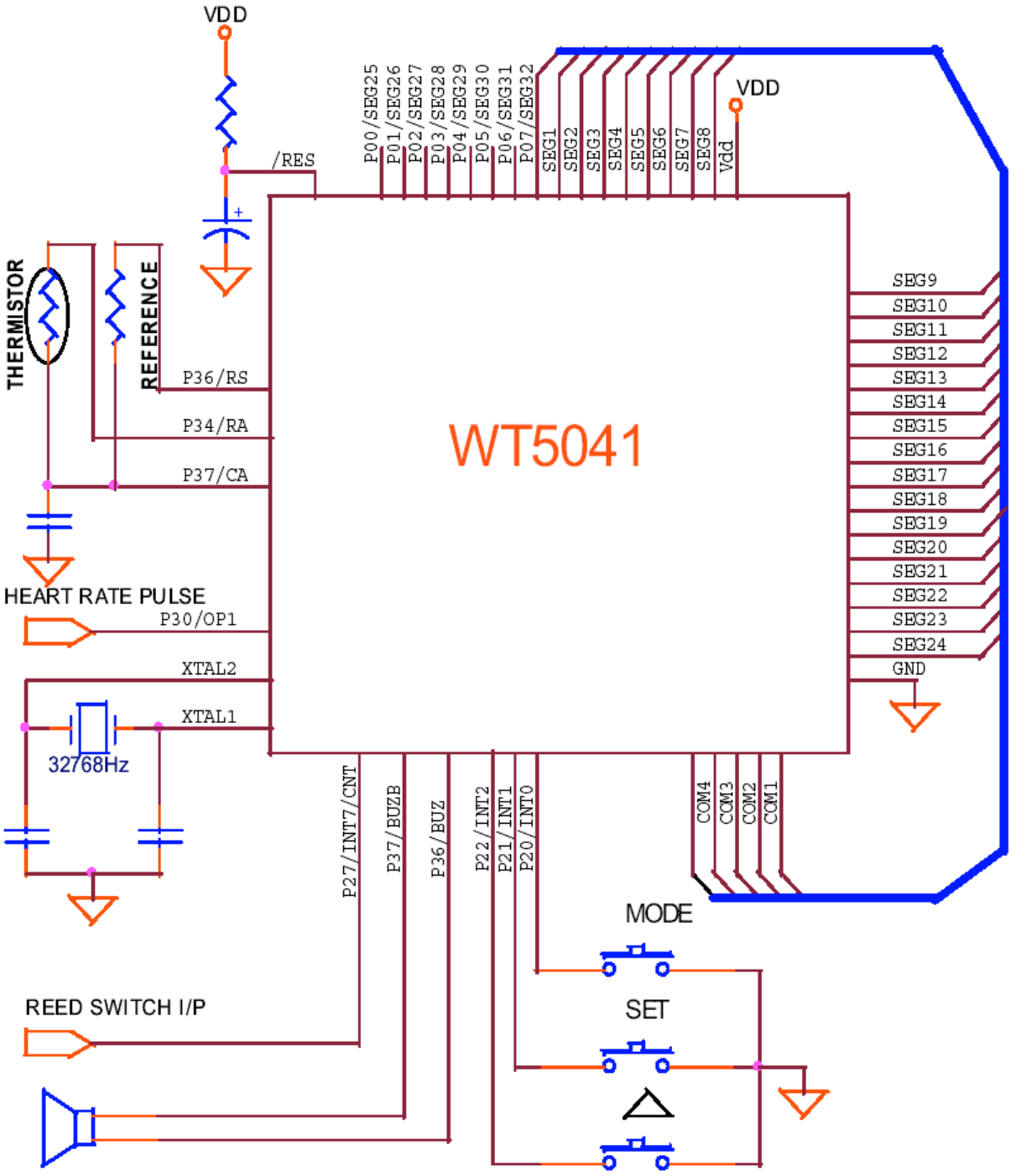
PIN FUNCTION

Name	No.	I/O	Description
COM1	1	O	LCD common1
COM2	2	O	LCD common2
COM3	3	O	LCD common3
COM4	4	O	LCD common4
SEG1	5	O	LCD segment1
SEG2	6	O	LCD segment2
SEG3	7	O	LCD segment3
SEG4	8	O	LCD segment4
SEG5	9	O	LCD segment5
SEG6	10	O	LCD segment6
SEG7	11	O	LCD segment7
SEG8	12	O	LCD segment8
SEG9	13	O	LCD segment9
SEG10	14	O	LCD segment10
SEG11	15	O	LCD segment11
SEG12	16	O	LCD segment12
SEG13	17	O	LCD segment13
SEG14	18	O	LCD segment14
SEG15	19	O	LCD segment15
SEG16	20	O	LCD segment16
SEG17	21	O	LCD segment17
SEG18	22	O	LCD segment18
SEG19	23	O	LCD segment19
SEG20	24	O	LCD segment20
SEG21	25	O	LCD segment21
SEG22	26	O	LCD segment22
SEG23	27	I/O	LCD segment23
SEG24	28	I/O	LCD segment24
P00/SEG25	29	I/O	I/O port 00 or LCD segment 25
P01/SEG26	30	I/O	I/O port 01 or LCD segment 26
P02/SEG27	31	I/O	I/O port 02 or LCD segment 27
P03/SEG28	32	I/O	I/O port 02 or LCD segment 28
P04/SEG29	33	I/O	I/O port 04 or LCD segment 29
P05/SEG30	34	I/O	I/O port 05 or LCD segment 20
P06/SEG31	35	I/O	I/O port 05 or LCD segment 31
P07/SEG32	36	I/O	I/O port 07 or LCD segment 32
P30/IN1	37	I/O	I/O port 30 or OP function Input1
P31/IN2	38	I/O	I/O port 31 or OP function Input2
P32/IN3	39	I/O	I/O port 32 or OP function Input3
P33/O1	40	I/O	I/O port 33 or OP function Output1
P34/O2	41	I/O	I/O port 34 or OP function Output2
P35/O3	42	I/O	I/O port 35 or OP function Output3
P36/BUZ	43	I/O	I/O port 36 or OP function Output3
P37/BUZB	44	I/O	I/O port 37 or BUZZERB function
P20/INT0	45	I/O	I/O port 20 or INT/wake up input 0 pull high.negative edge trigger.

P21/INT1	46	I/O	I/O port 21 or INT/wake up input 1 pull high.negative edge trigger.
P22/INT2	47	I/O	I/O port 22 or INT/wake up input 2 pull high.negative edge trigger.
P23/INT3	48	I/O	I/O port 23 or INT/wake up input 3 pull high.negative edge trigger.
P24/INT4	49	I/O	I/O port 24 or INT/wake up input 4 pull high.negative edge trigger.
P25/INT5	50	I/O	I/O port 25 or INT/wake up input 5 pull high.negative edge trigger.

Name	No.	I/O	Description
P26/INT6	51	I/O	I/O port 26 or INT/wake up input 6 pull high.negative edge trigger.
P27/INT6/CNT	52	I/O	I/O port 27 or INT/wake up input 7/counter input
GND	53	P	Ground (0V)
XTAL2	54	I/O	32768 Hz crystal oscillator
XTAL1	55	I	32768 Hz crystal oscillator
P10/PWM0	56	I/O	I/O port 10.or PWM0 output
P11/PWM1	57	I/O	I/O port 11.or PWM1 output
P12/PWM2	58	I/O	I/O port 12.or PWM2 output
P13/VR	59	I/O	I/O port 13. OP reference voltage output
P14/RA	60	I/O	I/O port 14 or RFC R thermistor
P15/RB	61	I/O	I/O port 15 or RFC R humidity sensor
P16/RS	62	I/O	I/O port 16 or RFC R standrad
P17/CA	63	I/O	I/O port 17 or RFC Capacitor
/RESET	64	I	Reset. Internal pull high, active low.
BIAS1	65	O	LCD bias voltage 1
BIAS2	66	O	LCD bias voltage 2
VDD	67	P	Power supply.

APPLICATION DIAGRAM



FUNCTION DESCRIPTION

[1] CPU

8-bit 6502 compatible

[2] RAM

256 bytes RAM, address from 0080H - 00FFH and 0180H ~ 01FFH Default stack pointer is 01FFH

[3] ROM

8Kbytes ROM, address from E000H to FFFFH

Program start/reset vector (cold start): FFFCH (Iow byte) and FFFDH(high byte)

Halt state wake up vector (warm start): FFFAH (Iow byte) and FFFBH(high byte)

Interrupt vector: FFFEH (Iow byte) and FFFFH (high byte)

[4] I/O PORT

The WT5041 has 4 ports (27 pins) each as follows:

- P30 ~ P37 ; 8-bit input port (shared with OPA, BUZ & BUZB pin)
- P20 ~ P27 ; 8-bit I/O port (shared with INT0 to INT7 &/CNT pin)
- P10 ~ P17 ; 8-bit I/O port (share with PWM0,PWM1,PWM2 & RFC)
- P00 ~ P07 ; 8-bit I/O port (shared with SEG25~SEG32)

PORT 0

P00/SEG25 - I/O pin P00 & LCD segment 25

P01/SEG26 - I/O pin P01 & LCD segment 26

P02/SEG27 - I/O pin P02 & LCD segment 27

P03/SEG28 - I/O pin P03 & LCD segment 28

P04/SEG29 - I/O pin P04 & LCD segment 29

P05/SEG30 - I/O pin P05 & LCD segment 30

P06/SEG31 – I/O pin P06 & LCD segment 31

P06/SEG32 – I/O pin P06 & LCD segment 32

✧ Port P0 (P00 ~ P07)

P0 register (address $40); b7 ~ b0, Read/Write

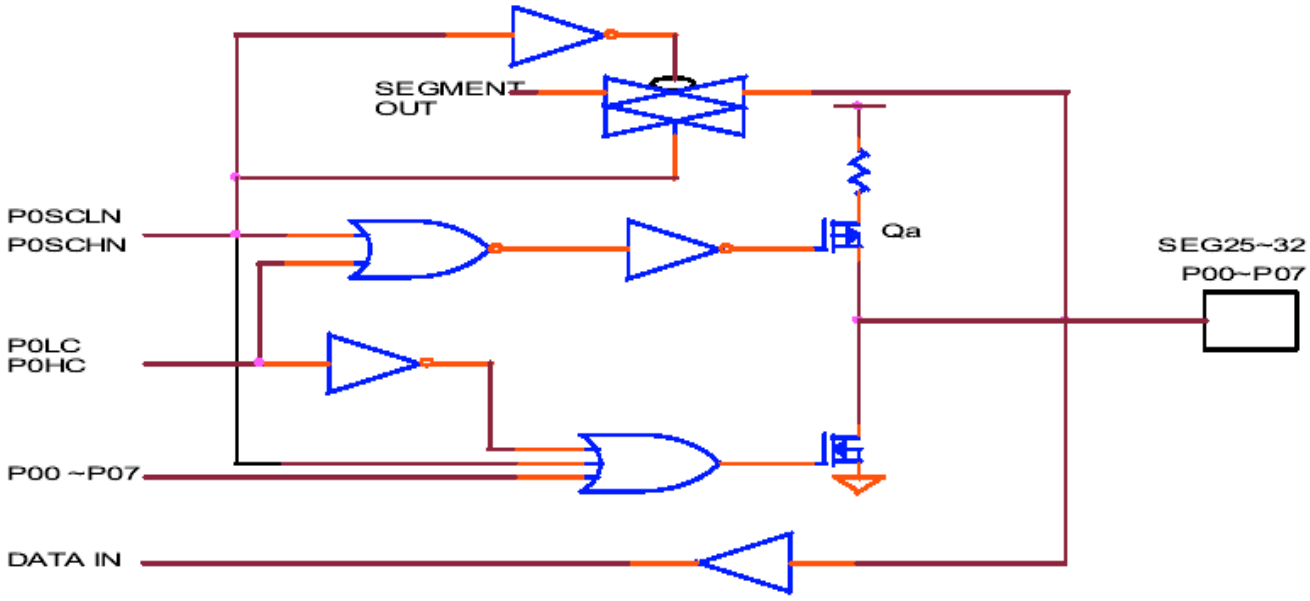
Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40H	R/W	xxxxxB	P07	P06	P05	P04	P03	P02	P01	P00

✧ Port P0 segment & I/O port control

P0C register (address $44); b3 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
44H	W	xxxx0000B	--	--	--	--	P0SCHN	P0SCLN	P0HC	P0LC

Bit Name	Bit=0	Bit=1
P0SCHN	P04 ~ P07 I/Os	P04 ~ P07 LCD segment
P0SCLN	P00 ~ P03 I/Os	P00 ~ P03 LCD segment
P0HC	P07, P06, P05, P04 input	P07, P06, P05, P04 output
P0LC	P03, P02, P01, P00 input	P03, P02, P01, P00 output
P0n(n=0~7)	Pin P0n is low level	Pin P0n is drain status



PORT 1

P10/PWM0 – I/O pin P10 & PWM0 (CMOS output)
P11/PWM1 – I/O pin P11 & PWM1 (CMOS output)
P12/PWM2 – I/O pin P12 & PWM2 (CMOS output)
P13/VR - I/O pin P13 & OPA VR (reference voltage)
P14/Ra - I/O pin P14 & thermistor sensor output for RFC Ra
P15/Rb - I/O pin P15 & humidity sensor output for RFC Rb
P16/Rs - I/O pin P16 & reference sensor output for RFC Rs
P17/Ca - I/O pin P17 & capacitor sensor output for RFC Ca

✧ Port P1 (P10 ~ P17)

P1 register (address $41); b7 ~ b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41H	R	xxxxxB	P17	P16	P15	P14	P13	P12	P11	P10

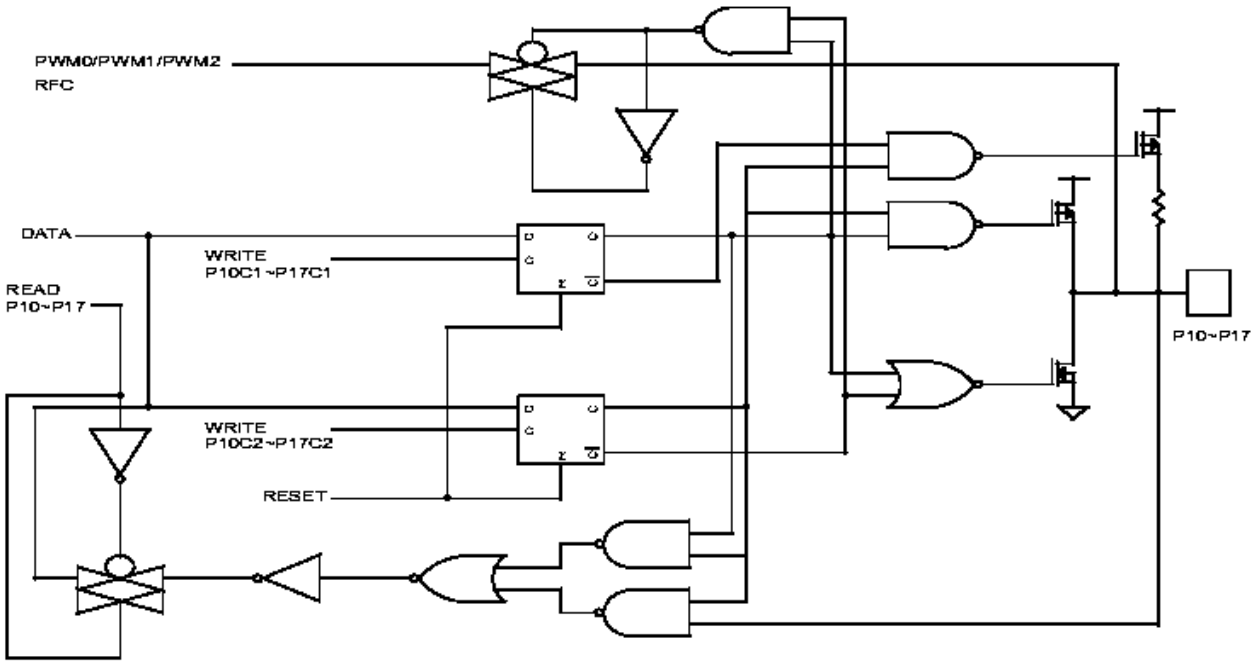
✧ Port P1 pull high control (P10C1 ~ P17C1); Port P1 I/O control (P10c2 ~ P17C2);

P0C1 register (address $45); b7 ~ b0, Write

P0C2 register (address $46); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
44H	W	xxxx0000B	--	--	--	--	P0SCHN	P0SCLN	P0HC	P0LC

Bit Name	Bit Value
P1mC2, P1mC1 (m=0~7)	P1mC2=1,P1mC1=1: P1m pin output port high level P1mC2=1,P1mC1=0: P1m pin output port low level
	P1mC2=0,P1mC1=1: P1m PWM0/PWM1/PWM2/RFC output P1mC2=0,P1mC1=0: P1m input with pull high
P1n (n=0~7)	P1n=0: Pin P1n is low level input P1n=1: Pin P1n is high level input

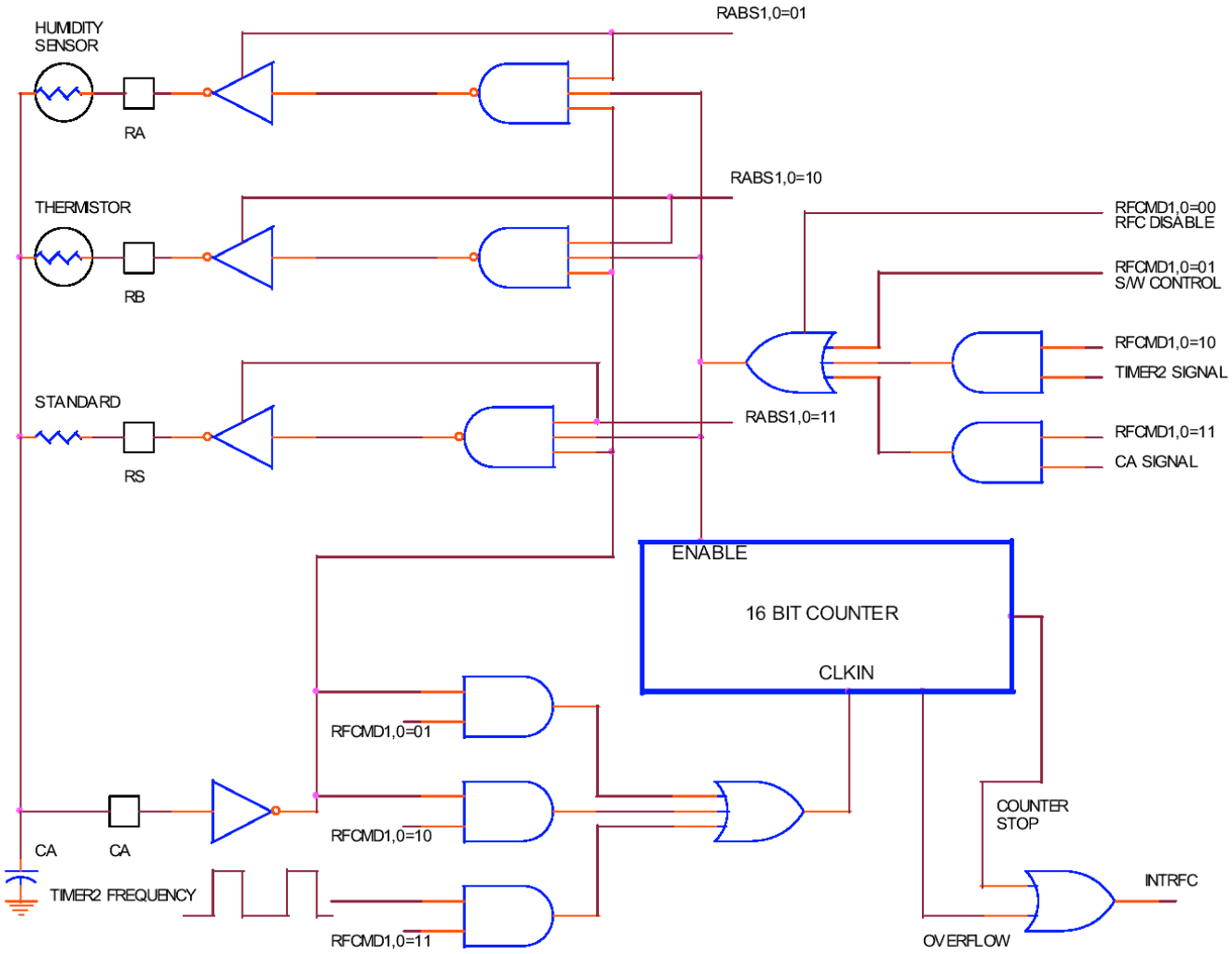


✧ RFC control (P14C1 ~ P17C1 & P14C2 ~P17C2, RFCMD1/RFCMD0,RHT1/RHT0)

RFCTL register (address $4F); b7 ~b5 & b3 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4FH	W	00000000B	WDT2	WDT1	WDT0	--	RABS1	RABS0	RFCMD1	RFCMD0

Bit Name	Bit Value (P14C2~P17C2=0 & P14C1~P17C1=1)	
RFCMD1 RFCMD0	00	Disable RFC 16 bit counter
	01	Mode 1: S/W control CA signal i/p to 16 bit counter
	10	Mode 2: Timer2 control CA signal i/p to 16 bit counter
	11	Mode 3: CA signal control Timer2 i/p to 16 bit counter
RABS1 RABS0	01	Enable RA circuit
	10	Enable RB circuit
	11	Enable RS circuit

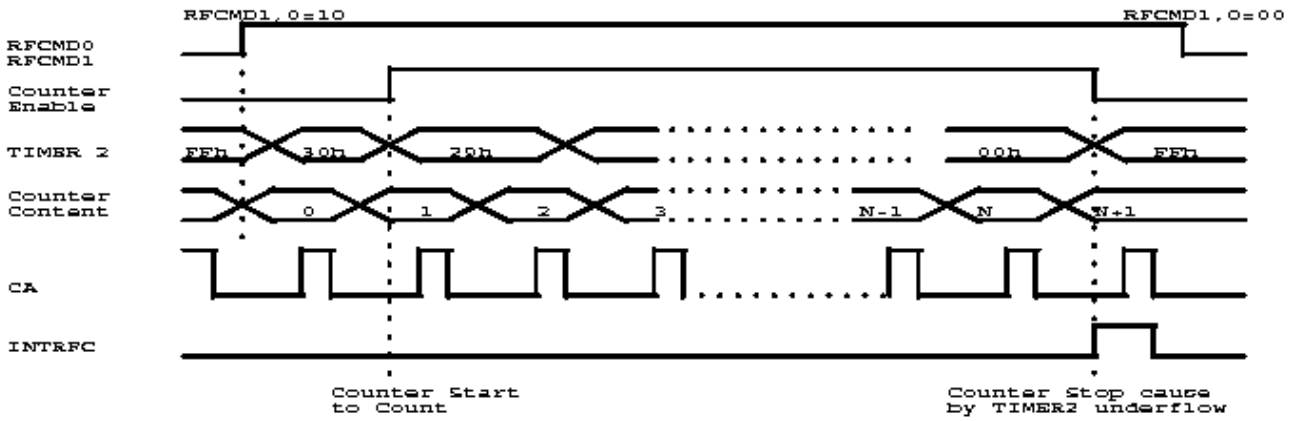


1. Model (RFCMDI=0,RFCMD0=I): Enable/Disable the counter by Software

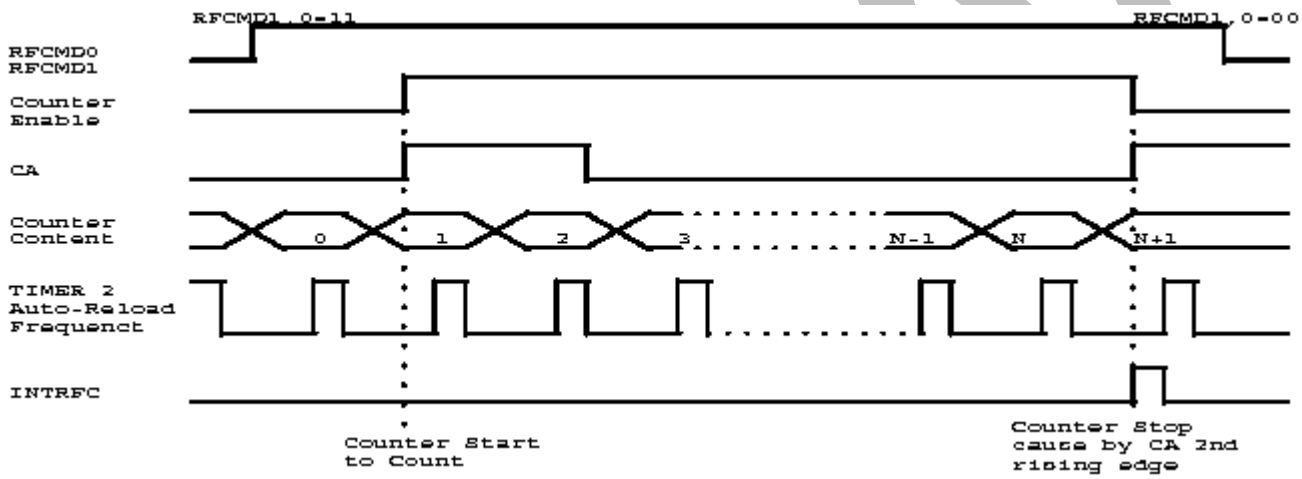
   The clock input of 16-bit counter comes from the CA pin & is enable/disable by the S/W. While set the RFCMDI=0 & RFCMD0-1 the counter start to count the pulse input from CA pin, until set the RFCMDI=0 & RFCMD0-0. If counter is overflow it will be stop automatically & INTRFC will be set to 1.

2. Mode2 (RFCMDI-1 ,RFCMD0=0): Enable/Disable the counter by Timer 2

   Timer 2 controls counter. When Timer 2 is enabled the counter start operate until Timer 2 underflow occurs.



3. Mode3 (RFCMDI:I ,RFCMD0:I): Enable/Disable the counter by CA Signal CA signal rising edge controls counter.
When 1st CA rising edge the counter start to operate until 2na CA rising edge occurs



PWM; when P1nC2=0, P1nC1=1: P1n is PWMn output function (n=0~2) Build in 8MHz (*@VDD=5V) ring oscillator
PWM frequency = 8MHz/32

PWMBUZ register (address $4B); b5 ~b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4BH	W	xx000000B	--	--	EPWM2	EPWM1	EPWM0	EVN1	EVN0	BUZ0

PWM0,PWM1,PWM2 register (address $4C,$4D,$4E); b7 ~ b0, Write

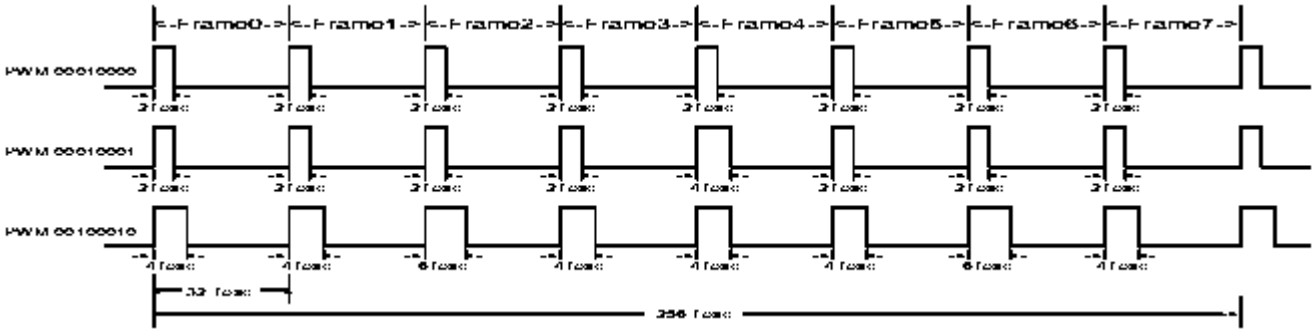
Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4CH	W	0000000B	PWM07	PWM06	PWM05	PWM04	PWM03	PWM02	PWM01	PWM00
4DH	W	0000000B	PWM17	PWM16	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10
4EH	W	0000000B	PWM27	PWM26	PWM25	PWM24	PWM23	PWM22	PWM21	PWM20

Bit Name	Bit Value
PWM07 ~ PWM00 PWM17 ~ PWM10 PWM27 ~ PWM20	Select 0/32 to 31/32 duty cycle 00000xxx: duty cycle = 0/32 00001xxx: duty cycle = 1/32 : 11110xxx: duty cycle = 30/32 11111xxx: duty cycle = 31/32
EPWM2, EPWM1, EPWM0	Enable corresponding PWM output: (PWM2, PWM1, PWM0)

The corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/32 to 31/32.
LSB 3-bit of PWM register determines which frame will be extended two Tosc.
000: no extended pulse.
001: extend two Tosc at frame 4.
010: extended two Tosc at frame 2 and 6.
011: extended two Tosc at frame 2, 4 and 6.
100: extended two Tosc at frame 1, 3, 5 and 7.
101: extended two Tosc at frame 1, 3, 4, 5 and 7.

110: extended two Tosc at frame 1, 2, 3, 5, 6 and 7.
111: extended two Tosc at frame 1,2, 3, 4, 5, 6 and

MSB 5-bit of PWM register determines 0/32 to 31/32 duty cycle in each frame.



PWM output waveform

PORT 2

P20/INT0 – I/O pin P20 & interrupt 0
P21/INT1 – I/O pin P21 & interrupt 1
P22/INT2 – I/O pin P22 & interrupt 2
P23/INT3 – I/O pin P23 & interrupt 3
P24/INT4 – I/O pin P24 & interrupt 4
P25/INT5 – I/O pin P25 & interrupt 5
P26/INT6 – I/O pin P26 & interrupt 6
P27/INT7/CNT – I/O pin P27 ,interrupt 7 & counter

✧ Port P2 (P20 ~ P27)

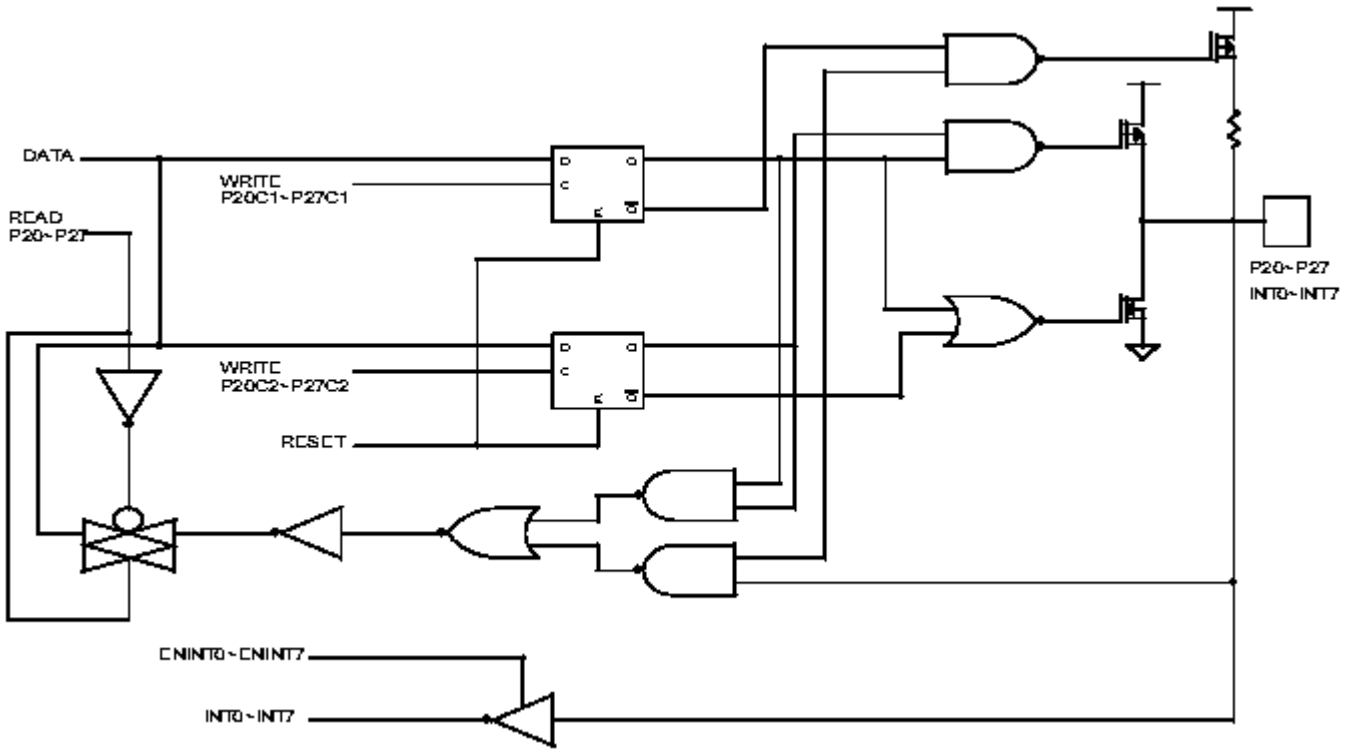
P2 register (address $42); b7 ~ b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4BH	R	xxxxxxxxB	P27	P26	P25	P24	P23	P22	P21	P20

Port P2 pull high control (address $47, $48); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
47H	W	00000000B	P27C1	P26C1	P25C1	P24C1	P23C1	P22C1	P21C1	P20C1
48H	W	00000000B	P27C2	P26C2	P25C2	P24C2	P23C2	P22C2	P21C2	P20C2

Bit Name	Bit Value
P2mC2, P2mC1 (m=0 ~ 7)	P1mC2=1,P1mC1=1: P2m pin output port high level P1mC2=1,P1mC1=0: P2m pin output port low level P1mC2=0,P1mC1=1: P2m input without pull high P1mC2=0,P1mC1=0: P2m input with pull high
P2n (n=0 ~ 7)	P1n=0: Pin P2n is low level input P1n=1: Pin P2n is high level input



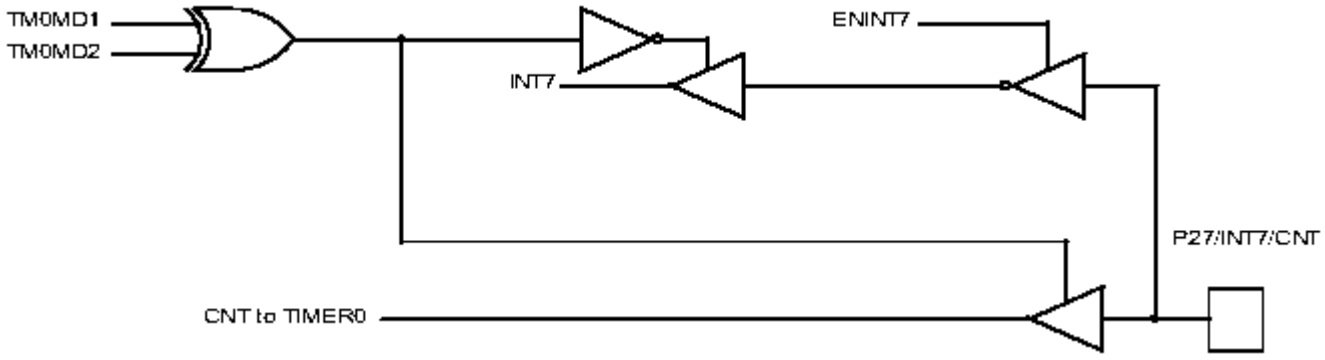
✧ INT pin control (INT7 ~ INT0)

INTEN0 register (address $54); b7 ~ b0, Write

INTFLG0 register (address $54); b7 ~ b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54H	W	00000000B	ENINT 7	ENINT 6	ENINT 5	ENINT 4	ENINT 3	ENiNT2	ENINT1	ENINT0
54H	R	00000000B	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0

Bit Name	Bit=0	Bit=1
EINTn (n:0~7)	INTn pin interrupt disable	INTn pin interrupt enable
INTn (n=0~7)	No INTn pin interrupt	INTn pin interrupt happened



PORT 3

P30/OP1N - I/O pin P30 & OP amp IN1
P31/OP2N - I/O pin P31 & OP amp IN2
P32/OP3N - I/O pin P32 & OP amp IN3
P33/OP10 - I/O pin P33 & OP amp O1
P34/OP20 -I/O pin P34 & OP amp 02
P35/OP30- I/O pin P35 & OP amp 03
P36/BUZ - I/O pin P36 & Buzzer output
P37/BUZB - I/O pin P37 & Buzzer Bar output

✧ Port P3 (P30 ~ P37)

P3 register (address $43); b7 ~ b0, Read

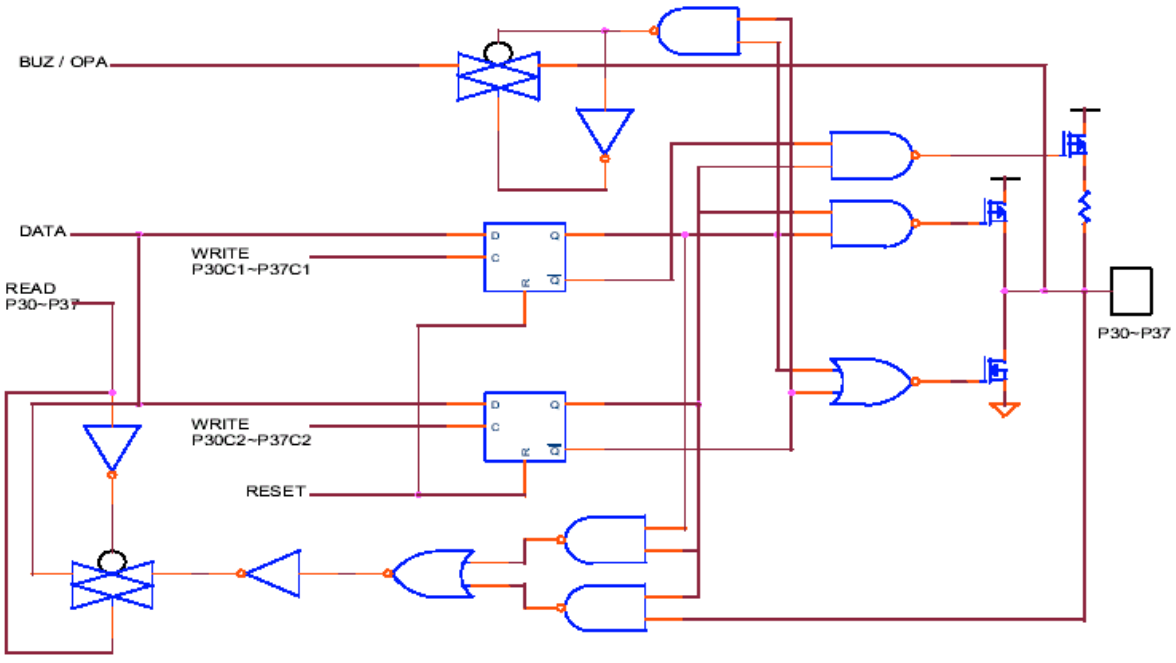
Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43H	R	xxxxxxxB	P37	P36	P35	P34	P33	P32	P31	P30

✧ Port P3 I/O control (P30C2 ~ P37C2) ; Port P3 pull high control (P30C 1 -P37C 1)

P3C1, P3C2 register (address $49, $4A); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
49H	W	00000000B	P37C1	P36C1	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
4AH	W	00000000B	P37C2	P36C2	P35C2	P34C2	P33C2	P32C2	P31C2	P30C2

Bit Name	Bit Value
P3mC2, P3mC1 (m=0-7)	P3mC2=I ,P3mC1 =1: P3m pin output high level P3mC2=I ,P3mCI=0: P3m pin output Iow level P3mC2=0,P3mCI=I: BUZ or OPA function P3mC2=0,P3mCI=0: P3m input with pull high
P3n (n=0-7)	P3n=0: Pin P3n is input Iow level P3n=l: Pin P3n is input high level



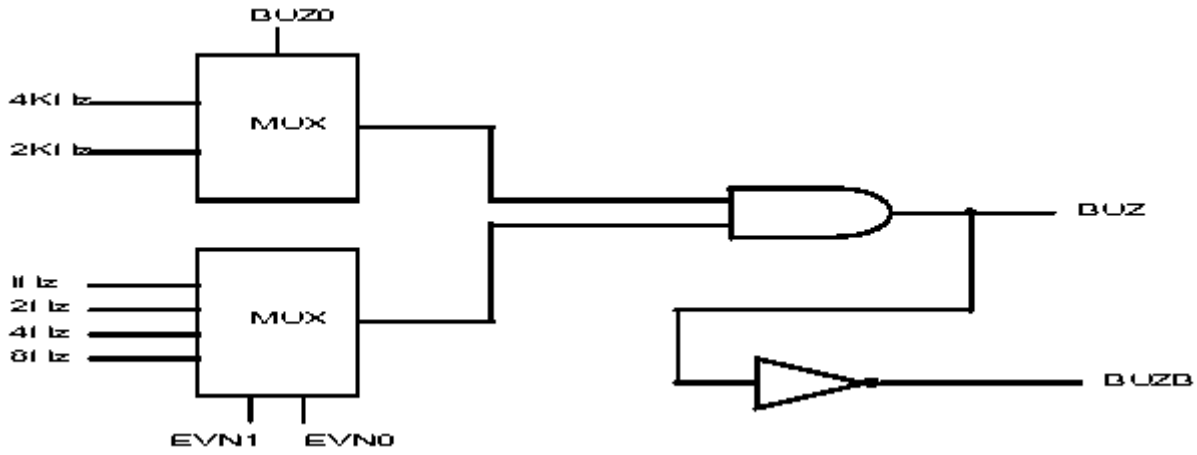
✧ BUZ; when P36C2=0, P36C1=1: P36 is buzzer output function

✧ BUZB; when P37C2=0, P37C1=1: P37 is buzzer bar output function

PWMBUZ register (address $4B); b5 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4BH	W	xxx00000B	--	--	EPWM2	EPWM1	EPWM0	EVN1	EVN0	BUZ0

Bit Name	Bit Value
BUZ0	BUZ0=0 4KHz frequency BUZ0=1 2KHz frequency
EVN1, EVN0	EVN1=0, EVN0=0 1Hz envelope EVN1=0, EVN0=1 2Hz envelope EVN1=1, EVN0=0 4Hz envelope EVN1=1, EVN0=1 Hi, no envelope

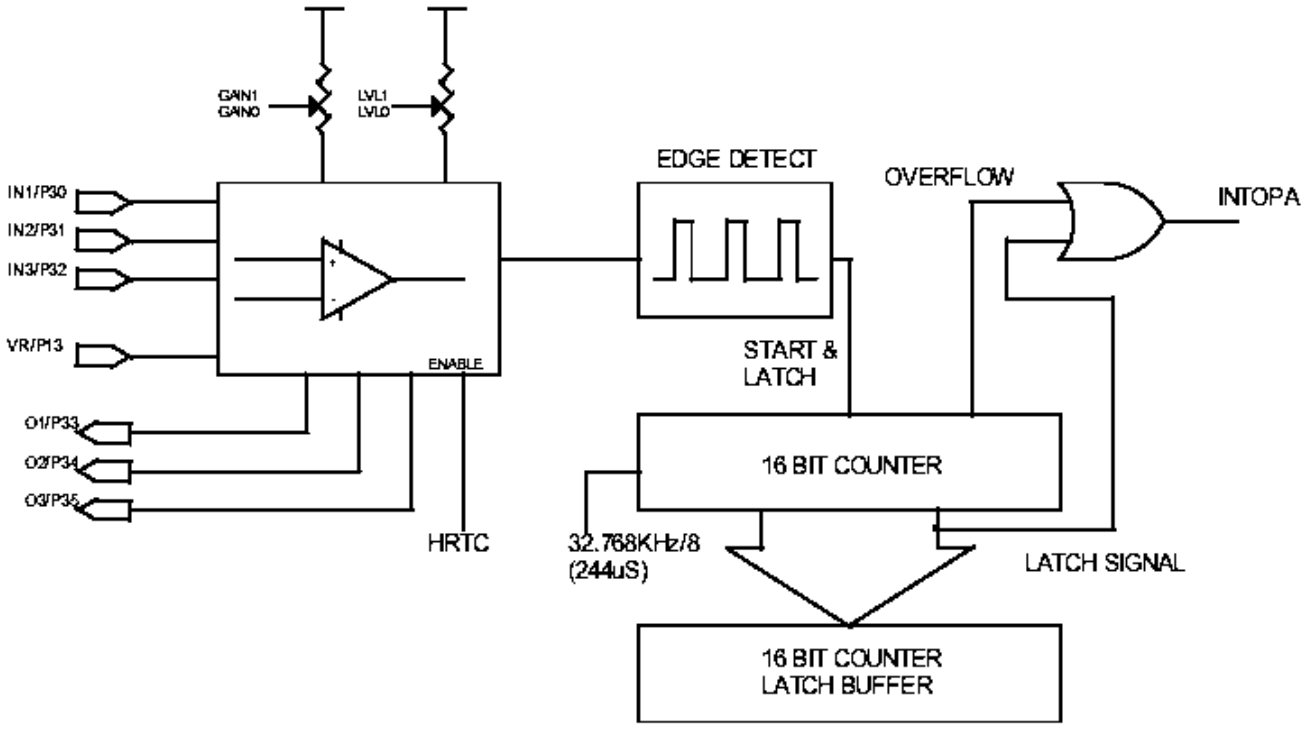


✧ OPA control (P30C1/P30C2 ~ P35C1/P35C2 & HRTC)

OPCTL register (address $58); b4 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58H	W	0000000B				LVL1	LVL0	GAIN1	GAIN0	HRTC

Bit Name		Bit Value
P35C2 ~ P30C2 =0 P35C1~P30C1 =1 OPA function enable		HRTC=0 OPA & EDGE DETECT CIRCUIT DISABLE
		HRTC=1 OPA & EDGE DETECT CIRCUIT ENABLE
LVL1 & LVL0 OPA Voltage level control	00	36/40 Vdd (max.)
	01	34/40 Vdd
	10	32/40 Vdd
	11	28/40 Vdd (min.)
GAIN1 & GAIN0 OPA Gain control	00	1st OPA Gain=10, 2nd OPA Gain=2(min.)
	01	1st OPA Gain=20, 2nd OPA Gain=2
	10	1st OPA Gain=10, 2nd OPA Gain=5
	11	1st OPA Gain=20, 2nd OPA Gain=5(max.)



[5] CLOCK SOURCE

The 32768Hz crystal oscillator generates the system clock bit of POWRMAN register could stop the oscillation.

[6] TIMER/COUNTERS

WT5041 has one 16-bit counter/timer, namely system time base use, namely TIMER1 & TIMER2.

TIMER 0

Timer 0 is a 16-bit up counter with two 8-bit output registers and a 3-bit prescaler. TMOL is Iow byte register and TMOH is the high byte register. The prescaler is a clock divider that can divide 32768Hz by controlled PS02, PS01, PS00. TMOM2 and TMOM1 bits control four operating modes of TIMER 0.

✧ Mode 0 (TMOM2=0, TMOMI=0) **(Disable mode)**

Counter is disabled. In this mode CNT pin function is disable. Only either P27 or INT7 pin function are available.

✧ Mode 1 (TMOM2=0, TMOMI=I) **(Counter mode)**

It can count pulses from CNT input pin. The counter uses positive edge trigger (XOR0=I) or negative edge trigger (XOR0=0).

Reading TMOH can load the counter value into TMOL and TMOH. After the counter value is read from TM0H, the counter is reset to 0.

If the counter overflows, the INTM0 bit will be set and generate an interrupt if ENTM0 bit is 1.

✧ Mode 2 (TMOM2=I, TMOMI=0) **(Reed switch mode)**

It can count time interval between two pulses from CNT0 pin. Every positive edge (XOR0=I) or negative edge (XOR0=0) will save the counter value in TMOL and TMOH, generate an interrupt (INTM0), and reset the counter. The clock of the counter is from the 3-bit prescaler, which can divide 32768Hz by controlled $PS0_2$, $PS0_1$, $PS0_0$.

The time interval is calculated by:

Time interval - (16-bit counter value)x (3-bit prescaler value) x (1/32768)

If the counter overflows the INTM0 bit will be set and interrupt occur if ENTM0 bit is 1.

✧ Mode 3 (TMOM2=I, TMOMI=I) **(16 bit free-run timer mode)**

The Same as mode 2; except reading TMOH resets the signal. The clock of the counter is from the 3-bit pre-scaler that can divide 32768Hz by controlled PS02, PS01 and PS00. If the counter overflows, the INTM0 bit will be set and generate an interrupt if ENTM0 bit is 1.

In this free-run timer mode, if ENTM0 bit is set to "1" in CPU halt state, the NTM0 interrupt can reset the HALT bit and let CPU continue working (warm start).

In this mode CNT pin function is disable. Only either P27 or INT7 function are available.

In mode 1 & 2, if ENTM0 bit is set to "1" in halt state, a positive edge (XOR0-"1") or falling edge (XOR0="0") from CNT pin can reset the HALT bit and let CPU continue working (warm start)..

TM0C register (address $50); b5~b0, Write

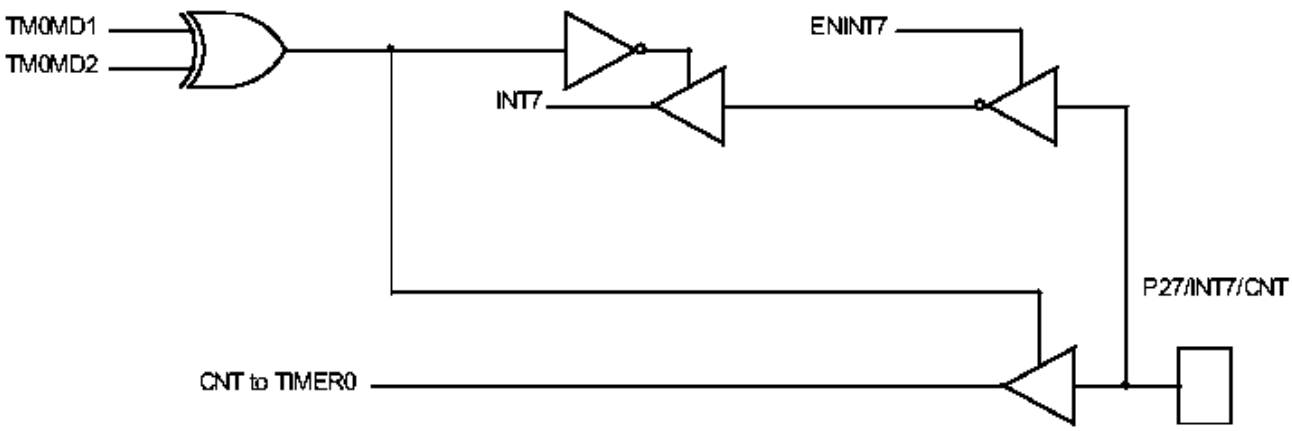
TM0L register (address $50); b7~b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50H	W	00H			XOR1	TMOM2	TMOM1	$PS0_2$	$PS0_1$	PS0o
50H	R	XxH	$CT0_7$	$CT0_6$	$CT0_5$	$CT0_4$	$CT0_3$	$CT0_2$	$CT0_1$	$CT0_0$

TM0H register (address $51); b7~b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51H	R	XxH	$CT0_{15}$	$CT0_{14}$	$CT0_{13}$	$CT0_{12}$	$CT0_{11}$	$CT0_{10}$	$CT0_9$	$CT0_8$

Bit Name	Bit = 0	Bit = 1
XOR0	Set counter 0 is triggered by negative	Set counter 0 is triggered by positive edge.
TMOM2,TMOM1	Timer0/Counter0control bits. 00: counter is disabled. (Disable mode) 01: count pulses from CNT0 input. (Counter mode) 10: measure time interval between two pulses input from CNT0. (Reed switch mode) 11: internal timer with prescaler. (16 bit free-run timer mode)	
PS02 ~ PS0o	Prescaler of TIMER0 000: 32768Hz divide by 1. 001: 32768Hz divide by 2. 010: 32768Hz divide by 4. 011: 32768Hz divide by 8. 101: 32768Hz divide by 32. 110: 32768Hz divide by 64. 111: 32768Hz divide by 128.	
CT015 - CT0o	Timer0/Counter0 output value.	



TIMER 1

Timer 1 is an 8-bit down counter with a reload register TMLD1. To set data in timer 1 first write data in TMLD1 and it will automatically transfer to timer 1. Timer 1 start counting when data is set in timer 1. Once the counter counts down to zero, when next clock is input, the timer 1 interrupt flag (INTM1) is set to "1", new data is loaded from TMLD1, and count continues. If the value set in TMLD1 is N, timer 1 interval is N/3-bit prescaler frequency (N=I to 255).

TM12C register (address $51); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51H	W	00H	--	--	$PS1_2$	$PS1_1$	$PS1_0$	$PS2_2$	$PS2_1$	$PS2_0$

TMLD1 register (address $52); b7-b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52H	W	00H	$TMLD1_7$	$TMLD1_6$	$TMLD1_5$	$TMLD1_4$	$TMLD1_3$	$TMLD1_2$	$TMLD1_1$	$TMLD1_0$

Bit Name	Bit value
TM_7 ~ TM_0	Timer 1 data.
$PS1_2$ ~ $PS1_0$	Prescaler of TIMER1. 000: 32768Hz divide by 1. 001: 32768Hz divide by 2. 010: 32768Hz divide by 4. 011: 32768Hz divide by 8. 100: 32768Hz divide by 16. 101: 32768Hz divide by 32. 110: 32768Hz divide by 64. 111: 32768Hz divide by 128.

TIMER 2

Timer 2 is an 8-bit down counter with a reload register TMLD2. To set data in timer 2, first write data in TMLD2 and it will automatically transfer to timer 2. Timer 2 start counting when data is set in timer 2. Once the counter counts down to zero, when next clock is input, the timer 2 interrupt flag (INTM2) is set to "1", new data is loaded from TMLD2, and count continues. If the value set in TMLD2 is N, timer 2 interval is **N**/3-bit prescaler frequency (N-1 to 255).

TM12C register (address $51); b7 ~ b0 , Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51H	W	00H	--	--	$PS1_2$	$PS1_1$	$PS1_0$	$PS2_2$	$PS2_1$	$PS2_0$

TMLD2 register (address $53); b7-b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52H	W	00H	$TMLD2_7$	$TMLD2_6$	$TMLD2_5$	$TMLD2_4$	$TMLD2_3$	$TMLD2_2$	$TMLD2_1$	$TMLD2_0$

Bit Name	Bit value
$TMLD2_7$ ~ $TMLD2_0$	Timer 1 data.
$PS2_2$ ~ $PS1_0$	Prescaler of TIMER2. 000: 32768Hz divide by 1. 001: 32768Hz divide by 2. 010: 32768Hz divide by 4. 011: 32768Hz divide by 8. 100: 32768Hz divide by 16. 101: 32768Hz divide by 32. 110: 32768Hz divide by 64. 111: 32768Hz divide by 128.

[7] REAL TIME CLOCK (2Hz TIMER)

WT5041 has a 2Hz real time clock source, When EN2HZ set NT2HZ will be set every 2Hz. After reading INT2HZ this flag will be reset NT2HZ can reset the HALT bit and let CPU continue working (warm start)

INTEN1 register (address $55); b5~b0, Write

INTFLG1 reclister (address $55); b5~b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
55H	W	00000H	--	--	EN2HZ	ENTM2	ENTM1	ENTM0	ENOPA	ENRFC
55H	R	00000H	--	--	INT2HZ	INTM2	INTM1	INTM0	INTOPA	INTRFC

Bit Name	Bit=0	Bit=1
EN2HZ	2Hz wake up flag disable	2Hz wake up flag enable
INT2HZ	2Hz wake up flag reset	2Hz wake up flag set

[8] WATCH-DOG TIMER

Watchdog timer is controlled by WDTRFC. It will generate reset while the timer reach 0.5 sec, 1 sec, 2 sec or 4 sec. Setting 0 in CLRWDT also can disable it. Every time when writing a value to this register will reset the watch-dog timer

WDTRFC register (address $4F); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4FH	W	00000B	WDT2	WDT1	WDT0	--	RABS1	RABS0	RFCMD1	RFCMD0

Bit Name	Bit value
$WDT2_7$ ~ $WTDT_0$	0xx: Watch-dog timer is disabled
	100:4 second. 101:2 second. 110:1 second. 111:0.5 second.

CLRWDT register (address $57); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
57H	W	xxxxxB	WDT2	WDT1	WDT0	--	RABS1	RABS0	RFCMD1	RFCMD0

[9] INTERRUPT

All the interrupt sources use the CPU's IRQ interrupt vector (FFFEH and FFFFH) at normal mode. And use the CPU's FFFBH) at halt mode. Each interrupt source could enable by setting the individual enable bit. Write any data to INT_CLR register ($59H) will clear all the interrupt flags.

INTEN0 register (address $54); b7~b0, Write
INTFLG0 register (address $54); b7~b0, Read.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54H	W	00000H	ENINT7	ENINT6	ENINT5	ENINT4	ENINT3	ENINT2	ENINT1	ENINT0
54H	R	xxxxxH	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0

INTEN1 register (address $55); b5~b0, Write
INTFLG1 register (address $55); b5 ~ b0, Read

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
55H	W	00000H			EN2HZ	ENTM2	ENTM1	ENTM0	ENOPA	ENRFC
55H	R	xxxxxH			INT2HZ	INTM2	INTM1	INTM0	INTOPA	INTRFC

Bit Name	Bit=0	Bit=1
EN2HZ	Disable 2HZ interrupt.	Enable 2HZ interrupt.
ENTM0	Disable TM0 interrupt.	Enable TM0 interrupt.
ENTM1	Disable TM1 interrupt.	Enable TM1 interrupt.
ENTM2	Disable TM2 interrupt.	Enable TM2 interrupt.
ENOPA	Disable OPA interrupt.	Enable OPA interrupt.
ENRFC	Disable RFC interrupt.	Enable RFC interrupt.
ENINTn	Disable INTn pin interrupt.	Enable INTn pin interrupt (n=0-7)
INT2HZ	No 2Hz interrupt	2Hz interrupt
INTM0	No TM0 interrupt	TM0 interrupt
INTM1	No TM1 interrupt	TM1 interrupt
INTM2	No TM2 interrupt	TM2 interrupt
INTOPA	No OPA interrupt	OPA interrupt
INTRFC	No RFC interrupt	RFC interrupt
INTn	No INTn pin interrupt	INTn pin interrupt (n=0 ~ 7)

INTCLR register (address $59); b7 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
59H	W	xxxxxH	--	--	--	--	--	--	--	--

Setting 0 in INTCLR can clear all of the interrupt flag.

[10] POWER DOWN MODE

POWRMAN register (address $56); b5 ~ b0, Write

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56H	W	xxx00B	--	--	--	--	--	--	OFF	HALT

Bit Name	Bit=0	Bit=1
OFF	No action.	Stop the oscillator and go to off state.
HALT	No action.	Stop the CPU and go to halt state.

HALT MODE

The HALT bit could halt the CPU operation. If any wake up signal is active, it will reset the HALT bit and let CPU continue working. This is called warm start. The program will execute the CPU's NMI routine (use vector stored in FFFAH and FFFBH).

HALT mode release signal sources:

(1) Timer0 is overflow or CNT match and ENTMO="1"
(2) Timer1 is underflow and ENTMI="1"
(3) Timer2 is underflow and ENTM2="1"
(4) A falling edge on INT0 pin when ENINT0="1"
(5) A falling edge on INT1 pin when ENINTI="1"
(6) A falling edge on INT2 pin when ENiNT2="1",
(7) A falling edge on INT3 pin when ENINT3="1",
(8) A falling edge on INT4 pin when ENINT4="1",
(9) A falling edge on INT5 pin when ENINT5="1"
(10) A falling edge on INT6 pin when ENINT6="1"
(11) A falling edge on INT7 pin when ENINT7="1"
(12) OPA counter overflow or counter match and ENOPA="1"
(13) RFC counter overflow or counter match and ENRFC="1"
(14) 2Hz come and EN2HZ="1"

OFF MODE

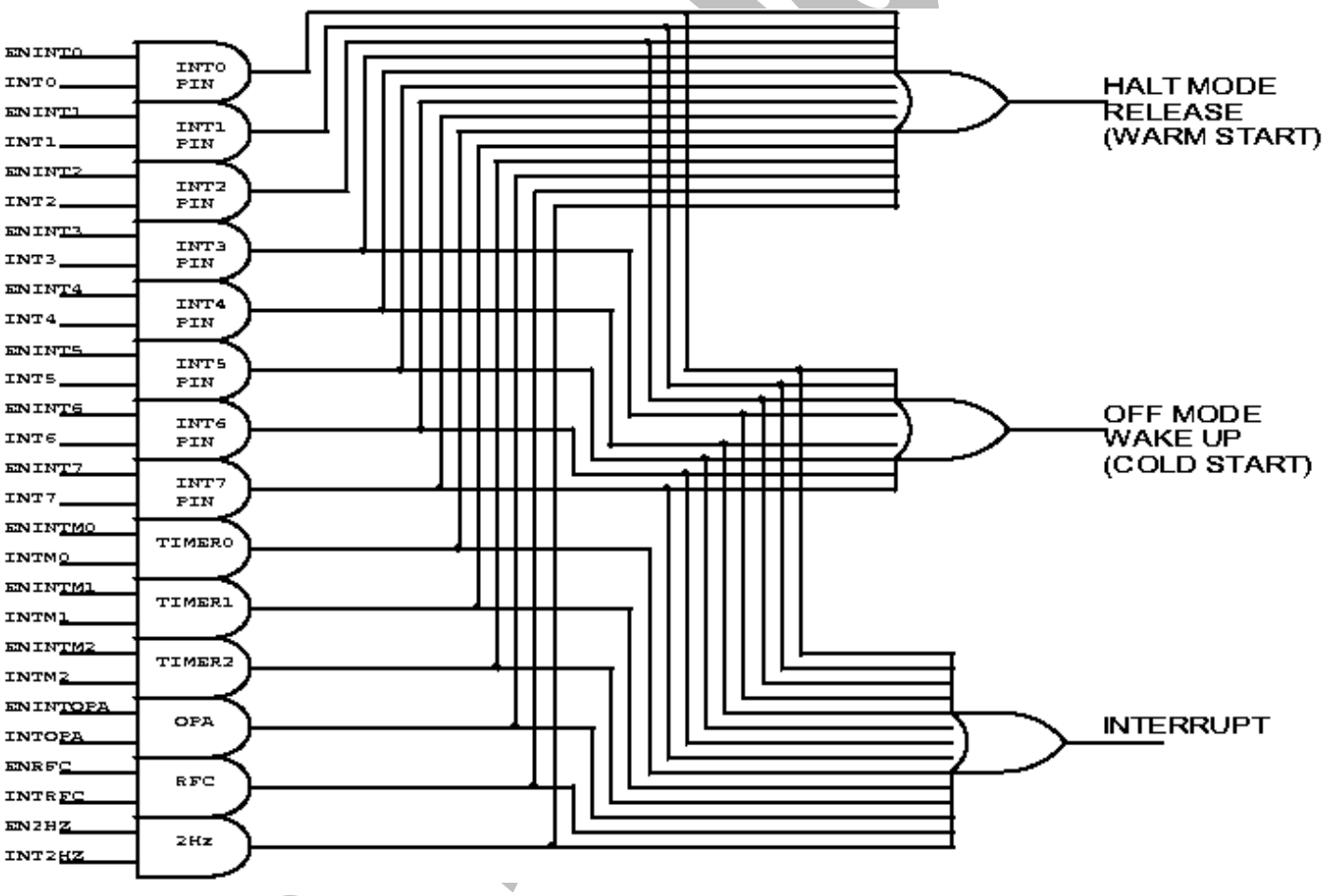
When OFF bit is "1", it goes Off mode immediately. The oscillator, LCD driver, and CPU are all disabled.

If reset pin goes low or any wake up signal is active, the whole chip will be reset. This is called cold start. The program will execute the CPU's Reset routine (use vector stored in FFFCH and FFFDH). Only the contents in RAM are not affected.

OFF mode wake up signal sources:

(1) A falling edge on INT0 pin when ENINT0="1"
(2) A falling edge on INT1 pin when ENINTI="1"

(3) A falling edge on INT2 pin when ENINT2="1"
(4) A falling edge on INT3 pin when ENINT3="1"
(5) A falling edge on INT4 pin when ENINT4="1"
(6) A falling edge on INT5 pin when ENINT5-"1"
(7) A falling edge on INT6 pin when ENINT6="1"
(8) A falling edge on INT7 pin when ENINT7="1"



[11] LCD DRIVER/CONTROLLER

The WT5041 contains 128 segments LCD driver/controllers and it has circuit that directly drives the Liquid Crystal Display (LCD) and its control circuit.
The WT5041 has the following connecting pins with
(1) Segment output 32 pins (SEG1-SEG32)
(2) Common output 4 pins (COM1-COM4)

in addition, Bias1 and Bias2 pins are bias voltage input pins to drive the LCD and should be connected with 0.01uF capacitors.
The devices that can be directly driven is selected for LCD drivers of following drive methods:
(1) 1/4 duty (1/3 bias) LCD... Max. 128 segments (8 segments X 16 digits)
(2) 1/3 duty (1/3 bias) LCD... Max. 96 segments (8 segments X 12 digits)
(3) 1/3 duty (1/2 bias) LCD ... Max. 96 segments (8 segments X 12 digits)

(4) 1/2 duty (1/2 bias) LCD ... Max. 64 segments (8 segments X 8 digits)

Control of LCD Driver

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10H	W	xxx00B	--	--	--	LCDON	LCDONT1	LCDONT0	DTY1	DTY0

Bit Name	Bit Value	Function
DTY1, DTY0 Duty & Bias Selection	00	1/4 duty. 1/3bias LCD PANEL
	01	1/3 duty. 1/3bias LCD PANEL
	10	1/3duty, 1/2bias LCD PANEL
	11	l/2dutv. 1/2bias LCD PANEL
LCDONT1 LCDONT0 LCD turn on scan time	00	Full time turn on
	01	1/4 cycle scan time turn on
	10	1/8 cycle scan time turn on
	11	1/16 cycle scan time turn on
LCDON	0	LCD turn off
	1	LCD turn on

Frame Frequency f(32 ~128Hz)

Base Freq.	1/4 Duty	1/3 Duty	1/2 Duty
Fs / 256	Fs/256	4/3 * Fs / 256	4/2 * Fs / 256
Fs = 32KHz	f = 128 Hz	f = 170 Hz	f= 256 Hz

LCD Display Operation

The display data stored to the display data area are read automatically and sent the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance easily by overwriting the contents of the display data area with a program

DISPLAY DATA AREA

Write the following assigned area

	SEG1-SEG8	SEG9-SEG16	SEG17-SEG24	SEG25-SEG32
COM1	DDA11 ($00)	DDA12 ($01)	DDA13 ($02)	DDA14 ($03)
COM2	DDA21 ($04)	DDA22 ($05)	DDA23 ($06)	DDA24 ($07)
COM3	DDA31 ($08)	DDA32 ($09)	DDA33 ($0A)	DDA34 ($0B)
COM4	DDA41 ($0C)	DDA42 ($0D)	DDA43 ($0E)	DDA44 ($0F)

1/4 DUTY	COM4	COM3	COM2	COM1
1/3 DUTY	****	COM3	COM2	COM1
1/2 DUTY	****	****	COM2	COM1

[12] I/O REGISTER ADDRESS MAPPING

NAME	ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
DDA11	$00	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA12	$01	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA13	$02	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA14	$03	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA21	$04	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA22	$05	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA23	$06	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA24	$07	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA31	$08	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA32	$09	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA33	$0A	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA34	$0B	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA41	$0C	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA42	$0D	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA43	$0E	R/W	B7	B6	B5	B4	B3	B2	B1	B0
DDA44	$0F	R/W	B7	B6	B5	B4	B3	B2	B1	B0
LCDC	$10	W	-	-	-	LCDON	LCDONT1	LCDONT0	DTY1	DTY0
P0	$40	R/W	P07	P06	P05	P04	P03	P02	P01	P00
P1	$41	R	P17	P16	P15	P14	P13	P12	P11	P10
P2	$42	R	P27	P26	P25	P24	P23	P22	P21	P20
P3	$43	R	P37	P36	P35	P34	P33	P32	P31	P30
P0C	$44	W	-	-	-	-	P0SCHN	P0SCLN	P0HC	P0LC
P1C1	$45	W	P17C1	P16C1	P15C1	P14C1	P13C1	P12C1	P11C1	P10C1
P1C2	$46	W	P17C2	P16C2	P15C2	P14C2	P13C2	P12C2	P11C2	P10C2
P2C1	$47	W	P27C1	P26C1	P25C1	P24C1	P23C1	P22C1	P21C1	P20C2
P2C2	$48	W	P27C2	P26C2	P25C2	P24C2	P23C2	P22C2	P21C2	P20C2
P3C1	$49	W	P37C1	P36C1	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
P3C2	$4A	W	P37C2	P36C2	P35C2	P34C2	P33C2	P32C2	P31C2	P30C2
OPCNTL	$4B	R	OPCNT7	OPCNT6	OPCNT5	OPCNT4	OPCNT3	OPCNT2	OPCNT1	OPCNT0
PWMBUZ	$4B	W	-	-	EPWM2	EPWM1	EPWM0	EVN1	EVN0	BUZ0
OPCNTH	$4C	R	OPCNT15	OPCNT14	OPCNT13	OPCNT12	OPCNT11	OPCNT10	OPCNT9	OPCNT8
PWM0	$4C	W	PWM07	PWM06	PWM05	PWM04	PWM03	PWM02	PWM01	PWM00
RFCNTL	$4D	R	RFCNT7	RFCNT6	RFCNT5	RFCNT4	RFCNT3	RFCNT2	RFCNT1	RFCNT0
PWM1	$4D	W	PWM17	PWM16	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10
RFCNTH	$4E	R	RFCNT15	RFCNT14	RFCNT13	RFCNT12	RFCNT11	RFCNT10	RFCNT9	RFCNT8
PWM2	$4E	W	PWM27	PWM26	PWM25	PWM24	PWM23	PWM22	PWM21	PWM20
WDTRFC	$4F	W	WDT2	WDT1	WDT0	-	RABS1	RABS0	RFCMD1	RFCMD0
TM0C	$50	W	-	-	XOR1	TM0M2	TM0M2	PS02	PS01	PS00
TM0L	$50	R	CT07	CT06	CT05	CT04	CT03	CT02	CT01	CT00
TM12C	$51	W	-	-	PS12	PS11	PS10	PS22	PS21	PS20
TM0H	$51	R	CT015	CT014	CT013	CT012	CT011	CT010	CT09	CT08
TMLD1	$52	W	TMLD17	TMLD16	TMLD15	TMLD14	TMLD13	TMLD12	TMLD11	TMLD10
TMLD2	$53	W	TMLD27	TMLD26	TMLD25	TMLD24	TMLD23	TMLD22	TMLD21	TMLD20
INTEN0	$54	W	ENINT7	ENINT6	ENINT5	ENINT4	ENINT3	ENINT2	ENINT1	ENINT0
INTFLG0	$54	R	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
INTEN1	$55	W	-	-	EN2HZ	ENTM1	ENTM0	ENTM0	ENOPA	RMTGV
INTFLG1	$55	R	-	-	INT2HZ	INTM1	INTM0	INTM0	INTOPA	INTRF
POWRMAN	$56	W	-	-	-	-	-	-	OFF	HALT
CLR_WDT	$57	W	-	-	-	-	-	-	-	-
OPCTL	$58	W	-	-	-	LVL1	LVL0	GAIN1	GAIM0	HRTC
INTCLR	$59	W	-	-	-	-	-	-	-	-

[13] ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{ss} = 0V)

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{dd}	-0.5 ~ +7	V
Input Voltage Range	V_{in}	-0.5 ~ VDD + 0.5	V
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	-50 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{ss} = 0V, T_{opr} = 0 to 70 °C)

PARAMETER	SYMBOL	Min.	Typ.	Max.	Unit	CONDITIONS
Operating Voltage	V_{dd}		-	5.5	V	
Operating Current	I_{op}		1		mA	
Standby Current (HALT)	I_{halt}		-	8	µ A	LCD turn on, V_{dd}=3.0V
Standby Current (OFF)	I_{off}		-	1	µ A	V_{dd}=3.0V
X'tal OSC frequency	F_{osc}		32.768		KHz	V_{dd}=3.0V
Ring Oscillator Frequency	F_{rosc}		8		MHz	V_{dd}=3.0V
PWM Output	I_{oh}		5		mA	V_{dd}=3.0V V_{oh}=2.0V
PWM Output	I_{ol}		5		mA	V_{dd}=3.0V V_{ol}= 0.8V
Input High Level	V_{ih}	2.0			V	V_{dd}=3.0V
Input Low level	V_{il}			0.8	V	V_{dd}=3.0V
Output High Source Current	I_{oh}	300			µ A	V_{dd}=3.0V V_{oh}=2.4V
Output low sink Current	I_{ol}	1.0			mA	V_{dd}=3.0V V_{ol}=0.8V
CPU Clock	F_{cpu}				KHz	F_{cpu}=F_{osc}@3.0V