Intel® Celeron® Processor in the 478-Pin Package up to 1.70 GHz

Datasheet

- Available at 1.70 GHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- System bus frequency at 400 MHz.
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency.
- Hyper Pipelined Technology.
- Advanced Dynamic Execution
  - —Very deep out-of-order execution
  - —Enhanced branch prediction
- 8 KB Level 1 data cache
- Level 1 Execution Trace Cache stores 12K micro-ops and removes decoder latency from main execution loops
- 128 KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache) with Error Correction Code (ECC)
- 144 Streaming SIMD Extensions 2 (SSE2) Instructions
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems

The Intel® Celeron® processor in the 478-pin package at 1.70 GHz expands Intel's processor family into the value-priced PC market segment. Intel Celeron processors provide the value customer the capability to affordably get onto the Internet, and utilize educational programs, home-office software and productivity applications. All of Intel's Celeron processors include an integrated L2 cache, and are built on Intel's advanced CMOS process technology. The Intel Celeron processor is backed by over 30 years of Intel experience in manufacturing high-quality, reliable microprocessors.

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Revision History

Revision	Description	Date
-001	Initial Release.	May 2002

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1.0 Introduction

The Intel® Celeron® processor in the 478-pin package utilizes Flip-Chip Pin Grid Array (FC-PGA2) package technology, and plugs into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Celeron processor in the 478-pin package maintains the tradition of compatibility with IA-32 software.

The Celeron processor in the 478-pin package is designed for uni-processor based Value PC desktop systems. Features of processor include hyper pipelined technology, a 400 MHz system bus, and an execution trace cache. The 400 MHz system bus is a quad-pumped bus that is clocked with a 100 MHz system clock, making 3.2 GB/sec data transfer rates possible. The execution trace cache is a first level cache that stores approximately 12k decoded micro-operations, which removes the decoder from the main execution path.

Additional features include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 128 KB, on-die level 2 (L2) cache. The floating point and multi-media units have 128 bit wide registers with a separate register for data movement. Finally, SSE2 support includes instructions for double-precision floating point, SIMD integer, and memory management. Power management capabilities such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep have also been retained.

The Celeron processor in the 478-pin package 400 MHz system bus utilizes a split-transaction, deferred reply protocol. This system bus is not compatible with the P6 processor family bus. The 400 MHz system bus uses Source-Synchronous Transfer (SST) of address and data to improve throughput by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock, and is referred to as a “double-clocked” or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2 GB/second.

Intel will be enabling support components for the Celeron processor in the 478-pin package including a heatsink, heat sink retention mechanism, and socket. Manufacturability is a high priority; hence mechanical assembly can be completed from the top of the motherboard and should not require any special tooling. The processor system bus uses a variant of GTL+ signalling technology called Assisted Gunning Transceiver Logic (AGTL+) signalling technology.

1.1 Terminology

A “#” symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the “#” symbol implies that the signal is inverted. For example, D[3:0] = “HLHL” refers to a hex “A”, and D[3:0]# = “LHLH” also refers to a hex “A” (H= High logic level, L= Low logic level).

System Bus refers to the interface between the processor and system core logic (a.k.a. the chipset components). The system bus is a multiprocessing interface for processors, memory, and I/O.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- *Celeron® processor in the 478-pin package (also referred as the Processor)* — 0.18 micron processor core in the FC-PGA2 package with a 128 KB L2 cache.
- *Pentium® 4 processor in the 478-pin package* — 0.18 micron Pentium® 4 processor core in the FC-PGA2 package with a 256 KB L2 cache.
- *Processor* — In this document, the term processor refers to the Celeron processor in the 478-pin package.
- *Keepout zone* — The area on or near the processor that system design can not utilize.
- *Intel® 845 chipset* — Chipset that supports PC133 and DDR memory technology for the Celeron processor in the 478-pin package.
- *Intel® 845G chipset* — Chipset with embedded graphics that supports DDR memory technology for the Celeron processor in the 478-pin package.
- *Intel® 845E chipset* — Chipset that supports DDR memory technology for the Celeron processor in the 478-pin package.
- *Processor core* — Processor core die with integrated L2 cache.
- *FC-PGA2 package* — Flip-Chip Pin Grid Array package with 50 mil pin pitch and Integrated heat spreader.
- *mPGA478B socket* — Surface mount, 478 pin, Zero Insertion Force (ZIF) socket with 50 mil pin pitch. The socket mates the processor to the system board.
- *Integrated heat spreader* —The surface used to make contact between a heatsink or other thermal solution and the processor. *Integrated heat spreader* is abbreviated IHS.
- *Retention mechanism* —The structure mounted on the system board that provides support and retention of the processor heatsink.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1. Reference Documents

Document	Order Number
Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 850 Chipset Platform Design Guide	http://developer.intel.com/design/pentium4/guides/249888.htm
Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 845 Chipset Platform for SDR Platform Design Guide	http://developer.intel.com/design/pentium4/guides/298354.htm
Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845 Chipset Platform for DDR Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298605.htm
Intel® Pentium® 4 Processor in the 478-pin PackageThermal Design Guidelines	http://developer.intel.com/design/pentium4/guides/249889.htm
Intel® Pentium® 4 Processor VR-Down Design Guidelines	http://developer.intel.com/design/Pentium4/guides/249891.htm
CK00 Clock Synthesizer/Driver Design Guidelines	http://developer.intel.com/design/pentium4/guides/249206.htm
CK408 Clock Design Guidelines	Contact Intel Field Representative
Intel® Pentium®4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines	http://developer.intel.com/design/pentium4/guides/249890.htm
IA-32 Intel® Architecture Software Developer's Manual, Volume 1: Basic Architecture	http://developer.intel.com/design/pentium4/manuals/245470.htm
IA-32 Intel® Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	http://developer.intel.com/design/pentium4/manuals/245471.htm
IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programming Guide	http://developer.intel.com/design/pentium4/manuals/245472.htm
AP-485 Intel® Processor Identification and the CPUID Instruction	http://developer.intel.com/design/xeon/applnots/241618.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xeon/guides/249679.htm

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2.0 Electrical Specifications

2.1 System Bus and GTLREF

Most Celeron processor in the 478-pin package system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signalling technology. As with the Intel P6 family of microprocessors, this signalling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Like the Pentium 4 processor, the termination voltage level for the Celeron processor in the 478-pin package AGTL+ signals is VCC, which is the operating voltage of the processor core. The use of a termination voltage that is determined by the processor core allows better voltage scaling on the system bus for the Celeron processor in the 478-pin package. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Design guidelines for the Celeron processor in the 478-pin package system bus are detailed in the in the appropriate Platform Design Guide (refer to Table 1).

The AGTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board (see Table 12 for GTLREF specifications). Termination resistors are provided on the processor silicon and are terminated to its core voltage (VCC). Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most AGTL+ signals.

Some AGTL+ signals do not include on-die termination and must be terminated on the system board. See Table 3 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Pins

For clean on-chip power distribution, the Celeron processor in the 478-pin package has 85 VCC (power) and 181 VSS (ground) inputs. All power pins must be connected to VCC, while all VSS pins must be connected to a system ground plane.The processor VCC pins must be supplied the voltage determined by the VID (Voltage ID) pins.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 6. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and design guidelines, refer to Table 1 for the appropriate platform design guide, and the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*.

2.3.1 Vcc Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, must be provided by the voltage regulator solution (VR). For more details on this topic, refer to Table 1 for the appropriate platform design guide, and the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*.

2.3.2 System Bus AGTL+ Decoupling

The Celeron processor in the 478-pin package integrates signal termination on the die as well as incorporates high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation. For more information, refer to Table 1 for the appropriate Platform Design Guide.

2.3.3 System Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the system bus interface speed as well as the core frequency of the processor. As in previous generation processors, the Celeron processor in the 478-pin package core frequency is a multiple of the BCLK[1:0] frequency. Like the Pentium 4 processor, the Celeron processor in the 478-pin package uses a differential clocking implementation. For more information on the Celeron processor in the 478-pin package clocking, refer to the *CK408 Clock Design Guidelines.*

The VID specification for the Celeron processor in the 478-pin package is supported by the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 6 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

The Celeron processor in the 478-pin package uses five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. Table 2 specifies the voltage level corresponding to the state of VID[4:0]. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to low voltage level. The definition provided in Table 2 is not related in any way to previous P6 processors or VRs, but is compatible with the Pentium 4 processor. If the processor socket is empty (VID[4:0] = 11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* for more details.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2. Voltage Identification Definition

VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

2.3.4 Phase Lock Loop (PLL) Power and Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Celeron processor in the 478-pin package . Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. A typical filter topology is shown in Figure 1.

The AC low-pass requirements, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 1), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2. For recommendations on implementing the filter refer to Table 1 for the appropriate Platform Design Guide.

Figure 1. Typical $V_{CCIOPLL}$, V_{CCA} and V_{SSA} Power Distribution

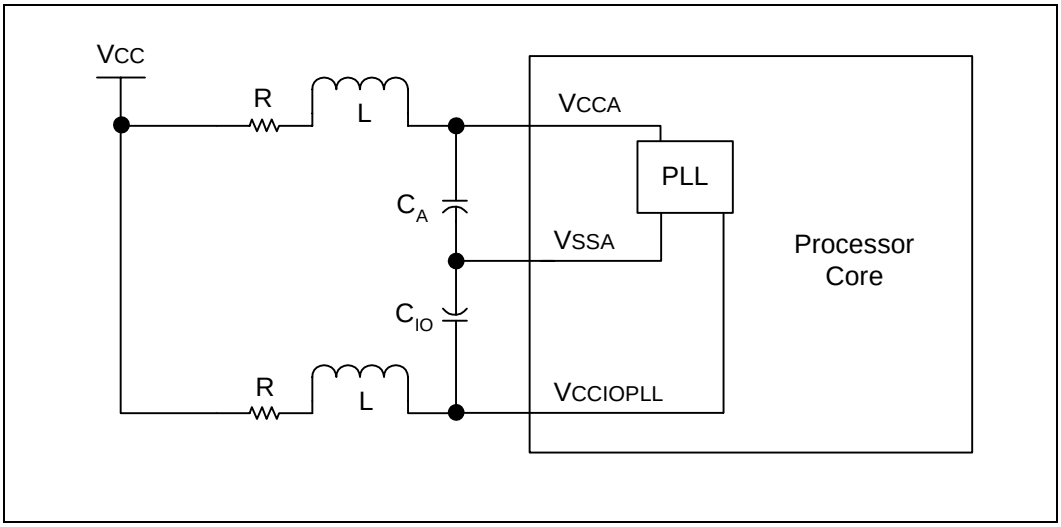
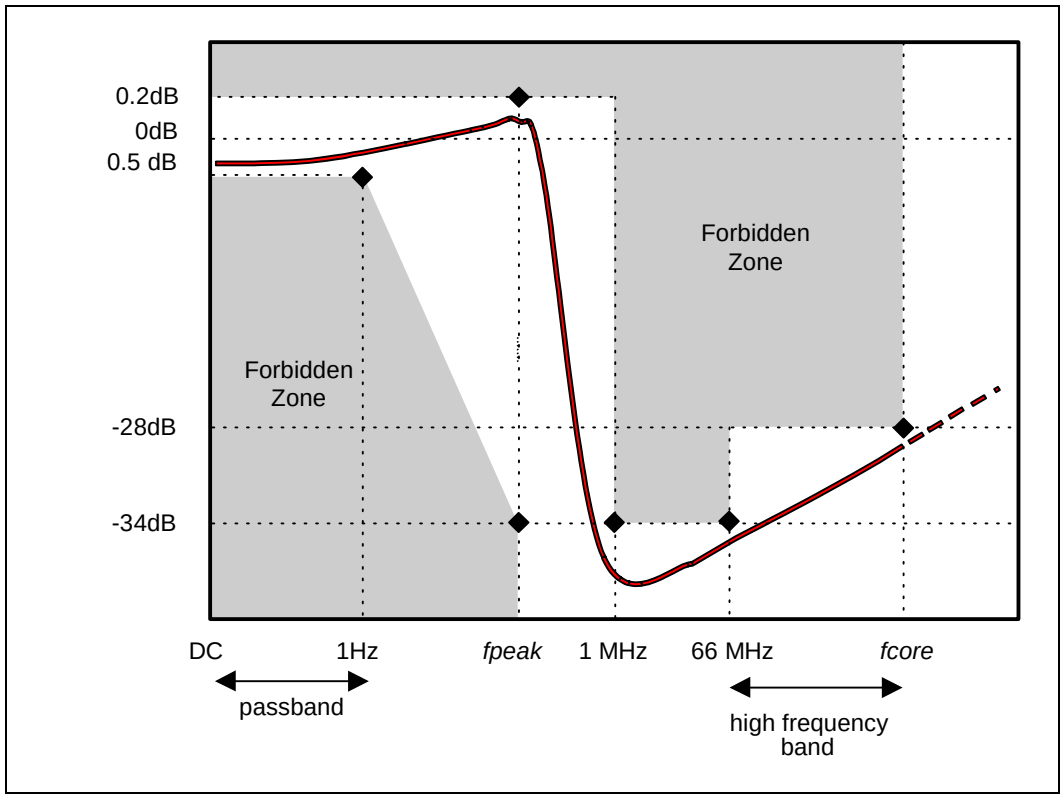


Figure 2. Phase Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.

2.4 Reserved, Unused, and TESTHI Pins

All RESERVED pins must remain unconnected. Connection of these pins to VCC, VSS, or to any other signal (including each other) can result in component malfunction or incompatibility with a future Celeron processors in the 478-pin package. See Chapter 5.0 for a pin listing of the processor and the location of all RESERVED pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. In a system level design, on-die termination has been included on the Celeron processor in the 478-pin package to allow signals to be terminated within the processor silicon. Most unused AGTL+ inputs should be left as no connects, as AGTL+ termination is provided on the processor silicon. However, see Table 3 for details on AGTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (VSS). Unused outputs can be left unconnected, however this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value for the on-die termination resistors (R_{TT}). See Table 12.

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Input and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused output unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate *Platform Design Guide,* and the *ITP700 Debug Port Design Guide*.

The TESTHI pins should be tied to the processor VCC using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, If the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor should be used for each group:

- TESTHI[1:0]
- TESTHI[5:2]
- TESTHI[10:8]
- TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used (see Table 32), they may be connected individually to VCC using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 kΩ resistors is acceptable. Tying ITPCLKOUT[1:0] directly to VCC or sharing a pull-up resistor to VCC will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

As an alternative, group 2 (TESTHI [5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor VCC. This has no impact on system functionality. TESTHI[0] and TESTHI[12] may also be tied directly to processor VCC if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0], direct tie to VCC is strongly discouraged for system boards that do not implement an onboard debug port.

2.5 System Bus Signal Groups

To simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term *AGTL+ Input* refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, *AGTL+ Output* refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 3 identifies which signals are common clock, source synchronous, and asynchronous.

Table 3. System Bus Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#[2], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#[2], BR0#[2], DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	**Signal** / **Associated Strobe** REQ[4:0]#, A[16:3]#[5] / ADSTB0# A[35:17]#[5] / ADSTB1# D[15:0]#, DBI0# / DSTBP0#, DSTBN0# D[31:16]#, DBI1# / DSTBP1#, DSTBN1# D[47:32]#, DBI2# / DSTBP2#, DSTBN2# D[63:48]#, DBI3# / DSTBP3#, DSTBN3#
Asynchronous GTL+ Input[4, 5]		A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#
Asynchronous GTL+ Output[4]		FERR#, IERR#, THERMTRIP#, PROCHOT#
TAP Input[4]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[4]	Synchronous to TCK	TDO
System Bus Clock	Clock	BCLK[1:0], ITP_CLK[1:0][3]
Power/Other		VCC, VCCA, VCCIOPLL, VID[4:0], VSS, VSSA, GTLREF[3:0], COMP[1:0], RESERVED, TESTHI[12:8], TESTHI[5:0], THERMDA, THERMDC, VCC_SENSE, VSS_SENSE, VCCVID, BSEL[1:0], SKTOCC#, DBR#[3], ITPCLKOUT[1:0], PWRGOOD

NOTE:
1. Refer to Chapter 5.0 for signal descriptions.
2. These AGTL+ signals do not have on-die termination and must be terminated on the system board.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. These signal groups are not terminated by the processor. Refer to Section 2.4 and the *ITP700 Debug Port Design Guide*, and the appropriate Platform Design Guide as referenced in Table 1 for termination requirements and further details.
5. The value of these pins during the active-to-inactive edge of RESET# determine processor configuration options. See Section 7.1 for details.

2.6 Asynchronous GTL+ Signals

The Celeron processor in the 478-pin package does not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them. See Section 2.10 and Section 2.12 for the DC and AC specifications for the Asynchronous GTL+ signal groups. See Section 7.2 for additional timing requirements for entering and leaving the low power states.

2.7 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Celeron processor in the 478-pin package be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. These considerations must be made for TCK, TMS, TRST#, TDI, and TDO. Two copies of each signal may be required, with each driving a different voltage level.

2.8 System Bus Frequency Select Signals (BSEL[1:0])

The BSEL[1:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Celeron processor in the 478-pin package currently operates at a 400 MHz system bus frequency (selected by a 100 MHz BCLK[1:0] frequency). Individual processors will only operate at their specified system bus frequency.

For more information about these pins refer to Chapter 5.0 and the appropriate Platform Design Guide.

Table 4. BSEL[1:0] Frequency Table for BCLK[1:0]

BSEL1	BSEL0	Function
L	L	100 MHz
L	H	RESERVED
H	L	RESERVED
H	H	RESERVED

2.9 Maximum Ratings

Table 5 lists the processor's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from electro static discharge (ESD), one should always take precautions to avoid high static voltages or electric fields.

Table 5. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	2
V_{CC}	Any processor supply voltage with respect to V_{SS}	–0.5	2.10	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.3	2.10	V	
$V_{inAsynch_GTL+}$	Asynch GTL+ buffer DC input voltage with respect to V_{SS}	–0.3	2.10	V	
I_{VID}	Max VID pin current		5	mA	

NOTE:
1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

2.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon and not at the package pins unless noted otherwise. See Chapter 5.0 for the pin signal definitions and signal pin assignments. Most of the signals on the processor system bus are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 9.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 10.

Table 6 through Table 11 list the DC specifications for the Celeron processor in the 478-pin package and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

2.10.1 Flexible Motherboard Guidelines (FMB)

The FMB guidelines are estimates of the maximum values the Celeron processor in the 478-pin package will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. The Celeron processor in the 478-pin package may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future releases of the Celeron processor in the 478-pin package.

Table 6. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1, 9]
V_{CC}	V_{CC} for processor at 1.70 GHz	1.565	Refer to Table 7 and Figure 3		V	2, 3, 4, 5
I_{CC}	I_{CC} for processor at 1.70 GHz			48.1	A	
I_{SGNT} I_{SLP}	I_{CC} Stop-Grant 1.70 GHz			12.9	A	6, 8
I_{TCC}	I_{CC} TCC active			I_{CC}	A	7
$I_{CC\ PLL}$	I_{CC} for PLL pins			30	mA	

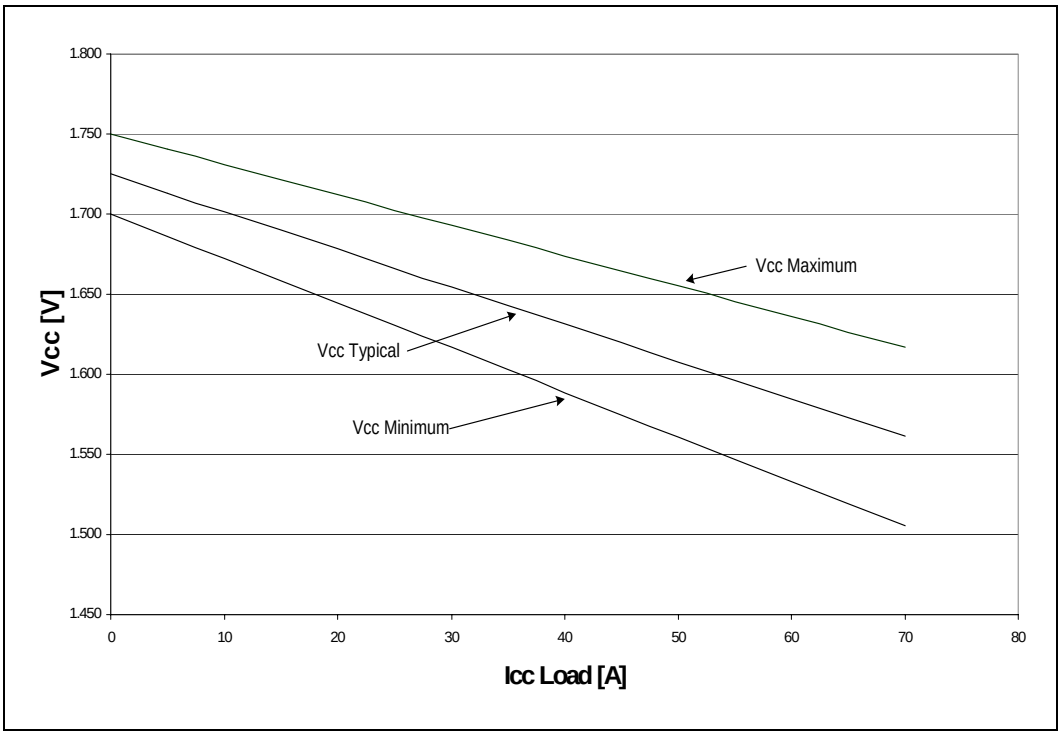
NOTES:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.4 and Table 2 for more information.
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE pins at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
4. Refer to Table 7 and Figure 3 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current. Moreover, V_{CC} should never exceed the VID voltage. Failure to adhere to this specification can shorten the processor lifetime.
5. V_{CC_MIN} is defined at I_{CC_MAX}.
6. The current specified is also for AutoHALT State.
7. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
8. I_{CC} Stop-Grant and I_{CC} Sleep are specified at V_{CC_MAX}.
9. These specifications apply to processors with a VID setting of 1.75 V.

Table 7. VCC Static and Transient Tolerance

Icc (A)	Voltage Deviation from VID Setting (V)[1, 2, 3]		
	Maximum	Typical	Minimum
0	0.000	–0.025	–0.050
5	–0.010	–0.037	–0.064
10	–0.019	–0.048	–0.078
15	–0.029	–0.060	–0.092
20	–0.038	–0.072	–0.106
25	–0.048	–0.083	–0.120
30	–0.057	–0.095	–0.133
35	–0.067	–0.107	–0.147
40	–0.076	–0.119	–0.161
45	–0.085	–0.130	–0.175
50	–0.095	–0.142	–0.189
55	–0.105	–0.154	–0.203
60	–0.114	–0.165	–0.217
65	–0.124	–0.177	–0.231
70	–0.133	–0.189	–0.245

NOTES:
1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 3.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* for socket loadline guidelines and VR implementation details.

Figure 3. VCC Static and Transient Tolerance



NOTES:
1. The loadline specification includes both static and transient limits.
2. This loadline specification applies to processors with a VID setting of 1.75 V.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* for socket loadline guidelines and VR implementation details.

Table 8. System Bus Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_L	Input Low Voltage	–.150	0.000	N/A	V	6	
V_H	Input High Voltage	0.660	0.710	0.850	V	6	
$V_{CROSS(abs)}$	Absolute Crossing Point	0.250	N/A	0.550	V	6, 7	2, 3, 8
$V_{CROSS(rel)}$	Relative Crossing Point	0.250 + 0.5(V_{Havg} - 0.71)	N/A	0.550 + 0.5(V_{Havg} - 0.71)	V	6, 7	2, 3, 8, 9
ΔV_{CROSS}	Range of Crossing Points	N/A	N/A	0.140	V	6, 7	2, 10
V_{OV}	Overshoot	N/A	N/A	V_H + 0.3	V	6	4
V_{US}	Undershoot	– 0.3	N/A	N/A	V	6	5
V_{RBM}	Ringback Margin	0.200	N/A	N/A	V	6	6
V_{TM}	Threshold Margin	V_{CROSS} - 0.100	N/A	V_{CROSS} + 0.100	V	6	7

NOTES:.
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 equals the falling edge of BCLK1.
3. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
4. Overshoot is defined as the absolute value of the maximum voltage.
5. Undershoot is defined as the absolute value of the minimum voltage.
6. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
7. Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
9. V_{Havg} can be measured directly using *Vtop* on Agilent* scopes and *High* on Tektronix* scopes.
10. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.

Table 9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	GTLREF - 0.100	V	2, 6
V_{IH}	Input High Voltage	GTLREF + 0.100	V_{CC}	V	3, 4, 6
V_{OH}	Output High Voltage	N/A	V_{CC}	V	4, 6
I_{OL}	Output Low Current	N/A	64	mA	7
I_{LI}	Input Leakage Current	N/A	± 100	µA	
I_{LO}	Output Leakage Current	N/A	± 100	µA	
R_{ON}	Buffer On Resistance	5	11	W	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. v_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. Refer to processor I/O Buffer Models for I/V characteristics.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
7. V_{OL_MAX} of 0.560 V is guaranteed when driving into a test load of 50 ohms as indicated in Figure 4, with R_{TT} enabled.

Table 10. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	GTLREF-0.100		3
V_{IH}	Input High Voltage	GTLREF+0.100	V_{CC}		4, 5, 7
V_{OH}	Output High Voltage		V_{CC}	V	2, 5, 7
I_{OL}	Output Low Current		64	mA	8, 9
I_{LI}	Input Leakage Current	N/A	± 100	µA	
I_{LO}	Output Leakage Current	N/A	± 100	µA	
R_{ON}	Buffer On Resistance	5	11	W	6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
6. Refer to the processor I/O Buffer Models for I/V characteristics.
7. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
8. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
9. V_{OL_MAX} of 0.560 V is guaranteed when driving into a test load of 50 ohms as indicated in Figure 4, with R_{TT} enabled.

Table 11. PWRGOOD and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1, 2]
V_{HYS}	Input Hysteresis	200	300	mV	8
V_{T+}	Input low to high threshold voltage	1/2 * (V_{CC} + V_{HYS_MIN})	1/2 * (V_{CC} + V_{HYS_MAX})	V	5
V_{T-}	Input high to low threshold voltage	1/2 * (V_{CC} - V_{HYS_MAX})	1/2 * (V_{CC} - V_{HYS_MIN})	V	5
V_{OH}	Output High Voltage	N/A	V_{CC}	V	3, 5
I_{OL}	Output Low Current		45	mA	6, 7
I_{LI}	Input Leakage Current		± 100	µA	
I_{LO}	Output Leakage Current		± 100	µA	
R_{ON}	Buffer On Resistance	6.25	13.25	W	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. All outputs are open drain
3. The TAP signal group must meet the signal quality specifications in Chapter 3.0.
4. Refer to the processor I/O Buffer Models for I/V characteristics.
5. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
7. V_{OL_MAX} of 0.360 V is guaranteed when driving into a test load as indicated in Figure 4.
8. V_{HYS} represents the amount of hysteresis, nominally centered about 1/2 V_{CC}, for all TAP inputs.

2.11 AGTL+ System Bus Specifications

Routing topology recommendations may be found in the appropriate Platform Design Guide as referenced in Table 1. Termination resistors are not required for most AGTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

Table 12 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on platform design see the Platform Design Guide.

Table 12. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF	Bus Reference Voltage	2/3 VCC - 2%	2/3 VCC	2/3 VCC + 2%	V	2, 3, 6
R_{TT}	Termination Resistance	45	50	55	W	4
COMP[1:0]	COMP Resistance	50.49	51	51.51	W	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of VCC.
3. GTLREF should be generated from VCC by a voltage divider of 1% resistors or 1% matched resistors. Refer to Table 1 for the appropriate Platform Design Guide for implementation details.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Refer to processor I/O buffer models for I/V characteristics.
5. COMP resistance must be provided on the system board with 1% resistors. See the appropriate platform design guide for implementation details.
6. The VCC referred to in these specifications is the instantaneous VCC.

2.12 System Bus AC Specifications

The processor system bus timings specified in this section are defined at the processor core silicon and are thus not measurable at the processor pins. See Chapter 5.0 for the Celeron processor in the 478-pin package pin signal definitions.

Table 14 through Table 18 list the AC specifications associated with the processor system bus.

All AGTL+ timings are referenced to GTLREF for both ‘0’ and ‘1’ logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Celeron processor in the 478-pin package in IBIS format. AGTL+ layout guidelines are also available in the appropriate Platform Design Guide.

Care should be taken to read all notes associated with a particular timing parameter.

Table 13. System Bus Differential Clock Specifications

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
System Bus Frequency			100	MHz		
T1: BCLK[1:0] Period	10.0		10.2	ns	6	2
T2: BCLK[1:0] Period Stability			200	ps	6	3, 4
T3: BCLK[1:0] High Time	3.94	5	6.12	ns	6	
T4: BCLK[1:0] Low Time	3.94	5	6.12	ns	6	
T5: BCLK[1:0] Rise Time	175		700	ps	6	5
T6: BCLK[1:0] Fall Time	175		700	ps	6	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor core frequencies.
2. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2).
3. For the clock jitter specification, refer to the *CK408 Clock Design Guidelines*.
4. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
5. Slew rate is measured between the 35% and 65% points of the clock swing (V_L to V_H).

Table 14. System Bus Common Clock AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3]
T10: Common Clock Output Valid Delay	0.200	1.45	ns	8	4
T11: Common Clock Input Setup Time	0.65	N/A	ns	8	5
T12: Common Clock Input Hold Time	0.40	N/A	ns	8	5
T13: RESET# Pulse Width	1.00	10.00	ms	9	6, 7, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
4. Valid delay timings for these signals are specified into the test circuit described in Figure 4 and with GTLREF at 2/3 V_{CC} ± 2%.
5. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.4 V/ ns to 4.0 V/ns.
6. RESET# can be asserted asynchronously, but must be deasserted synchronously.
7. This should be measured after V_{CC} and BCLK[1:0] become stable.
8. Maximum specification applies only while PWRGOOD is asserted.

Table 15. System Bus Source Synch AC Specifications AGTL+ Signal Group

T# Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2,3,4]
T20: Source Synchronous Data Output Valid Delay (first data/address only)	0.20		1.20	ns	10, 11	5
T21: T_{VBD}: Source Synchronous Data Output Valid Before Strobe	0.85			ns	11	5, 8
T22: T_{VAD}: Source Synchronous Data Output Valid After Strobe	0.85			ns	11	5, 8
T23: T_{VBA}: Source Synchronous Address Output Valid Before Strobe	1.88			ns	10	5, 8
T24: T_{VAA}: Source Synchronous Address Output Valid After Strobe	1.88			ns	10	5, 9
T25: T_{SUSS}: Source Synchronous Input Setup Time to Strobe	0.21			ns	10, 11	6
T26: T_{HSS}: Source Synchronous Input Hold Time to Strobe	0.21			ns	10, 11	6
T27: T_{SUCC}: Source Synchronous Input Setup Time to BCLK[1:0]	0.65			ns	10, 11	7
T28: T_{FASS}: First Address Strobe to Second Address Strobe		1/2		BCLK	10	10
T29: T_{FDSS}: First Data Strobe to Subsequent Strobes		n/4		BCLK	11	11, 12
T30: Data Strobe ‘n’ (DSTBN#) Output Valid Delay	8.80		10.20	ns	11	13
T31: Address Strobe Output Valid Delay	2.27		4.23	ns	10	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. Not 100% tested. Specified by design characterization.
3. All source synchronous AC timings are referenced to their associated strobe at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core.
4. Unless otherwise noted these specifications apply to both data and address timings.
5. Valid delay timings for these signals are specified into the test circuit described in Figure 4 and with GTLREF at 2/3 V_{CC} ± 2%.
6. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.3 V/ns to 4.0 V/ns.
7. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
8. This specification represents the minimum time the data or address will be valid before its strobe. Refer to Table 1 for the appropriate Platform Design *Guide* for more information on the definitions and use of these specifications.
9. This specification represents the minimum time the data or address will be valid after its strobe. Refer to Table 1 for the appropriate Platform Design Guide for more information on the definitions and use of these specifications.
10. The rising edge of ADSTB# must come approximately 1/2 BCLK period (5 ns) after the falling edge of ADSTB#.
11. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
12. The second data strobe (falling edge of DSTBn#) must come approximately 1/4 BCLK period (2.5 ns) after the first falling edge of DSTBp#. The third data strobe (falling edge of DSTBp#) must come approximately 2/4 BCLK period (5 ns) after the first falling edge of DSTBp#. The last data strobe (falling edge of DSTBn#) must come approximately 3/4 BCLK period (7.5 ns) after the first falling edge of DSTBp#.
13. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.

Table 16. Miscellaneous Signals AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3,6]
T35: Asynch GTL+ Input Pulse Width	2		BCLKs		
T36: PWRGOOD to RESET# de-assertion time	1	10	ms	12	
T37: PWRGOOD Inactive Pulse Width	10		BCLKs	12	4
T38: PROCHOT# pulse width	500		us	14	5
T39: THERMTRIP# Assertion until V_{CC} removal		0.5	s	13	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All AC timings for the Asynch GTL+ signals are referenced to the BCLK0 rising edge at Crossing Voltage. All Asynch GTL+ signal timings are referenced at GTLREF. PWRGOOD is referenced to the BCLK0 rising edge at 0.5 * VCC.
3. These signals may be driven asynchronously.
4. Refer to the PWRGOOD definition for more details regarding the behavior of this signal.
5. Length of assertion for PROCHOT# does not equal internal clock modulation time. Time is allocated after the assertion and before the deassertion of PROCHOT# for the processor to complete current instruction execution.
6. See section Section 7.2 for additional timing requirements for entering and leaving the low power states.

Table 17. System Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes
T45: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Setup Time	4		BCLKs	9	1
T46: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Hold Time	2	20	BCLKs	9	2

NOTES:
1. Before the deassertion of RESET#.
2. After clock that deasserts RESET#.

Table 18. TAP Signals AC Specifications

Parameter	Min	Max	Unit	Figure	Notes[1,2,3,9]
T55: TCK Period	60.0		ns	5	
T56: TCK Rise Time		9.5	ns	5	4
T57: TCK Fall Time		9.5	ns	5	4
T58: TMS, TDI Rise Time		8.5	ns	5	4
T59: TMS, TDI Fall Time		8.5	ns	5	4
T61: TDI, TMS Setup Time	0		ns	15	5, 7
T62: TDI, TMS Hold Time		3	ns	15	5, 7
T63: TDO Clock to Output Delay	0.5	3.5	ns	15	6
T64: TRST# Assert Time	2		TCK	14	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the TAP signals are referenced to the TCK signal at 0.5 VCC at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at 0.5 * VCC at the processor pins.
4. Rise and fall times are measured from the 20% to 80% points of the signal swing.
5. Referenced to the rising edge of TCK.
6. Referenced to the falling edge of TCK.
7. Specification for a minimum swing defined between TAP 20% to 80% points on the waveform. This assumes a minimum edge rate of 0.5 V/ns.
8. TRST# must be held asserted for 2 TCK periods to be guarantee that it is recognized by the processor.
9. It is recommended that TMS be asserted while TRST# is being deasserted.

2.13 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 14 through Table 18.

Note: For Figure 5 through Figure 14, the following apply:

- All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
- All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor silicon.
- All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at V_{CROSS}. All AGTL+ strobe signal timings are referenced at GTLREF at the processor silicon.
- All AC timings for the TAP signals are referenced to the TCK signal at 0.5 * VCC at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at 0.5 * VCC at the processor pins.

The circuit used to test the AC specifications is shown in Figure 4.

Figure 4. AC Test Circuit

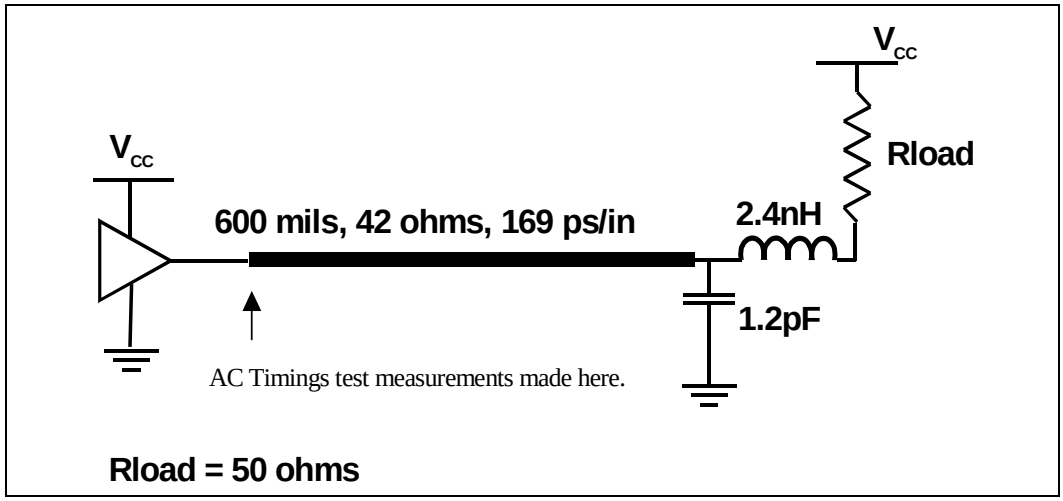


Figure 5. TCK Clock Waveform

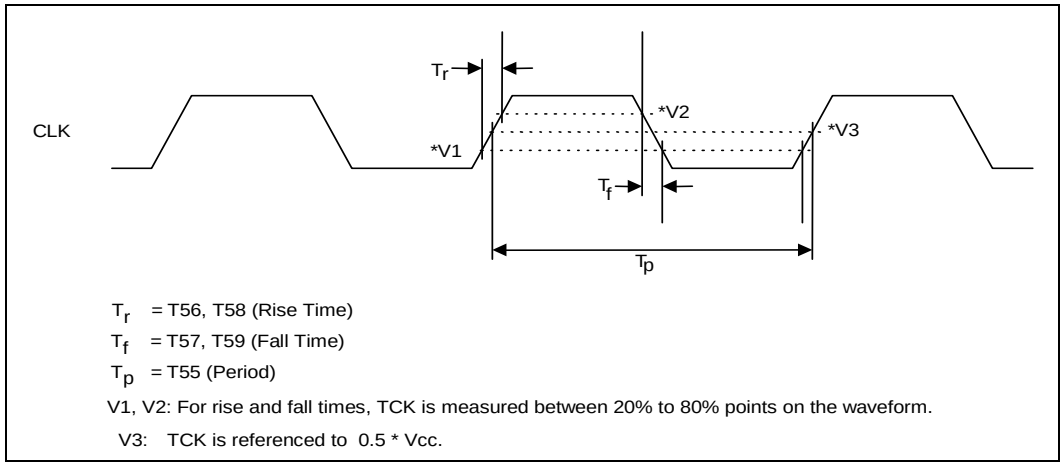
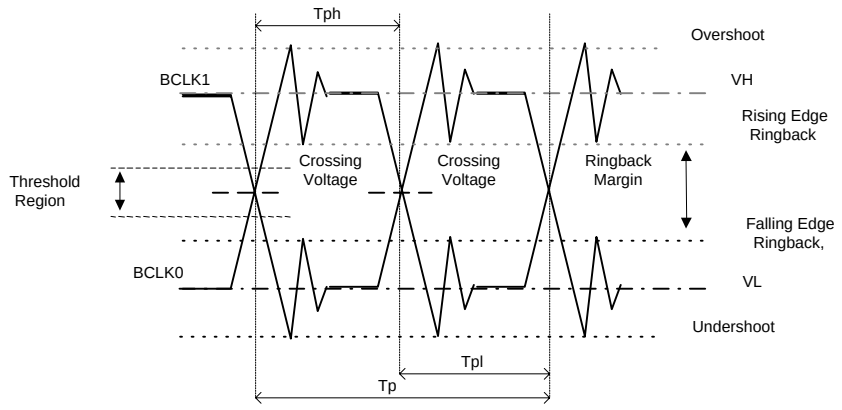


Figure 6. Differential Clock Waveform



Tp = T1 (BCLK[1:0] period)
T2 = BCLK[1:0] Period stability (not shown)
Tph =T3 (BCLK[1:0] pulse high time)
Tpl = T4 (BCLK[1:0] pulse low time)
T5 = BCLK[1:0] rise time through the threshold region
T6 = BCLK[1:0] fall time through the threshold region

Figure 7. Differential Clock Crosspoint Specification

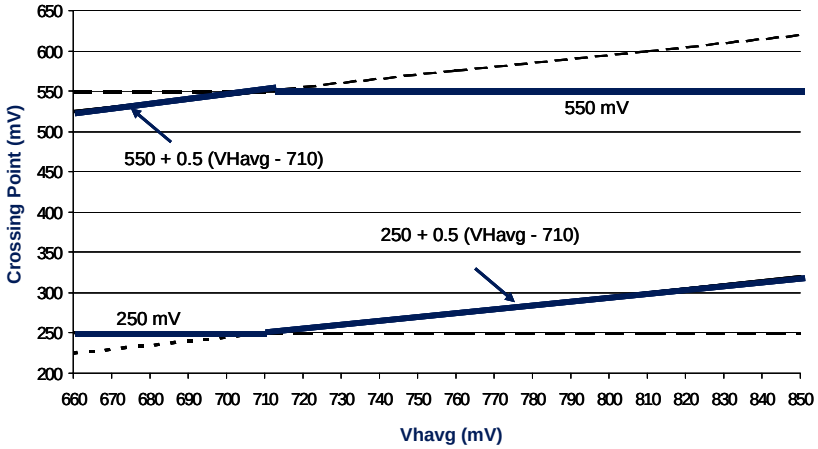


Figure 8. System Bus Common Clock Valid Delay Timings

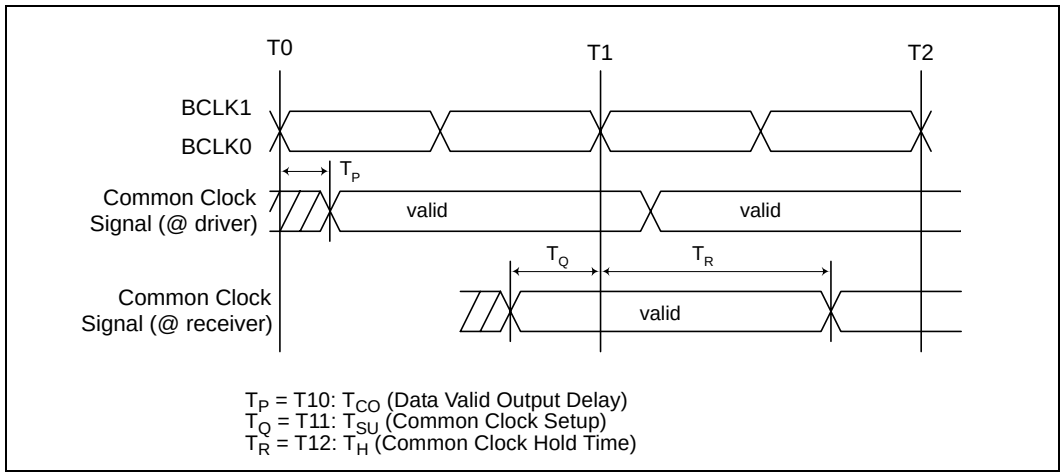


Figure 9. System Bus Reset and Configuration Timings

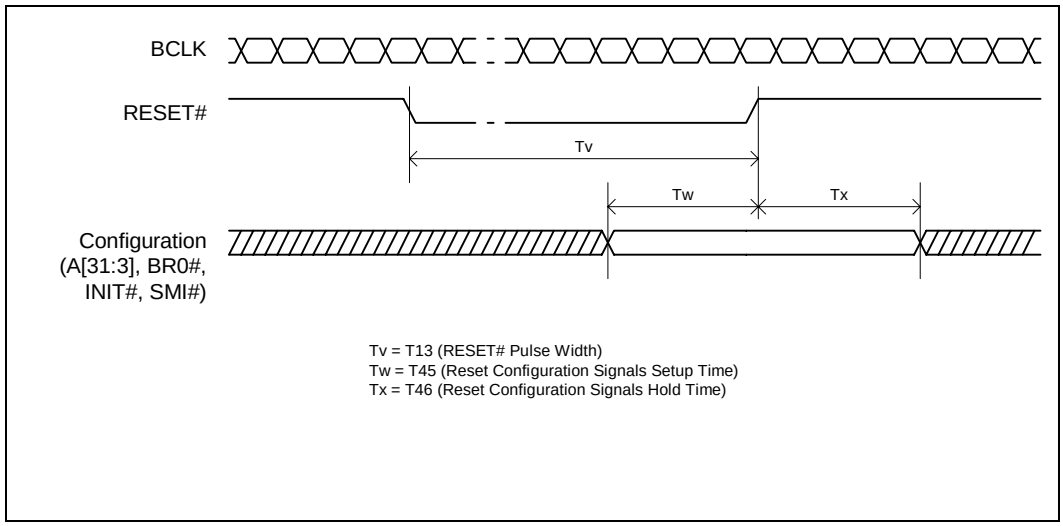
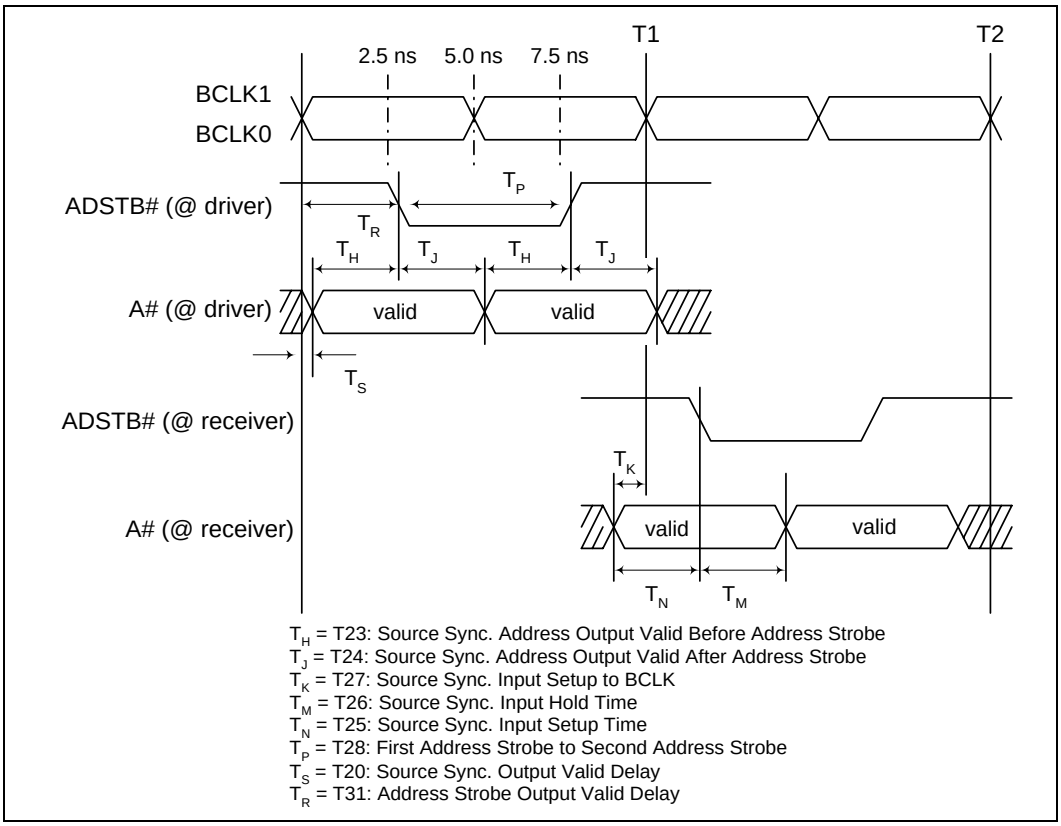
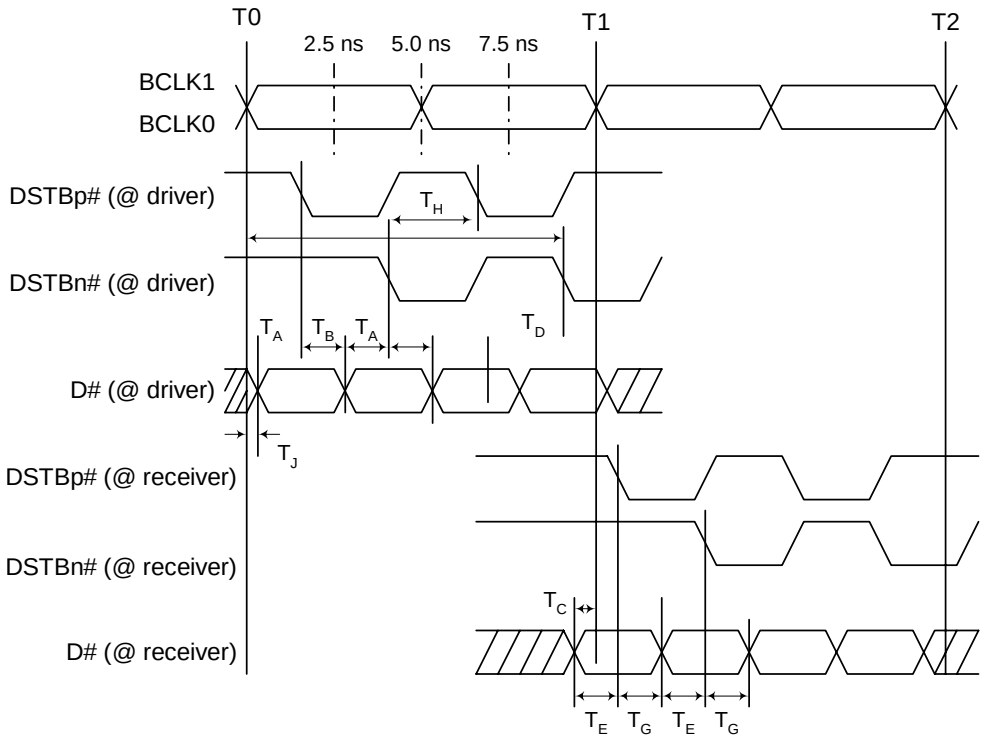


Figure 10. Source Synchronous 2X (Address) Timings



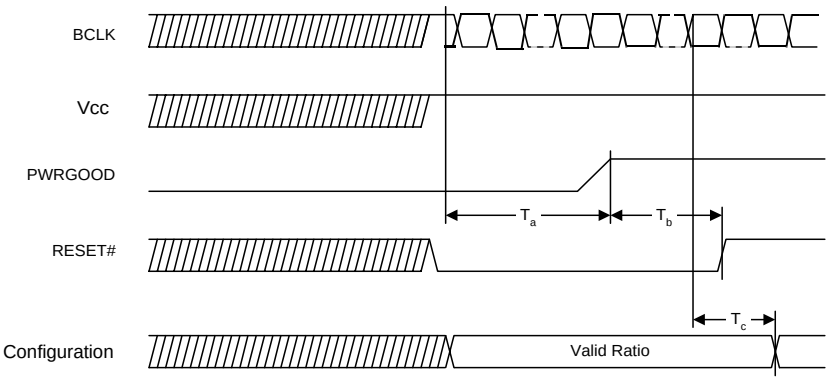
T_H = T23: Source Sync. Address Output Valid Before Address Strobe
T_J = T24: Source Sync. Address Output Valid After Address Strobe
T_K = T27: Source Sync. Input Setup to BCLK
T_M = T26: Source Sync. Input Hold Time
T_N = T25: Source Sync. Input Setup Time
T_P = T28: First Address Strobe to Second Address Strobe
T_S = T20: Source Sync. Output Valid Delay
T_R = T31: Address Strobe Output Valid Delay

Figure 11. Source Synchronous 4X Timings



T_A = T21: Source Sync. Data Output Valid Delay Before Data Strobe
T_B = T22: Source Sync. Data Output Valid Delay After Data Strobe
T_C = T27: Source Sync. Setup Time to BCLK
T_D = T30: Source Sync. Data Strobe 'N' (DSTBN#) Output Valid Delay
T_E = T25: Source Sync. Input Setup Time
T_G = T26: Source Sync. Input Hold Time
T_H = T29: First Data Strobe to Subsequent Strobes
T_J = T20: Source Sync. Data Output Valid Delay

Figure 12. Power-On Reset and Configuration Timings



Ta = T37 (PWRGOOD Inactive Pulse Width)
Tb = T36 (PWRGOOD to RESET# de-assertion time)
Tc = T46, (Reset Configuration Signals Hold Time)

Figure 13. THERMTRIP# Power Down Sequenc e

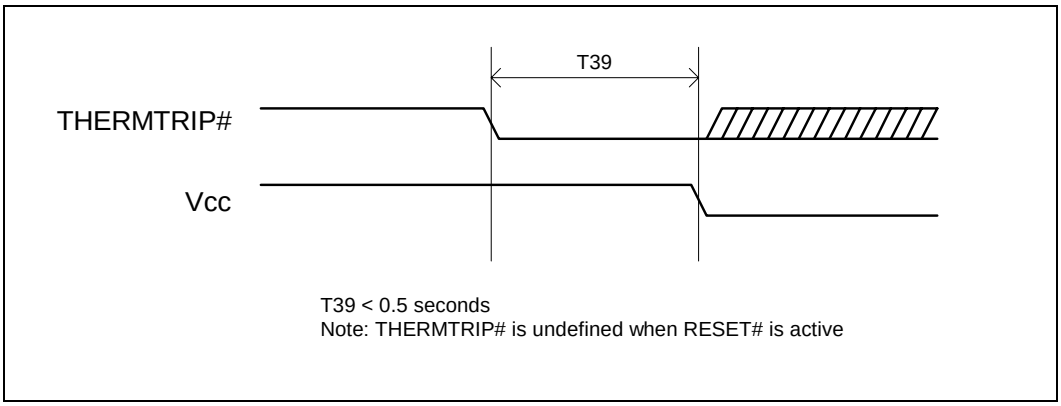


Figure 14. Test Reset (TRST#), Async GTL+ Input, and PROCHOT# Timing Waveform

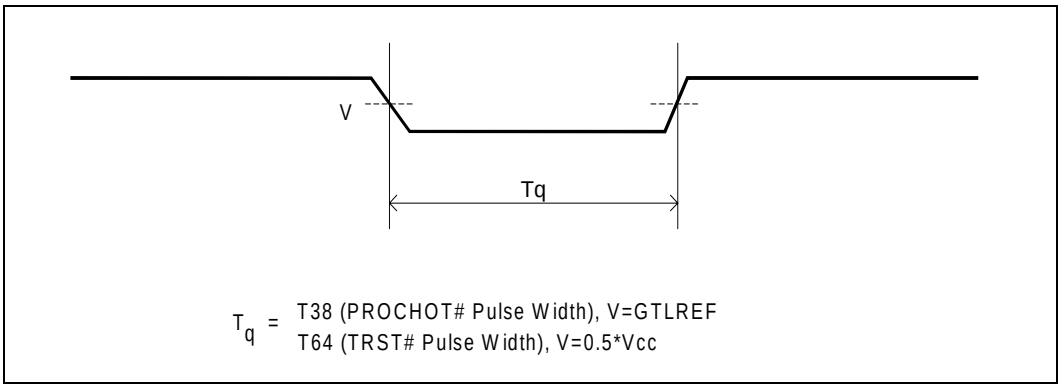
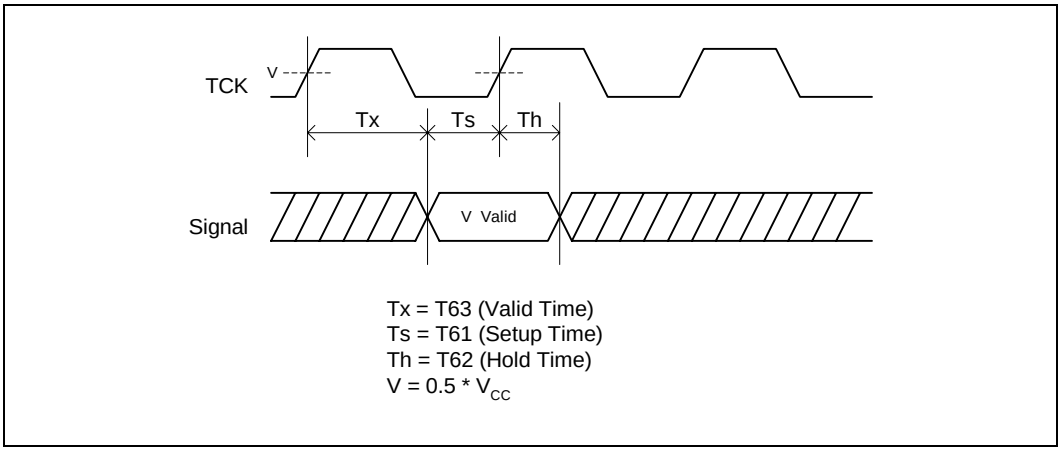


Figure 15. TAP Valid Delay Timing Waveform



3.0 System Bus Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Ringback and signal non-monotinicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, overshoot and undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is important that the designer work to achieve a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation, and all specifications are at the processor silicon and cannot be measured at the processor pins.

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. The same is true for all system bus AC timing specifications in Section 2.12. Therefore, proper simulation of the Celeron processor in the 478-pin package system bus is the only means to verify proper timing and signal quality metrics, and Intel highly recommends simulation during system design and measurement during system analysis.

3.1 BCLK Signal Quality Specifications and Measurement Guidelines

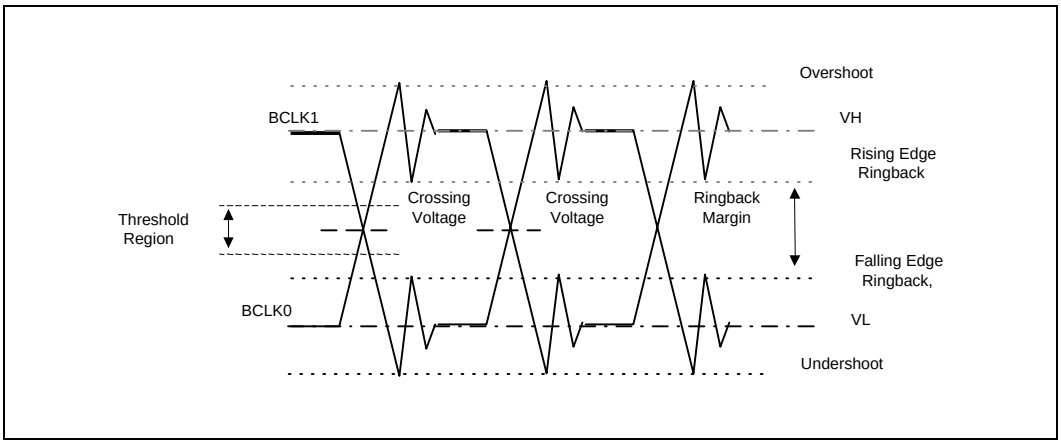
Table 19 describes the signal quality specifications at the processor silicon for the processor system bus clock (BCLK) signals. Figure 16 describes the signal quality waveform for the system bus clock at the processor silicon. Specifications are defined at the processor silicon, not the 478-pin socket pins.

Table 19. BCLK Signal Quality Specifications

Parameter	Min	Max	Unit	Figure	Notes[1]
BCLK[1:0] Overshoot	N/A	0.30	V	16	
BCLK[1:0] Undershoot	N/A	0.30	V	16	
BCLK[1:0] Ringback Margin	0.20	N/A	V	16	
BCLK[1:0] Threshold Region	N/A	0.20	V	16	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor in the 478-pin package frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 16. BCLK Signal Integrity Waveform



3.2 System Bus Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines that are available in the Platform Design Guidelines.

Table 20 provides the signal quality specifications for all processor signals for use in simulating signal quality at the processor silicon.

The Celeron processor in the 478-pin package maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 22 through Table 25. Figure 17 shows the system bus ringback tolerance for low-to-high transitions and Figure 18 shows ringback tolerance for high-to-low transitions.

Table 20. Ringback Specifications for AGTL+ and Asynchronous GTL+ Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
All Signals	0 → 1	GTLREF + 0.100	V	17	1,2,3,4,5,6,7
All Signals	1 → 0	GTLREF - 0.100	V	18	1,2,3,4,5,6,7

NOTES:
1. All signal integrity specifications are measured at the processor silicon.
2. Unless otherwise noted, all specifications in this table apply to all Celeron processor in the 478-pin package frequencies and cache sizes.
3. Specifications are for the edge rate of 0.3 – 4.0 V/ns.
4. All values specified by design characterization.
5. Ringback between GTLREF + 100 mV and GTLREF – 100 mV is not supported.
6. Intel recommends simulations not exceed a ringback value of GTLREF ± 200 mV to allow margin for other sources of system noise.

Table 21. Ringback Specifications for TAP and PWRGOOD Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
TAP and PWRGOOD	0 → 1	Vt+ (max) to Vt– (max)	V	19	1,2,3
TAP and PWRGOOD	1 → 0	Vt– (min) to Vt+ (min)	V	20	1,2,3

NOTES:
1. All signal integrity specifications are measured at the processor silicon.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. See Section 2.10 for the DC specifications.

Figure 17. Low-to-High System Bus Receiver Ringback Tolerance

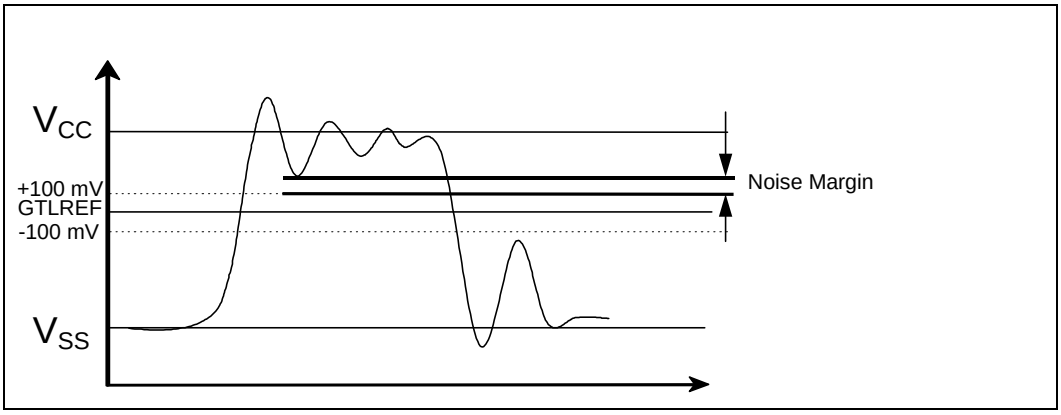


Figure 18. High-to-Low System Bus Receiver Ringback Tolerance

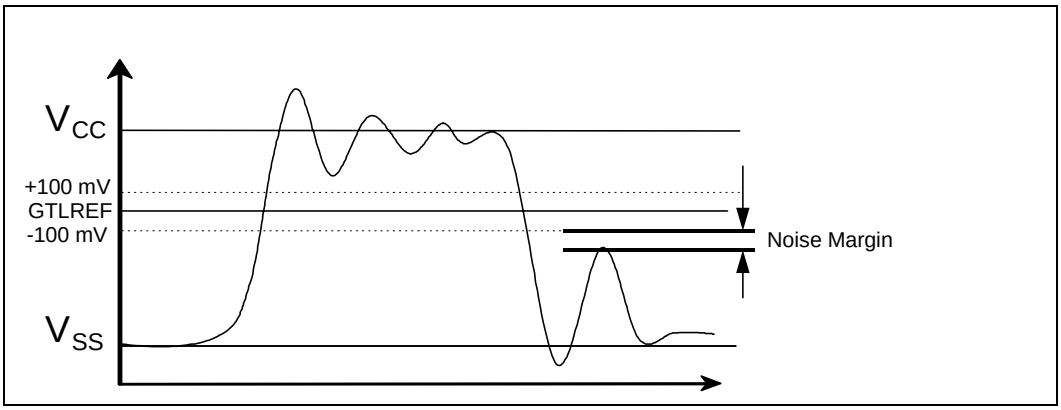


Figure 19. Low-to-High System Bus Receiver Ringback Tolerance for TAP and PWRGOOD Buffers

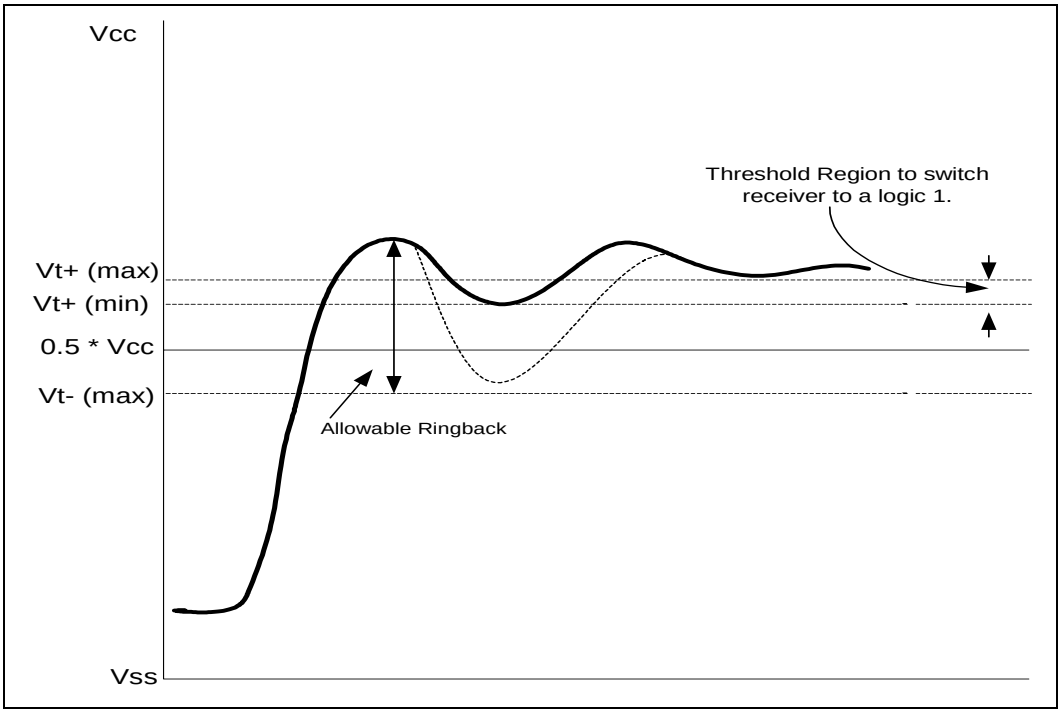
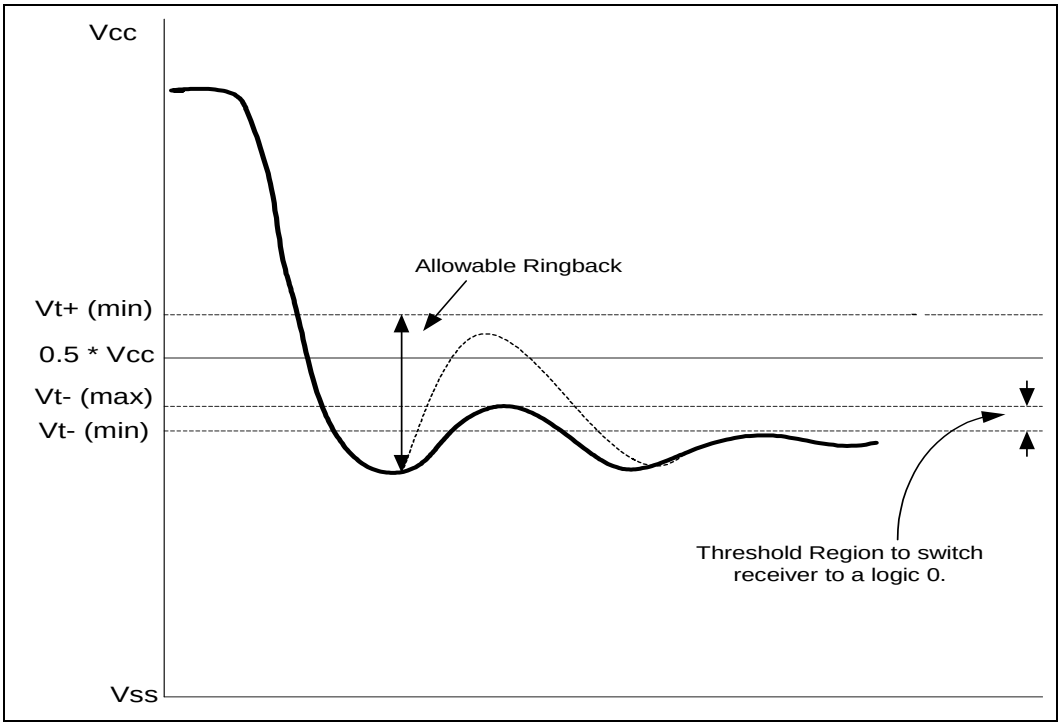


Figure 20. High-to-Low System Bus Receiver Ringback Tolerance for TAP and PWRGOOD Buffers



3.2.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage (or below VSS) as shown in Figure 21. The overshoot/undershoot guidelines limit transitions beyond VCC or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction, and the activity factor (AF) of the incident waveform. Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modelled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the Celeron processor in the 478-pin package system bus, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

3.2.1.1 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the Celeron processor in the 478-pin package both are referenced to VSS. It is important to note that overshoot and undershoot conditions are separate and their impact must be determined independently.

Overshoot/undershoot magnitude levels must observe the absolute maximum specifications listed in Table 22 through Table 25. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the absolute maximum specifications (2.3 V for overshoot and -0.65 V for undershoot), the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.2.1.2 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage (maximum overshoot = 2.3 V, maximum undershoot = -0.65 V). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage can not be subtracted from the total overshoot/undershoot pulse duration.

3.2.1.3 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

For source synchronous signals (address, data, and associated strobes), the activity factor is in reference to the strobe edge, since the highest frequency of assertion of any source synchronous signal is every active edge of its associated strobe. An AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every strobe cycle.

The specifications provided in Table 22 through Table 25 show the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Notes:

1. Activity factor for AGTL+ signals is referenced to BCLK[1:0] frequency.
2. Activity factor for source synchronous (2x) signals is referenced to ADSTB[1:0]#.
3. Activity factor for source synchronous (4x) signals is referenced to DSTBP[3:0]# and DSTBN[3:0]#.

3.2.1.4 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the Celeron processor in the 478-pin package is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the *signal group* a particular signal falls into. For AGTL+ signals operating in the common clock domain, use Table 24. For AGTL+ signals operating in the 2x source synchronous domain, use Table 23. For AGTL+ signals operating in the 4x source synchronous domain, use Table 22. Finally, all other signals reside in the 33 MHz domain (asynchronous GTL+, TAP, etc.) and are referenced in Table 25.
2. Determine the *magnitude* of the overshoot (relative to V_{SS})
3. Determine the *activity factor* (how often does this overshoot occur?)
4. Next, from the appropriate specification table, determine the *maximum pulse duration* (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

3.2.1.5 Determining if a System Meets the Over/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below. Results from simulation may also be evaluated by utilizing the *Intel® Pentium® 4 Processor in the 478-pin Package Overshoot Checker* through the use of time-voltage data files.

- Ensure no signal ever exceeds VCC_MAX or –0.25 V OR
- If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables OR
- If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

Notes: The following notes apply to Table 22 through Table 25.

1. Absolute Maximum Overshoot magnitude of 2.3 V must never be exceeded.
2. Absolute Maximum Overshoot is measured relative to VSS, Pulse Duration of overshoot is measured relative to VCC.
3. Absolute Maximum Undershoot and Pulse Duration of undershoot is measured relative to VCC.
4. Ringback below VCC can not be subtracted from overshoots/undershoots.
5. Lesser undershoot does not allocate longer or larger overshoot.
6. OEM's are strongly encouraged to follow Intel provided layout guidelines.
7. All values specified by design characterization.

Table 22. Source Synchronous (400 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
2.30	–0.585	0.06	0.63	5.00
2.25	–0.535	0.11	1.10	5.00
2.20	–0.485	0.22	2.20	5.00
2.15	–0.435	0.41	4.10	5.00
2.10	–0.385	0.75	5.00	5.00
2.05	–0.335	1.35	5.00	5.00
2.00	–0.285	2.50	5.00	5.00
1.95	–0.235	4.70	5.00	5.00
1.90	–0.185	5.00	5.00	5.00
1.85	–0.135	5.00	5.00	5.00
1.80	–0.085	5.00	5.00	5.00

NOTES:
1. These specifications are measured at the processor silicon.
2. BCLK period is 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 23. Source Synchronous (200 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
2.30	–0.585	0.12	1.2	10.0
2.25	–0.535	0.22	2.2	10.0
2.20	–0.485	0.44	4.4	10.0
2.15	–0.435	0.82	8.2	10.0
2.10	–0.385	1.5	10.0	10.0
2.05	–0.335	2.7	10.0	10.0
2.00	–0.285	5.0	10.0	10.0
1.95	–0.235	9.4	10.0	10.0
1.90	–0.185	10.0	10.0	10.0
1.85	–0.135	10.0	10.0	10.0
1.80	–0.085	10.0	10.0	10.0

NOTES:
1. These specifications are measured at the processor silicon.
2. BCLK period is 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 24. Common Clock (100 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
2.30	–0.585	0.24	2.4	20.0
2.25	–0.535	0.44	4.4	20.0
2.20	–0.485	0.88	8.8	20.0
2.15	–0.435	1.64	16.4	20.0
2.10	–0.385	3.0	20.0	20.0
2.05	–0.335	5.4	20.0	20.0
2.00	–0.285	10.0	20.0	20.0
1.95	–0.235	18.8	20.0	20.0
1.90	–0.185	20.0	20.0	20.0
1.85	–0.135	20.0	20.0	20.0
1.80	–0.085	20.0	20.0	20.0

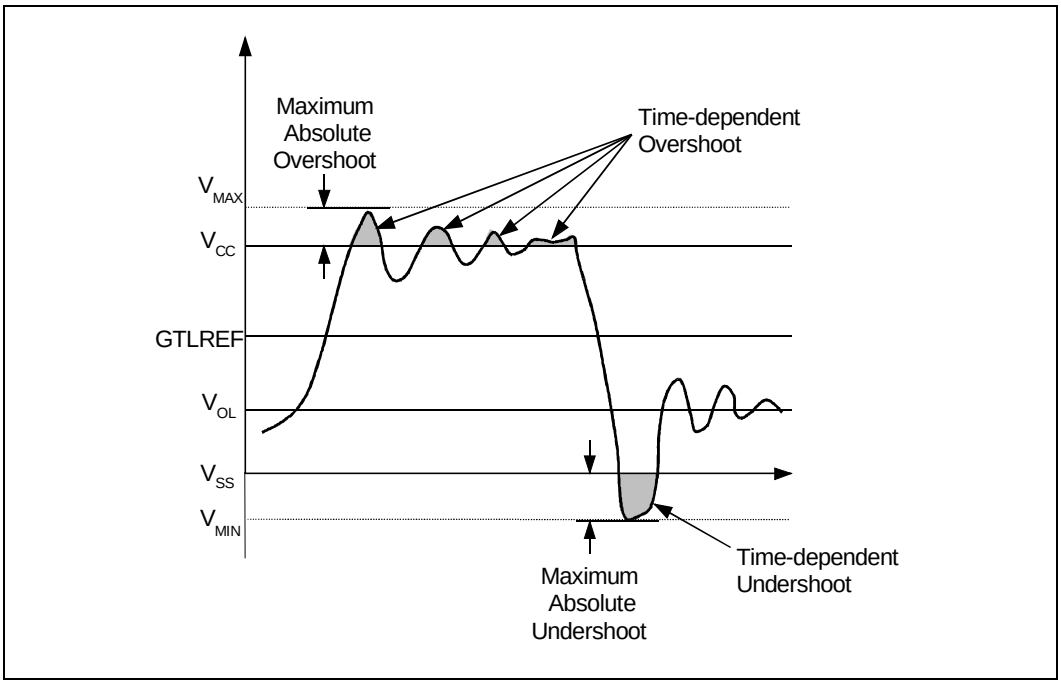
NOTES:
1. These specifications are measured at the processor silicon.
2. BCLK period is 10 ns.
3. AF is referenced to BCLK[1:0].

Table 25. Asynchronous GTL+, PWRGOOD, and TAP Signal Groups Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
2.30	–0.585	0.72	7.2	60.0
2.25	–0.535	1.32	13.2	60.0
2.20	–0.485	2.64	26.4	60.0
2.15	–0.435	4.92	49.2	60.0
2.10	–0.385	9.0	60.0	60.0
2.05	–0.335	16.2	60.0	60.0
2.00	–0.285	30.0	60.0	60.0
1.95	–0.235	56.4	60.0	60.0
1.90	–0.185	60.0	60.0	60.0
1.85	–0.135	60.0	60.0	60.0
1.80	–0.085	60.0	60.0	60.0

NOTES:
1. These specifications are specified at the processor silicon.
2. This table assumes a 33 MHz time domain.

Figure 21. Maximum Acceptable Overshoot/Undershoot Waveform



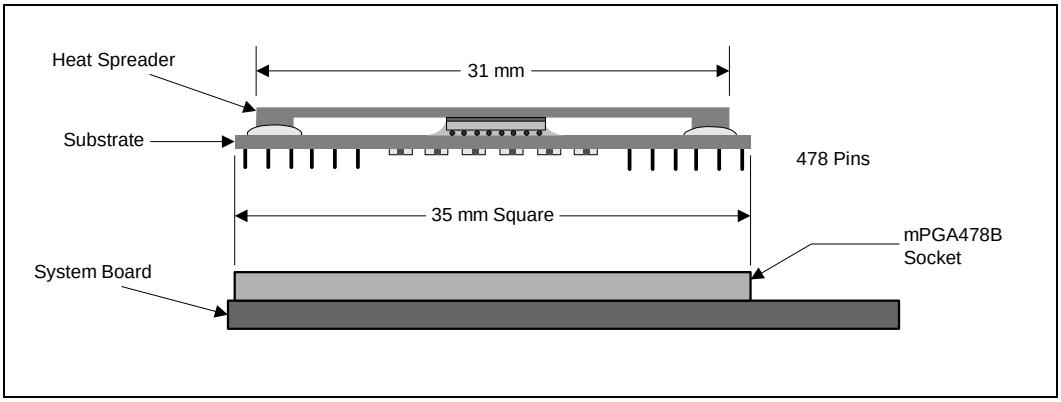
4.0 Package Mechanical Specifications

The Celeron processor in the 478-pin package is packaged in a Flip-Chip Pin Grid Array (FC-PGA2) package. Components of the package include an integrated heat spreader (IHS), processor core, and the substrate which is the pin carrier. Mechanical specifications for the processor are given in this section. See Section 1.1 for a terminology listing. The processor socket which accepts the Celeron processor in the 478-pin package is referred to as a 478-Pin micro PGA (mPGA478B) socket. See the *Intel® Pentium®4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines* for complete details on the mPGA478B socket.

Notes: The following notes apply to Figure 22 through Figure 27.

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.
2. All dimensions are not tested, but guaranteed by design characterization.
3. Figures and drawings labeled as “Reference Dimensions” are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are NOT checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
4. Drawings are not to scale.

Figure 22. Exploded View of Processor Components on a System Board



NOTE: The figure is not drawn to scale and is for reference only. The socket and system board are shown as a reference only.

Figure 23. Intel® Celeron® Processor in the 478-Pin Package

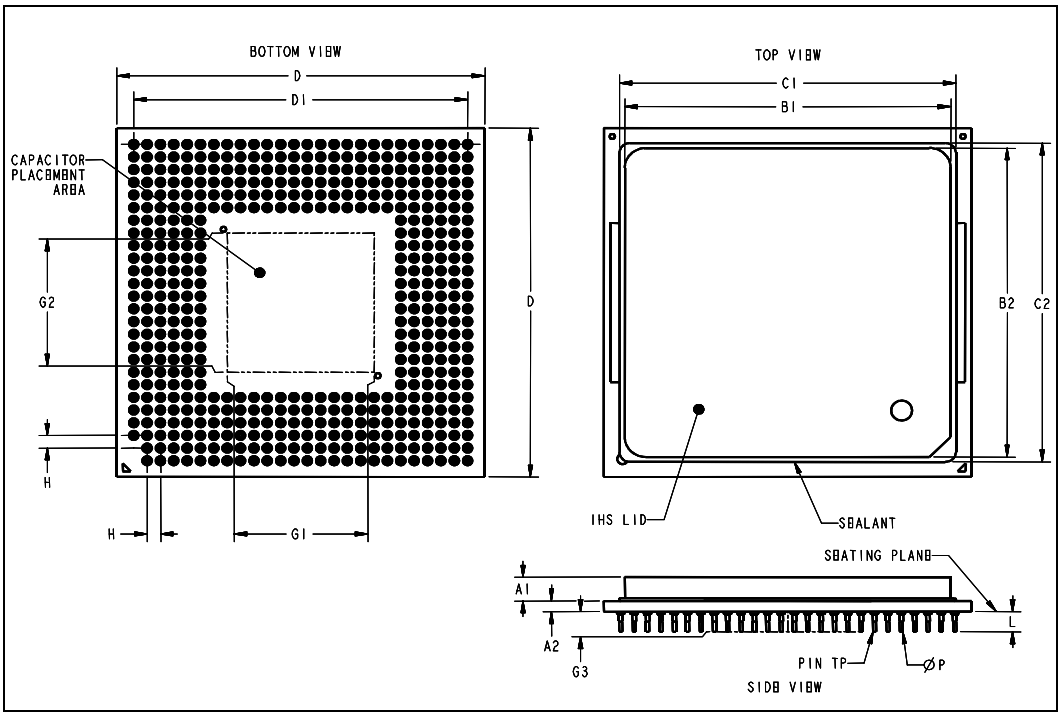


Table 26. Description Table for Processor Dimensions

Code Letter	Min (mm)	Nominal (mm)	Max (mm)	Notes
A1	2.266	2.378	2.490	
A2	0.980	1.080	1.180	
B1	30.800	31.000	31.200	
B2	30.800	31.000	31.200	
C1			33.000	Includes Placement Tolerance
C2			33.000	Includes Placement Tolerance
D	34.900	35.000	35.100	
D1	31.500	31.750	32.000	
G1			13.970	Keepin Zone Dimension
G2			13.970	Keepin Zone Dimension
G3			1.250	Keepin Zone Dimension
H		1.270		
L	1.950	2.030	2.110	
ϕP	0.280	0.305	0.330	
PIN TP			0.254	Diametric True Position (Pin-to-Pin)

Figure 24 details the keep in specification for pin-side components. The Celeron processor in the 478-pin package may contain pin side capacitors mounted to the processor package.

Figure 26 details the flatness and tilt specifications for the IHS. Tilt is measured with the reference datum set to the bottom of the processor interposer.

Figure 24. Processor Cross-Section and Keep-in

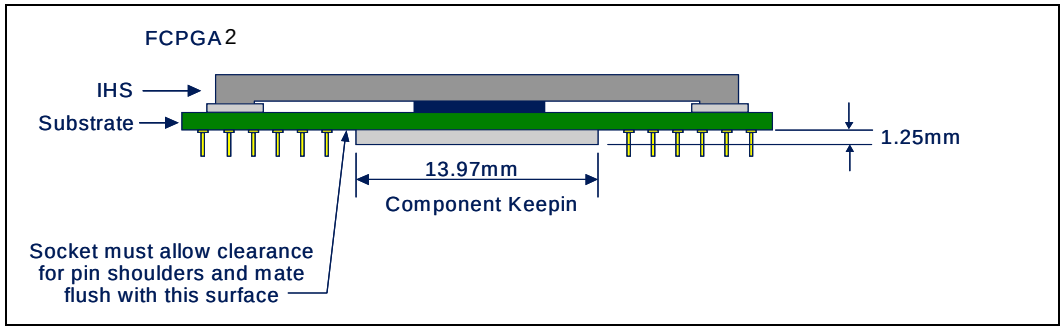
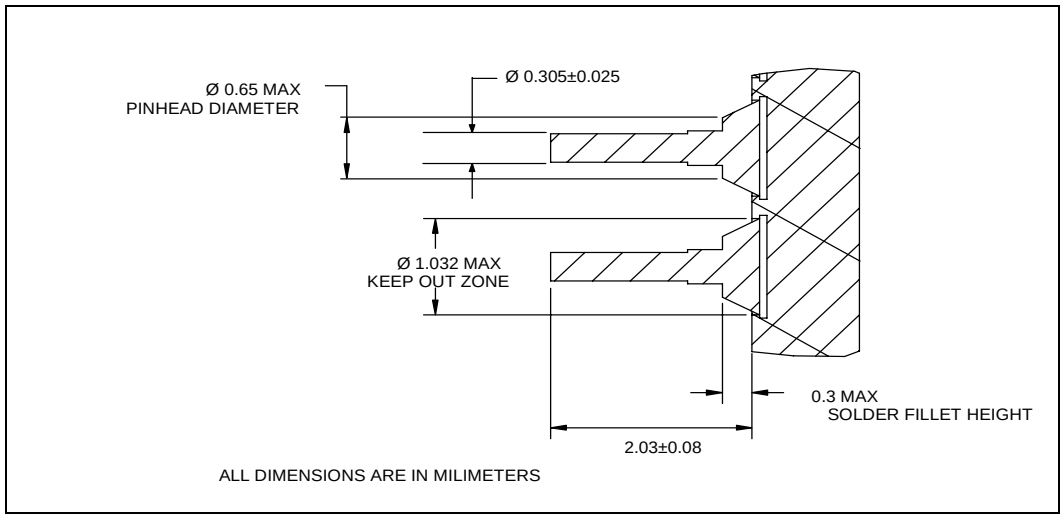
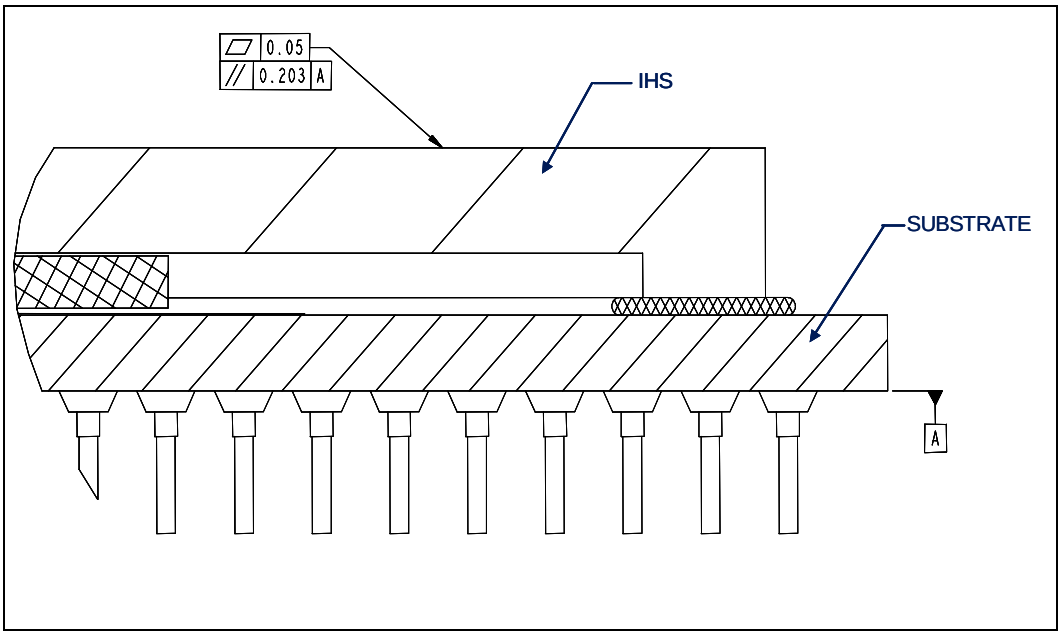


Figure 25. Processor Pin Detail



NOTES:
1. Pin plating consists of 0.2 micrometers Au over 2.0 micrometer Ni.
2. 0.254 mm diametric true position, pin to pin.

Figure 26. IHS Flatness Specification



NOTES:
1. Flatness is specific as overall, not per unit of length.
2. All dimensions are in mm.

4.1 Package Load Specifications

Table 27 provides dynamic and static load specifications for the Celeron processor in the 478-pin package IHS. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heat sink-to-processor thermal interface. It is not recommended to use any portion of the processor interposer as a mechanical reference or load bearing surface for thermal solutions.

Table 27. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Notes
Static	100	lbf	1, 2, 3
Dynamic	200	lbf	1, 3, 4

NOTES:
1. This specification applies to a uniform compressive load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. These parameters are based on limited testing for design characterization.
4. Dynamic loading specifications are defined assuming a maximum duration of 11ms and 200 lbf is achieved by superimposing a 100 lbf dynamic load (1 lbm heatsink at 50 g) on the static compressive load.

4.2 Processor Insertion Specifications

The Celeron processor in the 478-pin package can be inserted and removed 15 times from a mPGA478B socket that meets the specifications in the *Intel® Pentium®4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines*.

4.3 Processor Mass Specifications

Table 28 specifies the processor's mass. This includes all components which make up the entire processor product.

Table 28. Processor Mass

Processor	Mass (grams)
Celeron processor in the 478-pin package	19

4.4 Processor Materials

The Celeron processor in the 478-pin package is assembled from several components. The basic material properties are described in Table 29.

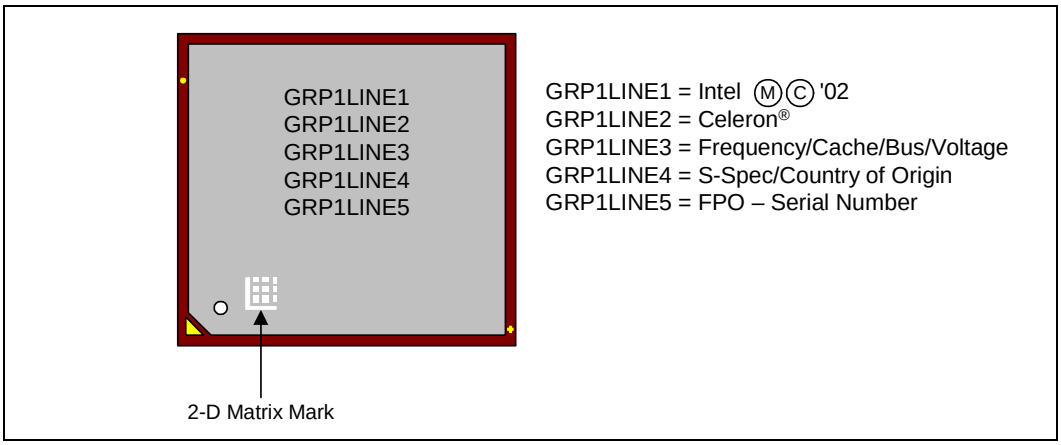
Table 29. Processor Material Properties

Component	Material
Integrated Heat Spreader	Nickel over copper
Substrate	Fiber-reinforced resin
Substrate pins	Gold over nickel

4.5 Processor Markings

Figure 27 details the processor top-side markings and is provided to aid in the identification of the Celeron processor in the 478-pin package.

Figure 27. Processor Markings



4.6 Processor Pin-Out Coordinates

Figure 28 and Figure 29 show the processor pin coordinates.

Figure 28. Processor Pinout Coordinates (Top View, Left Side)

	26	25	24	23	22	21	20	19	18	17	16	15	14
AF	SKTOCC#	RESERVED	RESERVED	BCLK1	BCLK0	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS
AE	VSS	DBR#	VSS	VCCIOPLL	VSS	RESERVED	VCC	VSS	VCC	VSS	VCC	VSS	VCC
AD	ITP_CLK1	TESTHI12	TESTHI0	VSS	VSSA	VSS	VCCA	VCC	VSS	VCC	VSS	VCC	VSS
AC	ITP_CLK0	VSS	TESTHI4	TESTHI5	VSS	TESTHI2	TESTHI3	VSS	VCC	VSS	VCC	VSS	VCC
AB	SLP#	RESET#	VSS	PWRGOOD	ITPCLKOUT1	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS
AA	VSS	D61#	D63#	VSS	D62#	GTLREF	ITPCLKOUT0	VSS	VCC	VSS	VCC	VSS	VCC
Y	D56#	VSS	D59#	D58#	VSS	D60#							
W	D55#	D57#	VSS	DSTBP3#	DSTBN3#	VSS							
V	VSS	D51#	D54#	VSS	D53#	DBI3#							
U	D48#	VSS	D49#	D50#	VSS	D52#							
T	D44#	D45#	VSS	D47#	D46#	VSS							
R	VSS	D42#	D43#	VSS	DSTBN2#	D40#							
P	DBI2#	VSS	D41#	DSTBP2#	VSS	D34#							
N	D38#	D39#	VSS	D36#	D33#	VSS							
M	D37#	VSS	D35#	D32#	VSS	D27#							
L	VSS	DP3#	COMP0	VSS	D28#	D24#							
K	DP2#	DP1#	VSS	D30#	DSTBN1#	VSS							
J	DP0#	VSS	D29#	DSTBP1#	VSS	D14#							
H	VSS	D31#	D26#	VSS	D16#	D11#							
G	D25#	DBI1#	VSS	D18#	D10#	VSS							
F	D22#	VSS	D20#	D19#	VSS	DSTBP0#	GTLREF	VCC	VSS	VCC	VSS	VCC	VSS
E	VSS	D21#	D17#	VSS	DSTBN0#	DBI0#	VCC	VSS	VCC	VSS	VCC	VSS	VCC
D	D23#	D15#	VSS	D13#	D5#	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS
C	D12#	VSS	D8#	D7#	VSS	D4#	VCC	VSS	VCC	VSS	VCC	VSS	VCC
B	VSS	D9#	D6#	VSS	D1#	D0#	VSS	VCC	VSS	VCC	VSS	VCC	VSS
A	VSS	D3#	VSS	D2#	RESERVED	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC
	26	25	24	23	22	21	20	19	18	17	16	15	14

Figure 29. Processor Pinout Coordinates (Top View, Right Side)

13	12	11	10	9	8	7	6	5	4	3	2	1	
VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCCVID	RESERVED	VCC	VSS	AF
VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VID0	VID1	VID2	VID3	VID4	AE
VCC	VSS	VCC	VSS	VCC	VSS	VCC	BSEL0	BSEL1	VSS	RESERVED	RESERVED	VSS	AD
VSS	VCC	VSS	VCC	VSS	VCC	VSS	BPM0#	VSS	BPM2#	IERR#	VSS	AP0#	AC
VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	BPM1#	BPM5#	VSS	RSP#	A35#	AB
VSS	VCC	VSS	VCC	VSS	VCC	VSS	GTLREF	BPM4#	VSS	BINIT#	TESTHI1	VSS	AA
							BPM3#	VSS	STPCLK#	TESTHI10	VSS	A34#	Y
							VSS	INIT#	TESTHI9	VSS	A33#	A29#	W
							MCERR#	AP1#	VSS	A32#	A27#	VSS	V
							TESTHI8	VSS	A31#	A25#	VSS	A23#	U
							VSS	A30#	A26#	VSS	A22#	A17#	T
							A28#	ADSTB1#	VSS	A21#	A18#	VSS	R
							A24#	VSS	A20#	A19#	VSS	COMP1	P
							VSS	A16#	A15#	VSS	A14#	A12#	N
							A8#	VSS	A11#	A10#	VSS	A13#	M
							A5#	ADSTB0#	VSS	A7#	A9#	VSS	L
							VSS	REQ1#	A4#	VSS	A3#	A6#	K
							TRDY#	VSS	REQ2#	REQ3#	VSS	REQ0#	J
							BR0#	DBSY#	VSS	REQ4#	DRDY#	VSS	H
							VSS	RS1#	LOCK#	VSS	BNR#	ADS#	G
VCC	VSS	VCC	VSS	VCC	VSS	TMS	GTLREF	VSS	RS2#	HIT#	VSS	RS0#	F
VSS	VCC	VSS	VCC	VSS	VCC	VSS	TRST#	LINT1	VSS	HITM#	DEFER#	VSS	E
VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	TDO	TCK	VSS	BPRI#	LINT0	D
VSS	VCC	VSS	VCC	VSS	VCC	VSS	A20M#	VSS	THERMDC	PROCHOT#	VSS	TDI	C
VCC	VSS	VCC	VSS	VCC	VSS	VCC	FERR#	SMI#	VSS	THERMDA	IGNNE#		B
VSS	VCC	VSS	VCC	VSS	VCC	RESERVED	TESTHI11	VCC_{SENSE}	VSSSENSE	VSS	THERMTRIP#		A
13	12	11	10	9	8	7	6	5	4	3	2	1	

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5.0 Pin Listing and Signal Definitions

5.1 Intel® Celeron® Processor in the 478-Pin Package Pin Assignments

Table 30 and Table 31 are pinlists for the Celeron processor in the 478-pin package. Table 30 is a listing of all processor pins ordered alphabetically by pin name. Table 31 is also a listing of all processor pins but ordered by pin number.

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
A3#	K2	Source Synch	Input/Output
A4#	K4	Source Synch	Input/Output
A5#	L6	Source Synch	Input/Output
A6#	K1	Source Synch	Input/Output
A7#	L3	Source Synch	Input/Output
A8#	M6	Source Synch	Input/Output
A9#	L2	Source Synch	Input/Output
A10#	M3	Source Synch	Input/Output
A11#	M4	Source Synch	Input/Output
A12#	N1	Source Synch	Input/Output
A13#	M1	Source Synch	Input/Output
A14#	N2	Source Synch	Input/Output
A15#	N4	Source Synch	Input/Output
A16#	N5	Source Synch	Input/Output
A17#	T1	Source Synch	Input/Output
A18#	R2	Source Synch	Input/Output
A19#	P3	Source Synch	Input/Output
A20#	P4	Source Synch	Input/Output
A21#	R3	Source Synch	Input/Output
A22#	T2	Source Synch	Input/Output
A23#	U1	Source Synch	Input/Output
A24#	P6	Source Synch	Input/Output
A25#	U3	Source Synch	Input/Output
A26#	T4	Source Synch	Input/Output
A27#	V2	Source Synch	Input/Output
A28#	R6	Source Synch	Input/Output
A29#	W1	Source Synch	Input/Output
A30#	T5	Source Synch	Input/Output
A31#	U4	Source Synch	Input/Output
A32#	V3	Source Synch	Input/Output
A33#	W2	Source Synch	Input/Output
A34#	Y1	Source Synch	Input/Output
A35#	AB1	Source Synch	Input/Output
A20M#	C6	Asynch GTL+	Input
ADS#	G1	Common Clock	Input/Output
ADSTB0#	L5	Source Synch	Input/Output
ADSTB1#	R5	Source Synch	Input/Output
AP0#	AC1	Common Clock	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
AP1#	V5	Common Clock	Input/Output
BCLK0	AF22	Bus Clock	Input
BCLK1	AF23	Bus Clock	Input
BINIT#	AA3	Common Clock	Input/Output
BNR#	G2	Common Clock	Input/Output
BPM0#	AC6	Common Clock	Input/Output
BPM1#	AB5	Common Clock	Input/Output
BPM2#	AC4	Common Clock	Input/Output
BPM3#	Y6	Common Clock	Input/Output
BPM4#	AA5	Common Clock	Input/Output
BPM5#	AB4	Common Clock	Input/Output
BPRI#	D2	Common Clock	Input
BR0#	H6	Common Clock	Input/Output
BSEL0	AD6	Power/Other	Output
BSEL1	AD5	Power/Other	Output
COMP0	L24	Power/Other	Input/Output
COMP1	P1	Power/Other	Input/Output
D0#	B21	Source Synch	Input/Output
D1#	B22	Source Synch	Input/Output
D2#	A23	Source Synch	Input/Output
D3#	A25	Source Synch	Input/Output
D4#	C21	Source Synch	Input/Output
D5#	D22	Source Synch	Input/Output
D6#	B24	Source Synch	Input/Output
D7#	C23	Source Synch	Input/Output
D8#	C24	Source Synch	Input/Output
D9#	B25	Source Synch	Input/Output
D10#	G22	Source Synch	Input/Output
D11#	H21	Source Synch	Input/Output
D12#	C26	Source Synch	Input/Output
D13#	D23	Source Synch	Input/Output
D14#	J21	Source Synch	Input/Output
D15#	D25	Source Synch	Input/Output
D16#	H22	Source Synch	Input/Output
D17#	E24	Source Synch	Input/Output
D18#	G23	Source Synch	Input/Output
D19#	F23	Source Synch	Input/Output
D20#	F24	Source Synch	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
D21#	E25	Source Synch	Input/Output
D22#	F26	Source Synch	Input/Output
D23#	D26	Source Synch	Input/Output
D24#	L21	Source Synch	Input/Output
D25#	G26	Source Synch	Input/Output
D26#	H24	Source Synch	Input/Output
D27#	M21	Source Synch	Input/Output
D28#	L22	Source Synch	Input/Output
D29#	J24	Source Synch	Input/Output
D30#	K23	Source Synch	Input/Output
D31#	H25	Source Synch	Input/Output
D32#	M23	Source Synch	Input/Output
D33#	N22	Source Synch	Input/Output
D34#	P21	Source Synch	Input/Output
D35#	M24	Source Synch	Input/Output
D36#	N23	Source Synch	Input/Output
D37#	M26	Source Synch	Input/Output
D38#	N26	Source Synch	Input/Output
D39#	N25	Source Synch	Input/Output
D40#	R21	Source Synch	Input/Output
D41#	P24	Source Synch	Input/Output
D42#	R25	Source Synch	Input/Output
D43#	R24	Source Synch	Input/Output
D44#	T26	Source Synch	Input/Output
D45#	T25	Source Synch	Input/Output
D46#	T22	Source Synch	Input/Output
D47#	T23	Source Synch	Input/Output
D48#	U26	Source Synch	Input/Output
D49#	U24	Source Synch	Input/Output
D50#	U23	Source Synch	Input/Output
D51#	V25	Source Synch	Input/Output
D52#	U21	Source Synch	Input/Output
D53#	V22	Source Synch	Input/Output
D54#	V24	Source Synch	Input/Output
D55#	W26	Source Synch	Input/Output
D56#	Y26	Source Synch	Input/Output
D57#	W25	Source Synch	Input/Output
D58#	Y23	Source Synch	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
D59#	Y24	Source Synch	Input/Output
D60#	Y21	Source Synch	Input/Output
D61#	AA25	Source Synch	Input/Output
D62#	AA22	Source Synch	Input/Output
D63#	AA24	Source Synch	Input/Output
DBI0#	E21	Source Synch	Input/Output
DBI1#	G25	Source Synch	Input/Output
DBI2#	P26	Source Synch	Input/Output
DBI3#	V21	Source Synch	Input/Output
DBR#	AE25	Power/Other	Output
DBSY#	H5	Common Clock	Input/Output
DEFER#	E2	Common Clock	Input
DP0#	J26	Common Clock	Input/Output
DP1#	K25	Common Clock	Input/Output
DP2#	K26	Common Clock	Input/Output
DP3#	L25	Common Clock	Input/Output
DRDY#	H2	Common Clock	Input/Output
DSTBN0#	E22	Source Synch	Input/Output
DSTBN1#	K22	Source Synch	Input/Output
DSTBN2#	R22	Source Synch	Input/Output
DSTBN3#	W22	Source Synch	Input/Output
DSTBP0#	F21	Source Synch	Input/Output
DSTBP1#	J23	Source Synch	Input/Output
DSTBP2#	P23	Source Synch	Input/Output
DSTBP3#	W23	Source Synch	Input/Output
FERR#	B6	Asynch AGL+	Output
GTLREF	AA21	Power/Other	Input
GTLREF	AA6	Power/Other	Input
GTLREF	F20	Power/Other	Input
GTLREF	F6	Power/Other	Input
HIT#	F3	Common Clock	Input/Output
HITM#	E3	Common Clock	Input/Output
IERR#	AC3	Common Clock	Output
IGNNE#	B2	Asynch GTL+	Input
INIT#	W5	Asynch GTL+	Input
ITPCLKOUT0	AA20	Power/Other	Output
ITPCLKOUT1	AB22	Power/Other	Output
ITP_CLK0	AC26	TAP	input

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
ITP_CLK1	AD26	TAP	input
LINT0	D1	Asynch GTL+	Input
LINT1	E5	Asynch GTL+	Input
LOCK#	G4	Common Clock	Input/Output
MCERR#	V6	Common Clock	Input/Output
PROCHOT#	C3	Asynch GTL+	Output
PWRGOOD	AB23	Power/Other	Input
REQ0#	J1	Source Synch	Input/Output
REQ1#	K5	Source Synch	Input/Output
REQ2#	J4	Source Synch	Input/Output
REQ3#	J3	Source Synch	Input/Output
REQ4#	H3	Source Synch	Input/Output
RESERVED	A22		
RESERVED	A7		
RESERVED	AD2		
RESERVED	AD3		
RESERVED	AE21		
RESERVED	AF3		
RESERVED	AF24		
RESERVED	AF25		
RESET#	AB25	Common Clock	Input
RS0#	F1	Common Clock	Input
RS1#	G5	Common Clock	Input
RS2#	F4	Common Clock	Input
RSP#	AB2	Common Clock	Input
SKTOCC#	AF26	Power/Other	Output
SLP#	AB26	Asynch GTL+	Input
SMI#	B5	Asynch GTL+	Input
STPCLK#	Y4	Asynch GTL+	Input
TCK	D4	TAP	Input
TDI	C1	TAP	Input
TDO	D5	TAP	Output
TESTHI0	AD24	Power/Other	Input
TESTHI1	AA2	Power/Other	Input
TESTHI2	AC21	Power/Other	Input
TESTHI3	AC20	Power/Other	Input
TESTHI4	AC24	Power/Other	Input
TESTHI5	AC23	Power/Other	Input

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
TESTHI8	U6	Power/Other	Input
TESTHI9	W4	Power/Other	Input
TESTHI10	Y3	Power/Other	Input
TESTHI11	A6	Power/Other	Input
TESTHI12	AD25	Power/Other	Input
THERMDA	B3	Power/Other	
THERMDC	C4	Power/Other	
THERMTRIP#	A2	Asynch GTL+	Output
TMS	F7	TAP	Input
TRDY#	J6	Common Clock	Input
TRST#	E6	TAP	Input
Vcc	A10	Power/Other	
Vcc	A12	Power/Other	
Vcc	A14	Power/Other	
Vcc	A16	Power/Other	
Vcc	A18	Power/Other	
Vcc	A20	Power/Other	
Vcc	A8	Power/Other	
Vcc	AA10	Power/Other	
Vcc	AA12	Power/Other	
Vcc	AA14	Power/Other	
Vcc	AA16	Power/Other	
Vcc	AA18	Power/Other	
Vcc	AA8	Power/Other	
Vcc	AB11	Power/Other	
Vcc	AB13	Power/Other	
Vcc	AB15	Power/Other	
Vcc	AB17	Power/Other	
Vcc	AB19	Power/Other	
Vcc	AB7	Power/Other	
Vcc	AB9	Power/Other	
Vcc	AC10	Power/Other	
Vcc	AC12	Power/Other	
Vcc	AC14	Power/Other	
Vcc	AC16	Power/Other	
Vcc	AC18	Power/Other	
Vcc	AC8	Power/Other	
Vcc	AD11	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AD13	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD19	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE16	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AE6	Power/Other	
VCC	AE8	Power/Other	
VCC	AF11	Power/Other	
VCC	AF13	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF19	Power/Other	
VCC	AF2	Power/Other	
VCC	AF21	Power/Other	
VCC	AF5	Power/Other	
VCC	AF7	Power/Other	
VCC	AF9	Power/Other	
VCC	B11	Power/Other	
VCC	B13	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B19	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C14	Power/Other	
VCC	C16	Power/Other	
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AD20	Power/Other	
VCCIOPLL	AE23	Power/Other	
VCC_{SENSE}	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VID0	AE5	Power/Other	Output
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VSS	D10	Power/Other	
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
Vss	A3	Power/Other	
Vss	A9	Power/Other	
Vss	AA1	Power/Other	
Vss	AA11	Power/Other	
Vss	AA13	Power/Other	
Vss	AA15	Power/Other	
Vss	AA17	Power/Other	
Vss	AA19	Power/Other	
Vss	AA23	Power/Other	
Vss	AA26	Power/Other	
Vss	AA4	Power/Other	
Vss	AA7	Power/Other	
Vss	AA9	Power/Other	
Vss	AB10	Power/Other	
Vss	AB12	Power/Other	
Vss	AB14	Power/Other	
Vss	AB16	Power/Other	
Vss	AB18	Power/Other	
Vss	AB20	Power/Other	
Vss	AB21	Power/Other	
Vss	AB24	Power/Other	
Vss	AB3	Power/Other	
Vss	AB6	Power/Other	
Vss	AB8	Power/Other	
Vss	AC11	Power/Other	
Vss	AC13	Power/Other	
Vss	AC15	Power/Other	
Vss	AC17	Power/Other	
Vss	AC19	Power/Other	
Vss	AC2	Power/Other	
Vss	AC22	Power/Other	
Vss	AC25	Power/Other	
Vss	AC5	Power/Other	
Vss	AC7	Power/Other	
Vss	AC9	Power/Other	
Vss	AD1	Power/Other	
Vss	AD10	Power/Other	
Vss	AD12	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
Vss	AD14	Power/Other	
Vss	AD16	Power/Other	
Vss	AD18	Power/Other	
Vss	AD21	Power/Other	
Vss	AD23	Power/Other	
Vss	AD4	Power/Other	
Vss	AD8	Power/Other	
Vss	AE11	Power/Other	
Vss	AE13	Power/Other	
Vss	AE15	Power/Other	
Vss	AE17	Power/Other	
Vss	AE19	Power/Other	
Vss	AE22	Power/Other	
Vss	AE24	Power/Other	
Vss	AE26	Power/Other	
Vss	AE7	Power/Other	
Vss	AE9	Power/Other	
Vss	AF1	Power/Other	
Vss	AF10	Power/Other	
Vss	AF12	Power/Other	
Vss	AF14	Power/Other	
Vss	AF16	Power/Other	
Vss	AF18	Power/Other	
Vss	AF20	Power/Other	
Vss	AF6	Power/Other	
Vss	AF8	Power/Other	
Vss	B10	Power/Other	
Vss	B12	Power/Other	
Vss	B14	Power/Other	
Vss	B16	Power/Other	
Vss	B18	Power/Other	
Vss	B20	Power/Other	
Vss	B23	Power/Other	
Vss	B26	Power/Other	
Vss	B4	Power/Other	
Vss	B8	Power/Other	
Vss	C11	Power/Other	
Vss	C13	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
Vss	C15	Power/Other	
Vss	C17	Power/Other	
Vss	C19	Power/Other	
Vss	C2	Power/Other	
Vss	C22	Power/Other	
Vss	C25	Power/Other	
Vss	C5	Power/Other	
Vss	C7	Power/Other	
Vss	C9	Power/Other	
Vss	D12	Power/Other	
Vss	D14	Power/Other	
Vss	D16	Power/Other	
Vss	D18	Power/Other	
Vss	D20	Power/Other	
Vss	D21	Power/Other	
Vss	D24	Power/Other	
Vss	D3	Power/Other	
Vss	D6	Power/Other	
Vss	D8	Power/Other	
Vss	E1	Power/Other	
Vss	E11	Power/Other	
Vss	E13	Power/Other	
Vss	E15	Power/Other	
Vss	E17	Power/Other	
Vss	E19	Power/Other	
Vss	E23	Power/Other	
Vss	E26	Power/Other	
Vss	E4	Power/Other	
Vss	E7	Power/Other	
Vss	E9	Power/Other	
Vss	F10	Power/Other	
Vss	F12	Power/Other	
Vss	F14	Power/Other	
Vss	F16	Power/Other	
Vss	F18	Power/Other	
Vss	F2	Power/Other	
Vss	F22	Power/Other	
Vss	F25	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
Vss	F5	Power/Other	
Vss	F8	Power/Other	
Vss	G21	Power/Other	
Vss	G24	Power/Other	
Vss	G3	Power/Other	
Vss	G6	Power/Other	
Vss	H1	Power/Other	
Vss	H23	Power/Other	
Vss	H26	Power/Other	
Vss	H4	Power/Other	
Vss	J2	Power/Other	
Vss	J22	Power/Other	
Vss	J25	Power/Other	
Vss	J5	Power/Other	
Vss	K21	Power/Other	
Vss	K24	Power/Other	
Vss	K3	Power/Other	
Vss	K6	Power/Other	
Vss	L1	Power/Other	
Vss	L23	Power/Other	
Vss	L26	Power/Other	
Vss	L4	Power/Other	
Vss	M2	Power/Other	
Vss	M22	Power/Other	
Vss	M25	Power/Other	
Vss	M5	Power/Other	
Vss	N21	Power/Other	
Vss	N24	Power/Other	
Vss	N3	Power/Other	
Vss	N6	Power/Other	
Vss	P2	Power/Other	
Vss	P22	Power/Other	
Vss	P25	Power/Other	
Vss	P5	Power/Other	
Vss	R1	Power/Other	
Vss	R23	Power/Other	
Vss	R26	Power/Other	
Vss	R4	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	T21	Power/Other	
VSS	T24	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	U2	Power/Other	
VSS	U22	Power/Other	
VSS	U25	Power/Other	
VSS	U5	Power/Other	
VSS	V1	Power/Other	
VSS	V23	Power/Other	
VSS	V26	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	V4	Power/Other	
VSS	W21	Power/Other	
VSS	W24	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	Y2	Power/Other	
VSS	Y22	Power/Other	
VSS	Y25	Power/Other	
VSS	Y5	Power/Other	
VSSA	AD22	Power/Other	
VSSSENSE	A4	Power/Other	Output

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
A2	THERMTRIP#	Asynch GTL+	Output
A3	Vss	Power/Other	
A4	VSSSENSE	Power/Other	Output
A5	VCC_{SENSE}	Power/Other	Output
A6	TESTHI11	Power/Other	Input
A7	RESERVED		
A8	Vcc	Power/Other	
A9	Vss	Power/Other	
A10	Vcc	Power/Other	
A11	Vss	Power/Other	
A12	Vcc	Power/Other	
A13	Vss	Power/Other	
A14	Vcc	Power/Other	
A15	Vss	Power/Other	
A16	Vcc	Power/Other	
A17	Vss	Power/Other	
A18	Vcc	Power/Other	
A19	Vss	Power/Other	
A20	Vcc	Power/Other	
A21	Vss	Power/Other	
A22	RESERVED		
A23	D2#	Source Synch	Input/Output
A24	Vss	Power/Other	
A25	D3#	Source Synch	Input/Output
A26	Vss	Power/Other	
AA1	Vss	Power/Other	
AA2	TESTHI1	Power/Other	Input
AA3	BINIT#	Common Clock	Input/Output
AA4	Vss	Power/Other	
AA5	BPM4#	Common Clock	Input/Output
AA6	GTLREF	Power/Other	Input
AA7	Vss	Power/Other	
AA8	Vcc	Power/Other	
AA9	Vss	Power/Other	
AA10	Vcc	Power/Other	
AA11	Vss	Power/Other	
AA12	Vcc	Power/Other	
AA13	Vss	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AA14	Vcc	Power/Other	
AA15	Vss	Power/Other	
AA16	Vcc	Power/Other	
AA17	Vss	Power/Other	
AA18	Vcc	Power/Other	
AA19	Vss	Power/Other	
AA20	ITPCLKOUT0	Power/Other	Output
AA21	GTLREF	Power/Other	Input
AA22	D62#	Source Synch	Input/Output
AA23	Vss	Power/Other	
AA24	D63#	Source Synch	Input/Output
AA25	D61#	Source Synch	Input/Output
AA26	Vss	Power/Other	
AB1	A35#	Source Synch	Input/Output
AB2	RSP#	Common Clock	Input
AB3	Vss	Power/Other	
AB4	BPM5#	Common Clock	Input/Output
AB5	BPM1#	Common Clock	Input/Output
AB6	Vss	Power/Other	
AB7	Vcc	Power/Other	
AB8	Vss	Power/Other	
AB9	Vcc	Power/Other	
AB10	Vss	Power/Other	
AB11	Vcc	Power/Other	
AB12	Vss	Power/Other	
AB13	Vcc	Power/Other	
AB14	Vss	Power/Other	
AB15	Vcc	Power/Other	
AB16	Vss	Power/Other	
AB17	Vcc	Power/Other	
AB18	Vss	Power/Other	
AB19	Vcc	Power/Other	
AB20	Vss	Power/Other	
AB21	Vss	Power/Other	
AB22	ITPCLKOUT1	Power/Other	Output
AB23	PWRGOOD	Power/Other	Input
AB24	Vss	Power/Other	
AB25	RESET#	Common Clock	Input

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AB26	SLP#	Asynch GTL+	Input
AC1	AP0#	Common Clock	Input/Output
AC2	VSS	Power/Other	
AC3	IERR#	Common Clock	Output
AC4	BPM2#	Common Clock	Input/Output
AC5	VSS	Power/Other	
AC6	BPM0#	Common Clock	Input/Output
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC9	VSS	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VSS	Power/Other	
AC14	VCC	Power/Other	
AC15	VSS	Power/Other	
AC16	VCC	Power/Other	
AC17	VSS	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	TESTHI3	Power/Other	Input
AC21	TESTHI2	Power/Other	Input
AC22	VSS	Power/Other	
AC23	TESTHI5	Power/Other	Input
AC24	TESTHI4	Power/Other	Input
AC25	VSS	Power/Other	
AC26	ITP_CLK0	TAP	input
AD1	VSS	Power/Other	
AD2	RESERVED		
AD3	RESERVED		
AD4	VSS	Power/Other	
AD5	BSEL1	Power/Other	Output
AD6	BSEL0	Power/Other	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VSS	Power/Other	
AD11	VCC	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AD12	VSS	Power/Other	
AD13	VCC	Power/Other	
AD14	VSS	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VSS	Power/Other	
AD19	VCC	Power/Other	
AD20	VCCA	Power/Other	
AD21	VSS	Power/Other	
AD22	VSSA	Power/Other	
AD23	VSS	Power/Other	
AD24	TESTHI0	Power/Other	Input
AD25	TESTHI12	Power/Other	Input
AD26	ITP_CLK1	TAP	input
AE1	VID4	Power/Other	Output
AE2	VID3	Power/Other	Output
AE3	VID2	Power/Other	Output
AE4	VID1	Power/Other	Output
AE5	VID0	Power/Other	Output
AE6	VCC	Power/Other	
AE7	VSS	Power/Other	
AE8	VCC	Power/Other	
AE9	VSS	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VSS	Power/Other	
AE16	VCC	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	RESERVED		
AE22	VSS	Power/Other	
AE23	VCCIOPLL	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AE24	Vss	Power/Other	
AE25	DBR#	Power/Other	Output
AE26	Vss	Power/Other	
AF1	Vss	Power/Other	
AF2	Vcc	Power/Other	
AF3	RESERVED		
AF4	VCCVID	Power/Other	Input
AF5	Vcc	Power/Other	
AF6	Vss	Power/Other	
AF7	Vcc	Power/Other	
AF8	Vss	Power/Other	
AF9	Vcc	Power/Other	
AF10	Vss	Power/Other	
AF11	Vcc	Power/Other	
AF12	Vss	Power/Other	
AF13	Vcc	Power/Other	
AF14	Vss	Power/Other	
AF15	Vcc	Power/Other	
AF16	Vss	Power/Other	
AF17	Vcc	Power/Other	
AF18	Vss	Power/Other	
AF19	Vcc	Power/Other	
AF20	Vss	Power/Other	
AF21	Vcc	Power/Other	
AF22	BCLK0	Bus Clock	Input
AF23	BCLK1	Bus Clock	Input
AF24	RESERVED		
AF25	RESERVED		
AF26	SKTOCC#	Power/Other	Output
B2	IGNNE#	Asynch GTL+	Input
B3	THERMDA	Power/Other	
B4	Vss	Power/Other	
B5	SMI#	Asynch GTL+	Input
B6	FERR#	Asynch AGL+	Output
B7	Vcc	Power/Other	
B8	Vss	Power/Other	
B9	Vcc	Power/Other	
B10	Vss	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
B11	Vcc	Power/Other	
B12	Vss	Power/Other	
B13	Vcc	Power/Other	
B14	Vss	Power/Other	
B15	Vcc	Power/Other	
B16	Vss	Power/Other	
B17	Vcc	Power/Other	
B18	Vss	Power/Other	
B19	Vcc	Power/Other	
B20	Vss	Power/Other	
B21	D0#	Source Synch	Input/Output
B22	D1#	Source Synch	Input/Output
B23	Vss	Power/Other	
B24	D6#	Source Synch	Input/Output
B25	D9#	Source Synch	Input/Output
B26	Vss	Power/Other	
C1	TDI	TAP	Input
C2	Vss	Power/Other	
C3	PROCHOT#	Asynch GTL+	Output
C4	THERMDC	Power/Other	
C5	Vss	Power/Other	
C6	A20M#	Asynch GTL+	Input
C7	Vss	Power/Other	
C8	Vcc	Power/Other	
C9	Vss	Power/Other	
C10	Vcc	Power/Other	
C11	Vss	Power/Other	
C12	Vcc	Power/Other	
C13	Vss	Power/Other	
C14	Vcc	Power/Other	
C15	Vss	Power/Other	
C16	Vcc	Power/Other	
C17	Vss	Power/Other	
C18	Vcc	Power/Other	
C19	Vss	Power/Other	
C20	Vcc	Power/Other	
C21	D4#	Source Synch	Input/Output
C22	Vss	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
C23	D7#	Source Synch	Input/Output
C24	D8#	Source Synch	Input/Output
C25	Vss	Power/Other	
C26	D12#	Source Synch	Input/Output
D1	LINT0	Asynch GTL+	Input
D2	BPRI#	Common Clock	Input
D3	Vss	Power/Other	
D4	TCK	TAP	Input
D5	TDO	TAP	Output
D6	Vss	Power/Other	
D7	Vcc	Power/Other	
D8	Vss	Power/Other	
D9	Vcc	Power/Other	
D10	Vss	Power/Other	
D11	Vcc	Power/Other	
D12	Vss	Power/Other	
D13	Vcc	Power/Other	
D14	Vss	Power/Other	
D15	Vcc	Power/Other	
D16	Vss	Power/Other	
D17	Vcc	Power/Other	
D18	Vss	Power/Other	
D19	Vcc	Power/Other	
D20	Vss	Power/Other	
D21	Vss	Power/Other	
D22	D5#	Source Synch	Input/Output
D23	D13#	Source Synch	Input/Output
D24	Vss	Power/Other	
D25	D15#	Source Synch	Input/Output
D26	D23#	Source Synch	Input/Output
E1	Vss	Power/Other	
E2	DEFER#	Common Clock	Input
E3	HITM#	Common Clock	Input/Output
E4	Vss	Power/Other	
E5	LINT1	Asynch GTL+	Input
E6	TRST#	TAP	Input
E7	Vss	Power/Other	
E8	Vcc	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
E9	Vss	Power/Other	
E10	Vcc	Power/Other	
E11	Vss	Power/Other	
E12	Vcc	Power/Other	
E13	Vss	Power/Other	
E14	Vcc	Power/Other	
E15	Vss	Power/Other	
E16	Vcc	Power/Other	
E17	Vss	Power/Other	
E18	Vcc	Power/Other	
E19	Vss	Power/Other	
E20	Vcc	Power/Other	
E21	DBI0#	Source Synch	Input/Output
E22	DSTBN0#	Source Synch	Input/Output
E23	Vss	Power/Other	
E24	D17#	Source Synch	Input/Output
E25	D21#	Source Synch	Input/Output
E26	Vss	Power/Other	
F1	RS0#	Common Clock	Input
F2	Vss	Power/Other	
F3	HIT#	Common Clock	Input/Output
F4	RS2#	Common Clock	Input
F5	Vss	Power/Other	
F6	GTLREF	Power/Other	Input
F7	TMS	TAP	Input
F8	Vss	Power/Other	
F9	Vcc	Power/Other	
F10	Vss	Power/Other	
F11	Vcc	Power/Other	
F12	Vss	Power/Other	
F13	Vcc	Power/Other	
F14	Vss	Power/Other	
F15	Vcc	Power/Other	
F16	Vss	Power/Other	
F17	Vcc	Power/Other	
F18	Vss	Power/Other	
F19	Vcc	Power/Other	
F20	GTLREF	Power/Other	Input

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
F21	DSTBP0#	Source Synch	Input/Output
F22	Vss	Power/Other	
F23	D19#	Source Synch	Input/Output
F24	D20#	Source Synch	Input/Output
F25	Vss	Power/Other	
F26	D22#	Source Synch	Input/Output
G1	ADS#	Common Clock	Input/Output
G2	BNR#	Common Clock	Input/Output
G3	Vss	Power/Other	
G4	LOCK#	Common Clock	Input/Output
G5	RS1#	Common Clock	Input
G6	Vss	Power/Other	
G21	Vss	Power/Other	
G22	D10#	Source Synch	Input/Output
G23	D18#	Source Synch	Input/Output
G24	Vss	Power/Other	
G25	DBI1#	Source Synch	Input/Output
G26	D25#	Source Synch	Input/Output
H1	Vss	Power/Other	
H2	DRDY#	Common Clock	Input/Output
H3	REQ4#	Source Synch	Input/Output
H4	Vss	Power/Other	
H5	DBSY#	Common Clock	Input/Output
H6	BR0#	Common Clock	Input/Output
H21	D11#	Source Synch	Input/Output
H22	D16#	Source Synch	Input/Output
H23	Vss	Power/Other	
H24	D26#	Source Synch	Input/Output
H25	D31#	Source Synch	Input/Output
H26	Vss	Power/Other	
J1	REQ0#	Source Synch	Input/Output
J2	Vss	Power/Other	
J3	REQ3#	Source Synch	Input/Output
J4	REQ2#	Source Synch	Input/Output
J5	Vss	Power/Other	
J6	TRDY#	Common Clock	Input
J21	D14#	Source Synch	Input/Output
J22	Vss	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
J23	DSTBP1#	Source Synch	Input/Output
J24	D29#	Source Synch	Input/Output
J25	Vss	Power/Other	
J26	DP0#	Common Clock	Input/Output
K1	A6#	Source Synch	Input/Output
K2	A3#	Source Synch	Input/Output
K3	Vss	Power/Other	
K4	A4#	Source Synch	Input/Output
K5	REQ1#	Source Synch	Input/Output
K6	Vss	Power/Other	
K21	Vss	Power/Other	
K22	DSTBN1#	Source Synch	Input/Output
K23	D30#	Source Synch	Input/Output
K24	Vss	Power/Other	
K25	DP1#	Common Clock	Input/Output
K26	DP2#	Common Clock	Input/Output
L1	Vss	Power/Other	
L2	A9#	Source Synch	Input/Output
L3	A7#	Source Synch	Input/Output
L4	Vss	Power/Other	
L5	ADSTB0#	Source Synch	Input/Output
L6	A5#	Source Synch	Input/Output
L21	D24#	Source Synch	Input/Output
L22	D28#	Source Synch	Input/Output
L23	Vss	Power/Other	
L24	COMP0	Power/Other	Input/Output
L25	DP3#	Common Clock	Input/Output
L26	Vss	Power/Other	
M1	A13#	Source Synch	Input/Output
M2	Vss	Power/Other	
M3	A10#	Source Synch	Input/Output
M4	A11#	Source Synch	Input/Output
M5	Vss	Power/Other	
M6	A8#	Source Synch	Input/Output
M21	D27#	Source Synch	Input/Output
M22	Vss	Power/Other	
M23	D32#	Source Synch	Input/Output
M24	D35#	Source Synch	Input/Output

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
M25	Vss	Power/Other	
M26	D37#	Source Synch	Input/Output
N1	A12#	Source Synch	Input/Output
N2	A14#	Source Synch	Input/Output
N3	Vss	Power/Other	
N4	A15#	Source Synch	Input/Output
N5	A16#	Source Synch	Input/Output
N6	Vss	Power/Other	
N21	Vss	Power/Other	
N22	D33#	Source Synch	Input/Output
N23	D36#	Source Synch	Input/Output
N24	Vss	Power/Other	
N25	D39#	Source Synch	Input/Output
N26	D38#	Source Synch	Input/Output
P1	COMP1	Power/Other	Input/Output
P2	Vss	Power/Other	
P3	A19#	Source Synch	Input/Output
P4	A20#	Source Synch	Input/Output
P5	Vss	Power/Other	
P6	A24#	Source Synch	Input/Output
P21	D34#	Source Synch	Input/Output
P22	Vss	Power/Other	
P23	DSTBP2#	Source Synch	Input/Output
P24	D41#	Source Synch	Input/Output
P25	Vss	Power/Other	
P26	DBI2#	Source Synch	Input/Output
R1	Vss	Power/Other	
R2	A18#	Source Synch	Input/Output
R3	A21#	Source Synch	Input/Output
R4	Vss	Power/Other	
R5	ADSTB1#	Source Synch	Input/Output
R6	A28#	Source Synch	Input/Output
R21	D40#	Source Synch	Input/Output
R22	DSTBN2#	Source Synch	Input/Output
R23	Vss	Power/Other	
R24	D43#	Source Synch	Input/Output
R25	D42#	Source Synch	Input/Output
R26	Vss	Power/Other	

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
T1	A17#	Source Synch	Input/Output
T2	A22#	Source Synch	Input/Output
T3	Vss	Power/Other	
T4	A26#	Source Synch	Input/Output
T5	A30#	Source Synch	Input/Output
T6	Vss	Power/Other	
T21	Vss	Power/Other	
T22	D46#	Source Synch	Input/Output
T23	D47#	Source Synch	Input/Output
T24	Vss	Power/Other	
T25	D45#	Source Synch	Input/Output
T26	D44#	Source Synch	Input/Output
U1	A23#	Source Synch	Input/Output
U2	Vss	Power/Other	
U3	A25#	Source Synch	Input/Output
U4	A31#	Source Synch	Input/Output
U5	Vss	Power/Other	
U6	TESTHI8	Power/Other	Input
U21	D52#	Source Synch	Input/Output
U22	Vss	Power/Other	
U23	D50#	Source Synch	Input/Output
U24	D49#	Source Synch	Input/Output
U25	Vss	Power/Other	
U26	D48#	Source Synch	Input/Output
V1	Vss	Power/Other	
V2	A27#	Source Synch	Input/Output
V3	A32#	Source Synch	Input/Output
V4	Vss	Power/Other	
V5	AP1#	Common Clock	Input/Output
V6	MCERR#	Common Clock	Input/Output
V21	DBI3#	Source Synch	Input/Output
V22	D53#	Source Synch	Input/Output
V23	Vss	Power/Other	
V24	D54#	Source Synch	Input/Output
V25	D51#	Source Synch	Input/Output
V26	Vss	Power/Other	
W1	A29#	Source Synch	Input/Output
W2	A33#	Source Synch	Input/Output

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
W3	Vss	Power/Other	
W4	TESTHI9	Power/Other	Input
W5	INIT#	Asynch GTL+	Input
W6	Vss	Power/Other	
W21	Vss	Power/Other	
W22	DSTBN3#	Source Synch	Input/Output
W23	DSTBP3#	Source Synch	Input/Output
W24	Vss	Power/Other	
W25	D57#	Source Synch	Input/Output
W26	D55#	Source Synch	Input/Output
Y1	A34#	Source Synch	Input/Output

Table 31. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
Y2	Vss	Power/Other	
Y3	TESTHI10	Power/Other	Input
Y4	STPCLK#	Asynch GTL+	Input
Y5	Vss	Power/Other	
Y6	BPM3#	Common Clock	Input/Output
Y21	D60#	Source Synch	Input/Output
Y22	Vss	Power/Other	
Y23	D58#	Source Synch	Input/Output
Y24	D59#	Source Synch	Input/Output
Y25	Vss	Power/Other	
Y26	D56#	Source Synch	Input/Output

5.2 Signal Descriptions

Table 32. Signal Description (Sheet 1 of 7)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Celeron processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 7.1 for more details.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as follows: **Signal** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB0# A[35:17]# — ADSTB1#
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Celeron processor in the 478-pin package system bus agents. The following defines the coverage model of these signals: **Request Signal** — **Subphase** — **Subphase 2** A[35:24]# — AP0# — AP1# A[23:3]# — AP1# — AP0# REQ[4:0]# — AP1# — AP0#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.

Table 32. Signal Description (Sheet 2 of 7)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Celeron processor in the 478-pin package system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Refer to Table 1 for the appropriate Platform Design Guide, and the *ITP700 Debug Port Design Guide* for more detailed information. These signals do not have on-die termination. Refer to Section 2.4, and the appropriate Platform Design Guide for termination requirements.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. This signal does not have on-die termination and must be terminated.
BSEL[1:0]	Output	The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Celeron processor in the 478-pin package operates currently at a 400 MHz system bus frequency (100 MHz BCLK[1:0] frequency). For more information about these pins, including termination recommendations refer to Section 2.8 and the appropriate Platform Design Guide.
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the appropriate Platform Design Guide for details on implementation.

Table 32. Signal Description (Sheet 3 of 7)

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following are the groupings of the quad-pumped data signals, and their associated data strobes and DBI#: **Data Group / DSTBN# / DSTBP# / DBI#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. The following are the DBI[3:0] assignments to the data bus: **Bus Signal / Data Bus Signals** DBI3# — D[63:48]# DBI2# — D[47:32]# DBI1# — D[31:16]# DBI0# — D[15:0]#
DBR#	Output	DBR# is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.
DP[3:0]#	Input/ Output	DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Celeron processor in the 478-pin package system bus agents.
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.
DSTBN[3:0]#	Input/ Output	The following are the DSTBN data strobes that are used to latch D[63:0]#: **Signals / Associated Strobe** D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#

Table 32. Signal Description (Sheet 4 of 7)

Name	Type	Description
DSTBP[3:0]#	Input/ Output	The following are the DSTBP data strobes that are used to latch D[63:0]#: **Signals** — **Associated Strobe** D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#	Output	FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 VCC. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the appropriate Platform Design Guide for more information.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. IERR# is de-asserted on assertion of RESET# only and not other signals. This signals does not have on-die termination. Refer to Section 2.4 for termination requirements.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	The ITPCLKOUT[1:0] pins do not provide any output for the Celeron processor in the 478-pin package. The function of these pins for the Pentium® 4 processor with 512 KB L2 Cache on 0.13 micron process can be found in the *Intel® Pentium® 4 Processor with 512 KB L2 Cache on 0.13 Micron Process Datasheet*. Refer to Section 2.4 for additional details and termination requirements.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

Table 32. Signal Description (Sheet 5 of 7)

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Section 7.3 for more details.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 12 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 16, and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.

Table 32. Signal Description (Sheet 6 of 7)

Name	Type	Description
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. This signal does not have on-die termination and must be terminated on the system board.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET#, the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.

Table 32. Signal Description (Sheet 7 of 7)

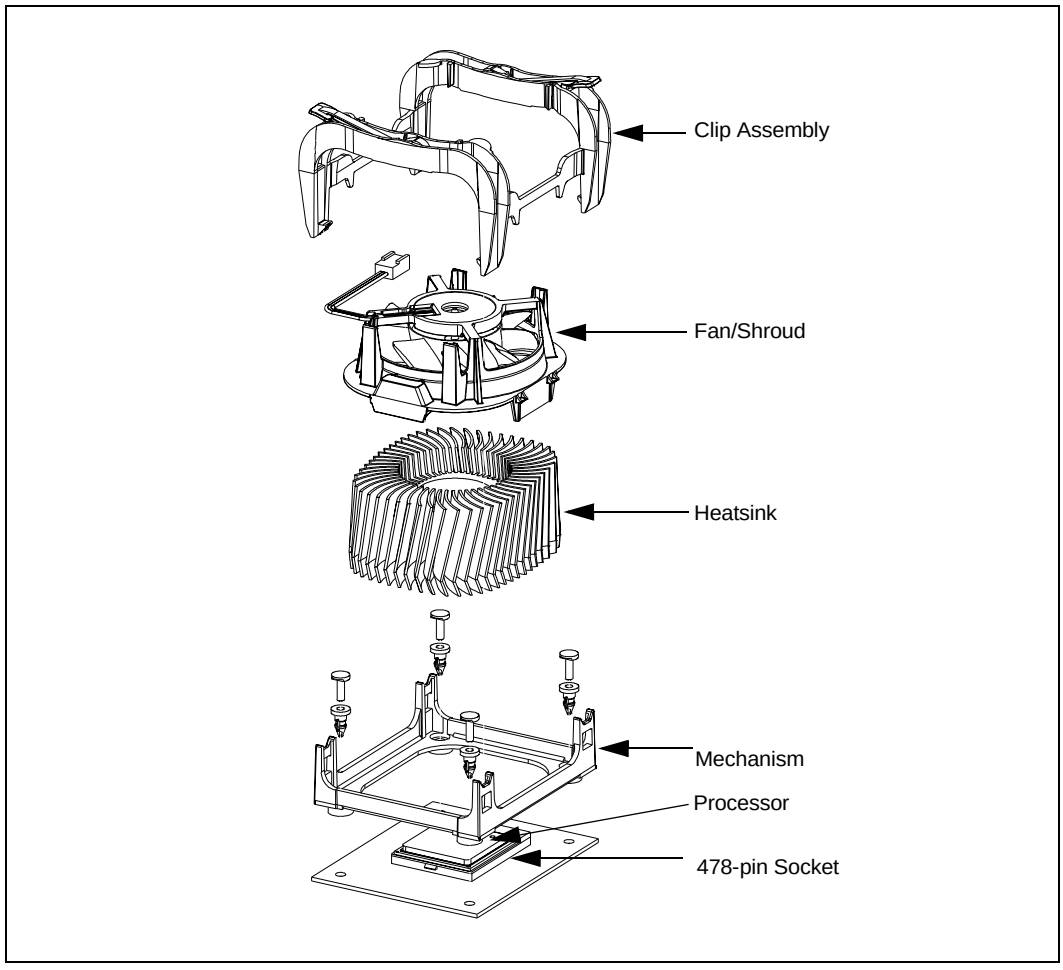
Name	Type	Description
TESTHI[12:8] TESTHI[5:0]	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation. See Section 2.4 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 7.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 7.3.1.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. See Figure 13 and Table 16 for the appropriate power down sequence and timing requirements. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 Ω pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the appropriate Platform Design Guide for complete implementation details.
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor system bus PLLs. Follow the guidelines for VCCA, and refer to the appropriate Platform Design Guide for complete implementation details.
VCC_{SENSE}	Output	VCC_{SENSE} is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	1.2 V are required to be supplied to the VCCVID pin if the platform is going to support the Pentium® processor with 512 KB L2 cache on .13 micron process. This requirement is to enable the platform to be upgradeable to the Pentium® processor with 512 KB L2 cache on 0.13 micron process and is not necessary if the platform will only support the Celeron processor in the 478-pin package. Refer to the *Pentium® 4 Processor with 512 KB L2 Cache on 0.13 Micron Process Datasheet* and the appropriate Platform Design Guide for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (VCC). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise

6.0 Thermal Specifications and Design Considerations

The Celeron processor in the 478-pin package uses an integrated heat spreader (IHS) for heatsink attachment that is intended to provide for multiple types of thermal solutions. This section provides data necessary for development of a thermal solution. See Figure 30 for an exploded view of an example thermal solution for the Celeron processor in the 478-pin package. This is for illustration purposes. For further thermal solution design details, refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

Note: The processor is either shipped by itself or with a heatsink for boxed processors. See Chapter 8.0 for details on boxed processors.

Figure 30. Example Thermal Solution for the Intel® Celeron Processor in the 478-Pin Package



NOTE: This figure is not to scale.

6.1 Thermal Specifications

Table 33 specifies the thermal design power dissipation envelope for the Celeron processor in the 478-pin package. Analysis indicates that real applications are unlikely to cause the processor to consume the maximum possible power consumption. Intel recommends that system thermal designs target the "Thermal Design Power" indicated in Table 33 instead of "Max Processor Power." The Thermal Monitor feature (refer to Section 7.3) is designed to help protect the processor from overheating while executing high power code that exceeds the recommendations in this table. To ensure maximum flexibility, systems should be designed to the Flexible Motherboard guidelines, even if a processor with a lower thermal dissipation is planned. **In all cases the Thermal Monitor feature must be enabled for the processor to be in specification.** Table 33 also lists the maximum and minimum processor temperature specifications for T_C. A thermal solution must be designed to ensure the temperature of the processor does not exceed these specifications.

Table 33. Intel® Celeron® Processor in the 478-Pin Package Thermal Design Power

Processor and Core Frequency (GHz)	Thermal Design Power[2] (W)	Minimum T_C (°C)	Maximum T_C (°C)	Notes[1]
1.70 GHz	63.5	5	76	

NOTES:
1. These values are specified at V_{CC_MAX} for the processor. The processor should not be subjected to any static Vcc and Icc combination wherein Vcc exceeds V_{CC_MAX} for a given current.
2. The numbers in this column reflect Intel's recommended design point and are not indicative of the maximum power the processor can dissipate under worst conditions. For more details refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

6.2 Thermal Analysis

6.2.1 Thermal Solution Performance

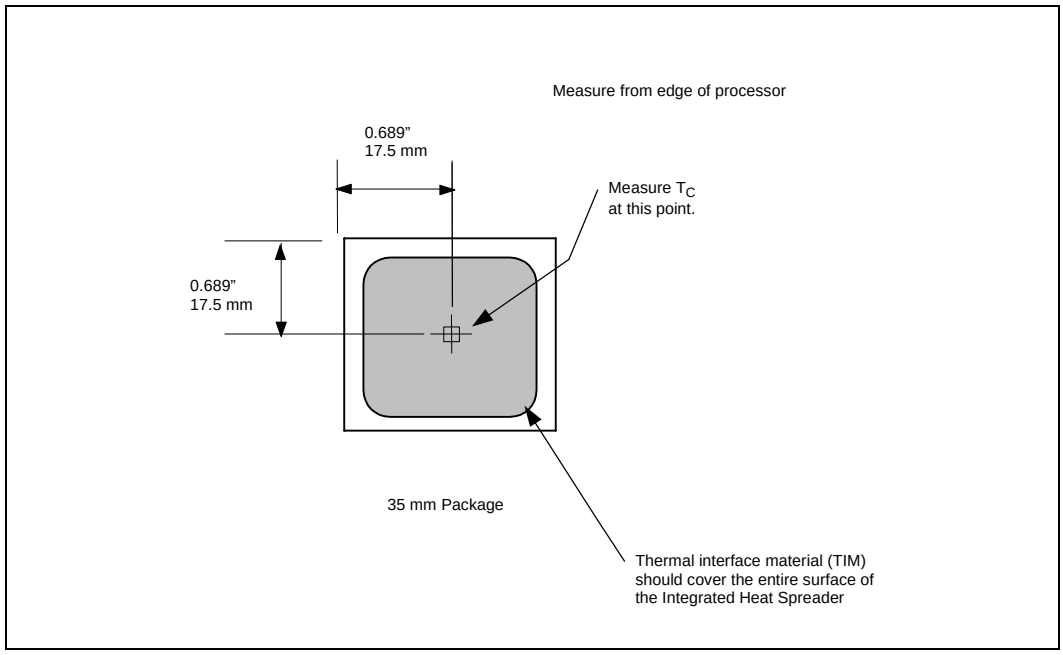
Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

6.2.2 Measurements For Thermal Specifications

6.2.2.1 Processor Case Temperature Measurement

The maximum and minimum case temperatures (T_C) for the Celeron processor in the 478-pin package are specified in Table 33. These temperature specifications are meant to ensure correct and reliable operation of the processor. Figure 31 illustrates where Intel recommends T_C thermal measurements should be made.

Figure 31. Guideline Locations for Case Temperature (T_C) Thermocouple Placement



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7.0 Features

7.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Celeron processor in the 478-pin package samples the hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 34.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a *warm* reset and a *power-on* reset.

Table 34. Power-On Configuration Option Pins

Configuration Option	Pin[1]
Output tristate	SMI#
Execute BIST	INIT#
In Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Symmetric agent arbitration ID	BR0#

NOTES:
1. Asserting this signal during RESET# will select the corresponding option.

7.2 Clock Control and Low Power States

The use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states is allowed in the Celeron processor in the 478-pin package based systems to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 32 for a visual representation of the processor low power states.

7.2.1 Normal State—State 1

This is the normal operating state for the processor.

7.2.2 AutoHALT Powerdown State—State 2

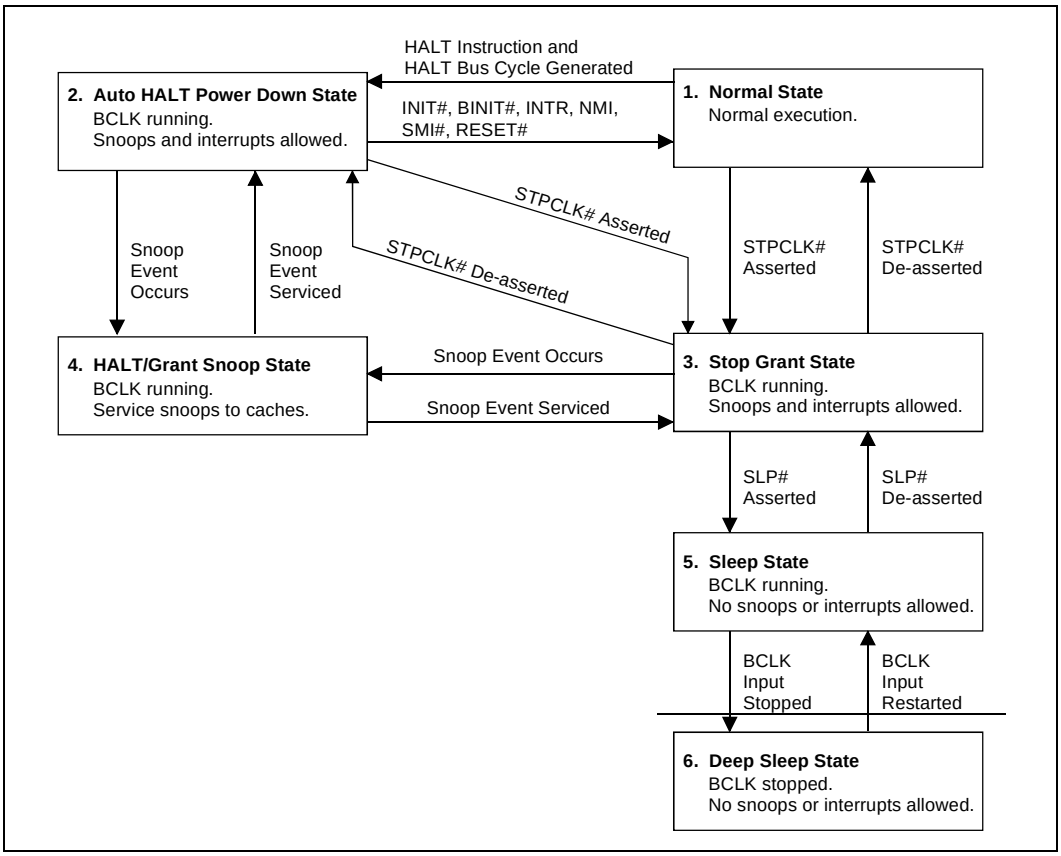
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process bus snoops.

Figure 32. Stop Clock State Machine



7.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 7.2.4). A transition to the Sleep state (see Section 7.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process a system bus snoop.

7.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

7.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop Grant state is out of specification and may result in unapproved operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK[1:0] inputs. (See Section 7.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin must be de-asserted if another asynchronous system bus event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

7.2.6 Deep Sleep State—State 6

Deep Sleep state is the lowest power state the processor can enter while maintaining context. Deep Sleep state is entered by stopping the BCLK[1:0] inputs (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK[1:0] is stopped. To provide maximum power conservation hold the BLCK0 input at V_{OL} and the BCLK1 input at V_{OH} during the Deep Sleep state. Stopping the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior. The processor has to stay in Deep Sleep mode for minimum of 25 µs.

When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions.

7.3 Thermal Monitor

The Thermal Monitor feature found in the Celeron processor in the 478-pin package allows system designers to design lower cost thermal solutions without compromising system integrity or reliability. By using a factory-tuned, precision on-die thermal sensor, and a fast acting thermal control circuit (TCC), the processor, without the aid of any additional software or hardware, can keep the processor's die temperature within factory specifications under nearly all conditions. Thermal Monitor thus allows the processor and system thermal solutions to be designed much closer to the power envelopes of real applications, instead of being designed to the much higher maximum processor power envelopes.

Thermal Monitor controls the processor temperature by modulating the internal processor core clocks. The processor clocks are modulated when the TCC is activated. Thermal Monitor uses two modes to activate the TCC: Automatic mode and On-Demand mode. **Automatic mode is required for the processor to operate within specifications and must first be enabled via BIOS.** Once automatic mode is enabled, the TCC will activate only when the internal die temperature is very near the temperature limits of the processor. When TCC is enabled, and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Clocks will not be off for more than 3 µs when TCC is active. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. Once the temperature has returned to a non-critical level, and the hysteresis timer has expired, modulation ceases and TCC goes inactive. Processor performance will be decrease by ~50% when the TCC is active (assuming a 50% duty cycle), however, with a properly designed and characterized thermal solution the TCC most likely will only be activated briefly when the system is near maximum temperature and during the most power intensive applications.

For automatic mode, the 50% duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers or interrupt handling routines.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Thermal Monitor Control Register is written to a "1" the TCC will be activated immediately, independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via On-Demand mode at the same time automatic mode is enabled AND a high temperature condition exists, the 50% duty cycle of the automatic mode will override the duty cycle selected by the On-Demand mode.

An external signal, PROCHOT# (processor hot) is asserted at any time the TCC is active (either in automatic or On-Demand mode). Bus snooping and interrupt latching are also active while the TCC is active. The temperature at which the thermal control circuit activates is not user configurable and is not software visible.

Besides the thermal sensor and thermal control circuit, the Thermal Monitor feature also includes one ACPI register, one performance counter register, three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Thermal Monitor feature. Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT# (i.e., upon the activation/deactivation of TCC).

If automatic mode is disabled the processor will be operating out of specification and cannot be guaranteed to provide reliable results. Regardless of enabling of the automatic or On-Demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 135 °C. At this point the system bus signal THERMTRIP# will go active and stay active until RESET# has been initiated. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (V_{CC}) must be removed within the timeframe defined in Table 16.

7.3.1 Thermal Diode

The Celeron processor in the 478-pin package incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the Celeron processor in the 478-pin package for thermal management/long term die temperature change purposes. Table 35 and Table 36 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 35. Thermal Diode Parameters

Symbol	Min	Typ	Max	Unit	Notes[1]
$I_{forward\ bias}$	5		450	uA	2
n_ideality	0.9933	1.0045	1.0368		3, 4

NOTES:
1. Not 100% tested. Specified by design characterization.
2. Intel does not support or recommend operation of the thermal diode under reverse bias.
3. At room temperature with a forward bias of 630 mV.
4. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I=Io(e (Vd*q)/(nkT) – 1).

Table 36. Thermal Diode Interface

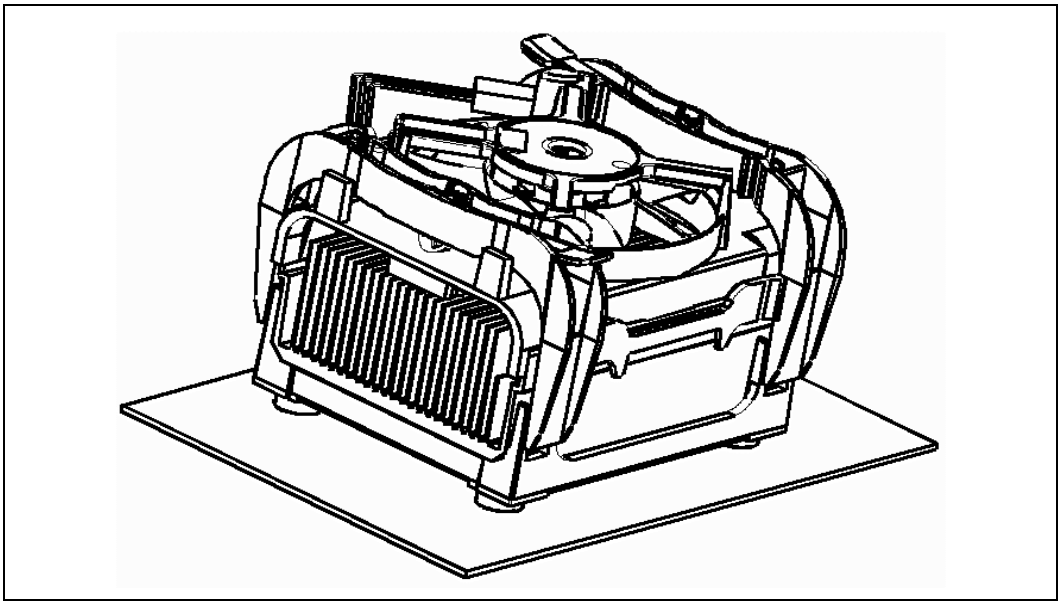
Pin Name	Pin Number	Pin Description
THERMDA	B3	Diode Anode
THERMDC	C4	Diode Cathode

8.0 Boxed Processor Specifications

The Celeron processor in the 478-pin package will also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Celeron processor in the 478-pin package will be supplied with a cooling solution. This chapter documents motherboard and system requirements for the cooling solution that will be supplied with the boxed Celeron processor in the 478-pin package. This chapter is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 33 shows a mechanical representation of a boxed Celeron processor in the 478-pin package.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines* for further guidance. Contact your local Intel Sales Representative for this document.

Figure 33. Mechanical Representation of the Boxed Intel® Celeron® Processor in the 478-Pin Package



NOTE: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

8.1 Mechanical Specifications

8.1.1 Boxed Processor Cooling Solution Dimensions

This section documents the mechanical specifications of the boxed Celeron processor in the 478-pin package. The boxed processor will be shipped with an unattached fan heatsink. Figure 33 shows a mechanical representation of the boxed Celeron processor in the 478-pin package.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 34 (Side Views), and Figure 35 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new motherboard and system designs. Airspace requirements are shown in Figure 38 and Figure 39. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 34. Side View Space Requirements for the Boxed Processor

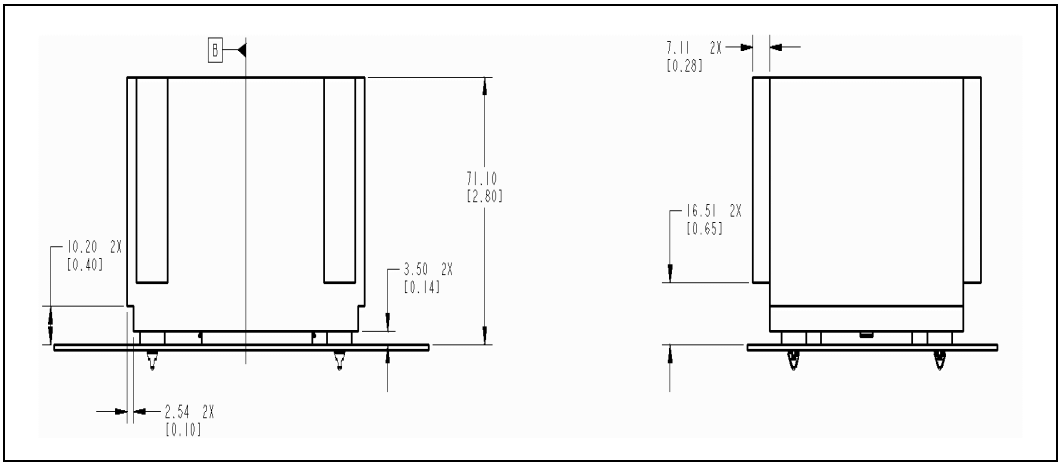
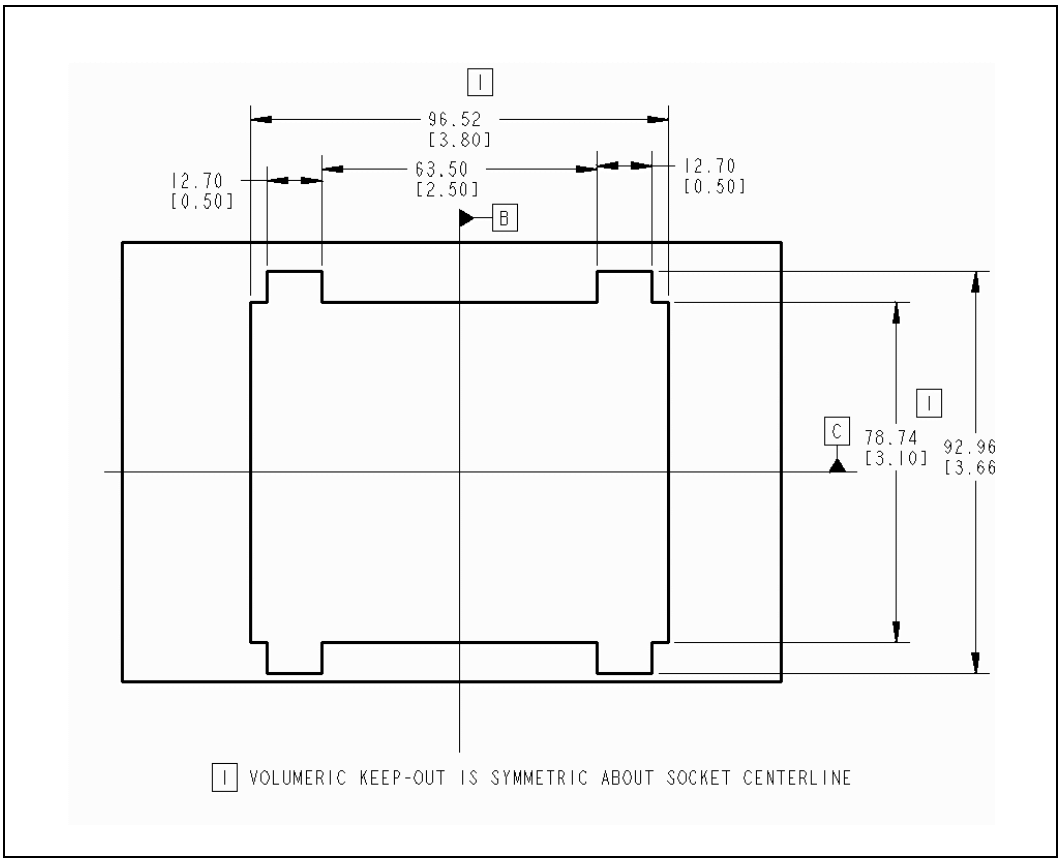


Figure 35. Top View Space Requirements for the Boxed Processor



8.1.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. See Chapter 6.0 and the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines* for details on the processor weight and heatsink requirements.

8.1.3 Boxed Processor Retention Mechanism and Heatsink Attach Clip Assembly

The boxed processor thermal solution requires a processor retention mechanism and a heatsink attach clip assembly, to secure the processor and fan heatsink in the baseboard socket. The boxed processor will not ship with retention mechanisms but will ship with the heatsink attach clip assembly. Motherboards designed for use by system integrators should include the retention mechanism that supports the boxed Celeron processor in the 478-pin package. Motherboard documentation should include appropriate retention mechanism installation instructions.

Note: The processor retention mechanism based on the Intel reference design should be used, to ensure compatibility with the heatsink attach clip assembly and the boxed processor thermal solution. The heatsink attach clip assembly is latched to the retention tab features at each corner of the retention mechanism.

The target load applied by the clips to the processor heat spreader for Intel's reference design is 75 ± 15 lbf (maximum load is constrained by the package load capability). It is normal to observe a bow or bend in the board due to this compressive load on the processor package and socket. The level of bow or bend depends on the motherboard material properties and component layout. Any additional board stiffening devices (such as plates) are not necessary and should not be used with the reference mechanical components and boxed processor. Using such devices increases the compressive load on the processor package and socket, likely beyond the maximum load that is specified for those components. See the *Intel® Pentium® Processor in the 478 pin Package Thermal Design Guidelines* for details on the Intel reference design.

Chassis that have adequate clearance between the motherboard and chassis wall (minimum 0.250 inch) should be selected to ensure that the board's underside bend does not contact the chassis.

8.2 Electrical Requirements

8.2.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 36. Motherboards must provide a matched power header to support the boxed processor. Table 37 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides V_{OH} to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

Note: The motherboard must supply a constantat +12V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 37 shows the location of the fan power connector relative to the processor socket. The motherboard power header should be positioned within 4.33 inches from the center of the processor socket.

Figure 36. Boxed Processor Fan Heatsink Power Cable Connector Description

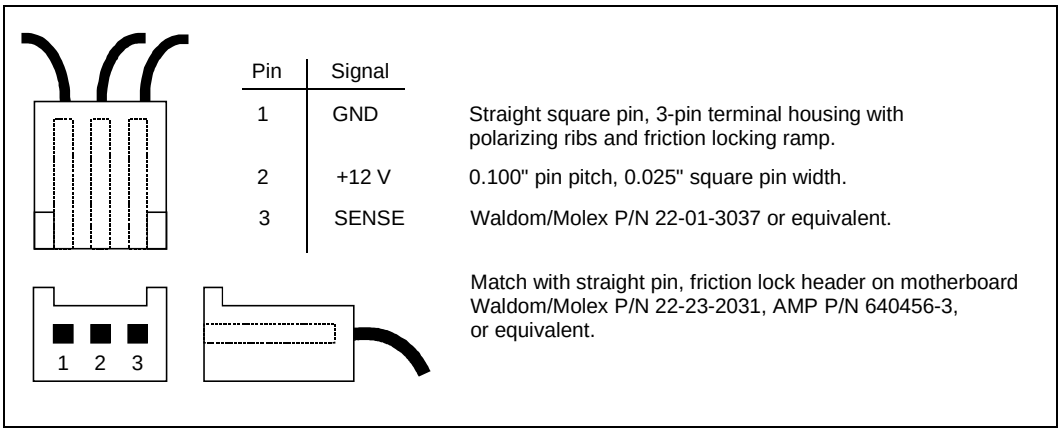
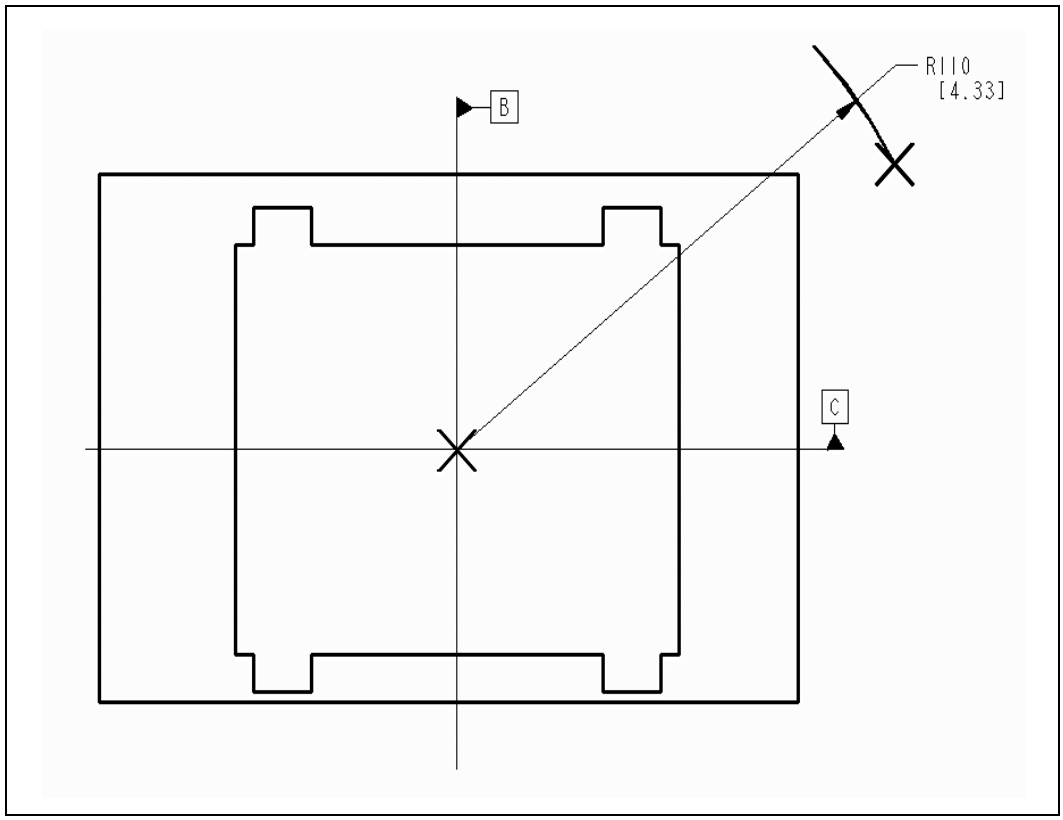


Table 37. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12 V: 12 volt fan power supply	10.2	12	13.8	V	
IC: Fan current draw			740	mA	
SENSE: SENSE frequency		2		pulses per fan revolution	see note

NOTE: Motherboard should pull this pin up to V_{CC} with a resistor.

Figure 37. Motherboard Power Header Placement Relative to Processor Socket



8.3 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

8.3.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 6.0. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 33) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 38 and Figure 39 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 40° C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Figure 38. Boxed Processor Fan Heatsink Airspace Keepout Requirements (Side 1 View)

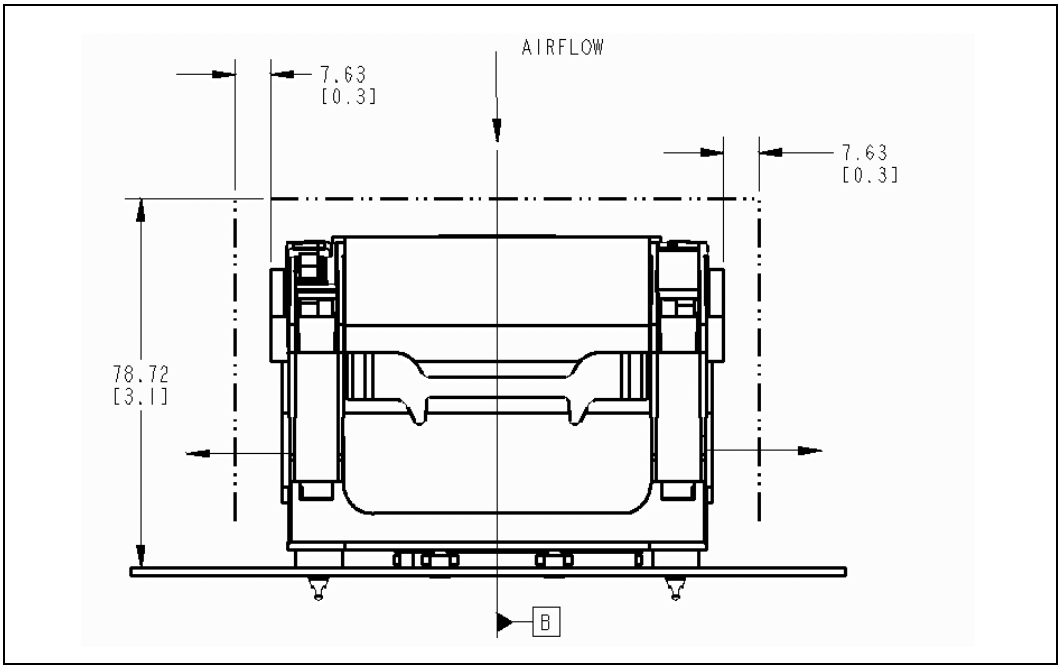
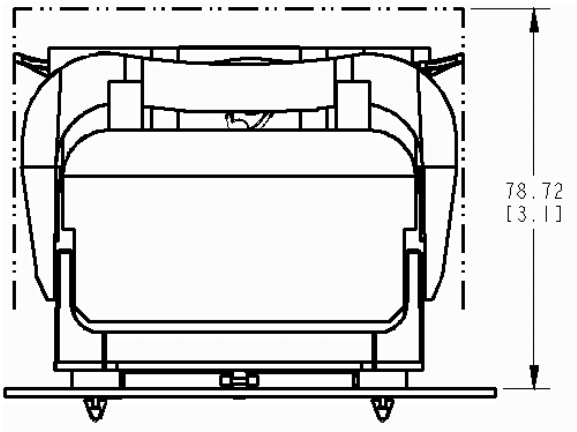


Figure 39. Boxed Processor Fan Heatsink Airspace Keepout Requirements (Side 2 View)



8.3.2 Variable Speed Fan

The boxed processor fan will operate at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed and noise level, while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains below the lower set point. These set points, represented in Figure 40 and Table 38, can vary by a few degrees from fan heatsink to fan heatsink. The internal chassis temperature should be kept below 40ºC. Meeting the processor's temperature specification (see Chapter 6.0) is the responsibility of the system integrator.

Figure 40. Boxed Processor Fan Heatsink Set Points

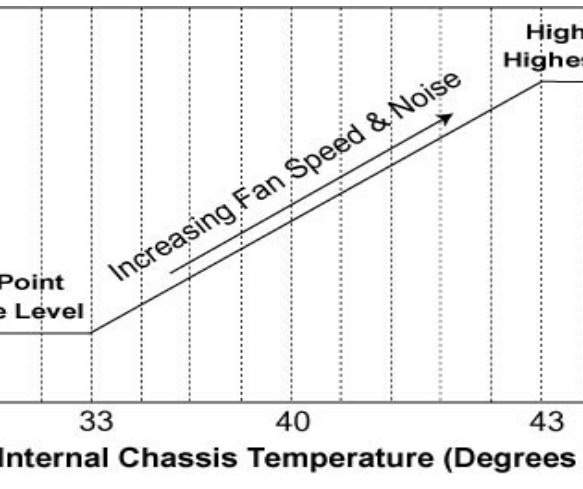


Table 38. Boxed Processor Fan Heatsink Set Points

Boxed Processor Fan Heatsink Set Point (ºC)	Boxed Processor Fan Speed	Notes
33	When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.	1
40	When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.	
43	When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.	1

NOTE:
1. Set point variance is approximately ± 1°C from fan heatsink to fan heatsink

9.0 Debug Tools Specifications

Refer to the *ITP700 Debug Port Design Guide* and the appropriate Platform Design Guide for information regarding debug tools specifications.

9.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Celeron processor in the 478-pin package systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Celeron processor in the 478-pin package systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Celeron processor in the 478-pin package system that can make use of an LAI: mechanical and electrical.

9.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the Celeron processor in the 478-pin package. The LAI pins plug into the socket, while the Celeron processor in the 478-pin package pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Celeron processor in the 478-pin package and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Celeron processor in the 478-pin package heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

9.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.