iC-VR

BIDIRECTIONAL µP INTERFACE TO 24V

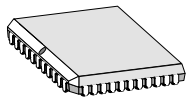
FEATURES

- 2 × 4 bidirectional input/output stages at 24 V
- Input/output mode programmable for each 4 bits
- Guaranteed low-side driving capability of 100 mA_{dc} and 500 mA_{peak} for pulse load
- Short-circuit-proof driver with high electric strength up to 48 V
- Low saturation voltage of 0.4 V at 10 mA and 1.5 V at 500 mA
- Programmable pull-down current sources
- Built-in free-wheeling diodes with externally accessible common cathode
- Flashing function for the outputs
- Programmable digital input filters with externally adjusted filtering times
- Bus capability via high-speed microprocessor interface
- Programmable interrupt output
- Shutdown at overtemperature and low voltage

APPLICATIONS

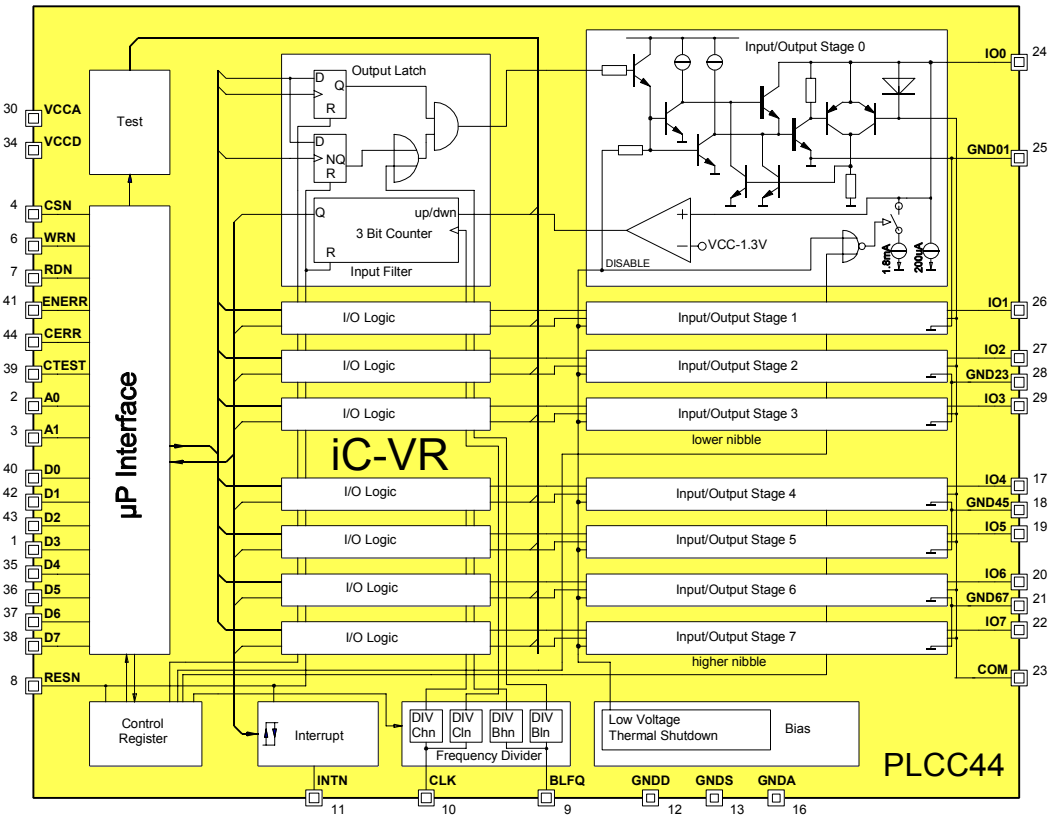
- Dual quad low-side driver as bidirectional µP interface with digital filtering in 24 V industrial applications

PACKAGES



PLCC44

BLOCK DIAGRAM



DESCRIPTION

iC-VR is an 8-fold low-side driver with integrated control logic which is divided internally into two mutually independent blocks (nibbles).

In the input mode, ports IO0 to IO7 can be used to record logical levels. In this process, a programmable pull-down current (200 µA or 2 mA) sets a defined level and functions as the biasing current for switching contacts. The stages programmed as outputs can drive any desired loads (e. g. lamps, long cables, relays) at a continuous current of 100 mA or 500 mA in pulse operation. The free-wheeling currents created upon each stage turn-off are discharged through the integrated free-wheeling diodes to a voltage applied externally to the COM pin; a circuit with a Zener diode is also possible.

In the event of a short circuit, a protective circuit breaker ensures that the output stage affected does not just simply switch off but is instead clocked as a function of the load. As a result, the current assumes a low average value. The output stage is ready for operation immediately just as soon as the cause of the short circuit has been eliminated.

The shutdown at overtemperature protects the IC against thermal destruction by causing the output stages to turn off and the pull-down currents to be reduced from 2 mA to 200 µA. This shutdown is also triggered in case of undervoltage at VCC.

Due to the microprocessor interface the iC-VR can be operated directly on a bus system. The interface consists of the data bits D0 to D7 and the associated control signals A0, A1, CSN, WRN and RDN. The signal CLK clocks the implemented digital input filter and BLFQ clocks the programmed flashing function. In the event of a signal change of the I/O pins programmed as inputs, an interrupt signal can be generated at output INTN.

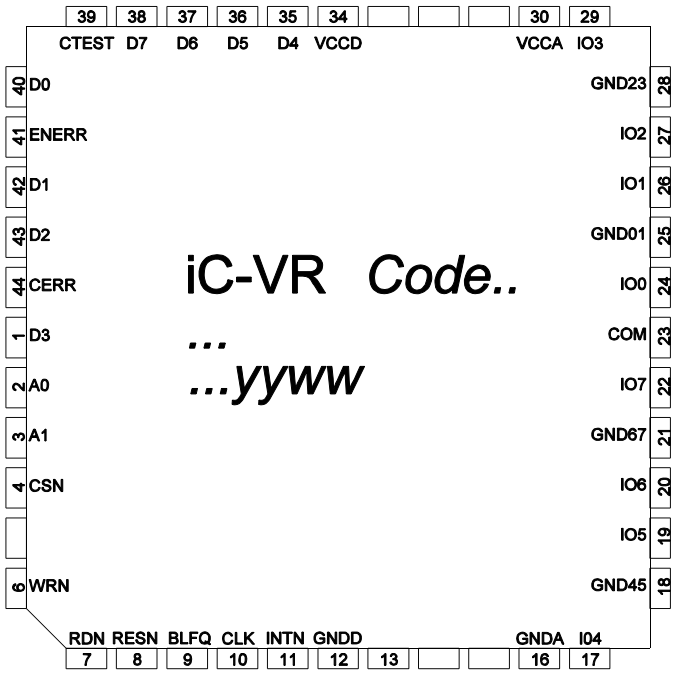
Activating the input RESN resets the initial condition.

Chip programming is conducted via four addresses at A0 and A1. During this programming, presettings for flashing frequencies, filtering times, interrupt control, pull-down currents and input/output mode, etc. are stored in two registers (CONTROL WORD1+2).

All inputs and outputs are protected with diodes against destruction due to ESD.

PACKAGES PLCC44 to JEDEC Standard

PIN CONFIGURATION PLCC44
(top view)



PIN FUNCTIONS PLCC44

No.	Name	Function	Description	No.	Name	Function	Description
1	D3	B	Bus Data Bit 3	23	COM		Diodes, common cathode
2	A0	I	Address	24	IO0	B	I/O Stage 0
3	A1	I	Address	25	GND01		Ground Stage 0+1
4	CSN	I	Chip Select	26	IO1	B	I/O Stage 1
5	n.c.			27	IO2	B	I/O Stage 2
6	WRN	I	Write Enable	28	GND23		Ground Stage 2+3
7	RDN	I	Read Enable	29	IO3	B	I/O Stage 3
8	RESN	I	Reset	30	VCCA		+5 V Supply (analog section)
9	BLFQ	I	Clock, flashing function	31	n.c.		
10	CLK	I	Clock, filter function	32	n.c.		
11	INTN	O	Interrupt Report	33	n.c.		
12	GNDD		Digital Ground	34	VCCD		+5 V Supply (digital section)
13	n.c.			35	D4	B	Bus Data Bit 4
14	n.c.			36	D5	B	Bus Data Bit 5
15	n.c.			37	D6	B	Bus Data Bit 6
16	GNDA		Analog Ground	38	D7	B	Bus Data Bit 7
17	IO4	B	I/O Stage 4	39(*)	CTEST		
18	GND45		Ground Stage 4+5	40	D0	B	Bus Data Bit 0
19	IO5	B	I/O Stage 5	41(*)	ENERR		
20	IO6	B	I/O Stage 6	42	D1	B	Bus Data Bit 1
21	GND67		Ground Stage 6+7	43	D2	B	Bus Data Bit 2
22	IO7	B	I/O Stage 7	44(x)	CERR		

*: pin needs external wiring to Ground
x: pin should left open
Function: I = Input, O = Output, B = bidirectional

PROGRAMMING

Selection of functions

Address		Data Word D7..D0							
		higher nibble				**lower nibble**			
		Selected I/O Stage function:							
		Input		Output		Input		Output	
A1	**A0**	Write	Read	Write	Read	Write	Read	Write	Read
0	0	Test Pattern	IR Inputs	Outputs	Outputs	Test Pattern	IR Inputs	Outputs	Outputs
0	1	IR Enable	IR Enable	Pulse Enable	Pulse Enable	IR Enable	IR Enable	Pulse Enable	Pulse Enable
1	0	Control Word 2	Inputs	Control Word 2	Feedback I/O Stages	Control Word 2	Inputs	Control Word 2	Feedback I/O Stages
1	1	Control Word 1	Control Word 1	Control Word 1	Control Word 1	Control Word 1	Control Word 1	Control Word 1	Control Word 1

Reading the inputs or the output feedback (IO7..0 to D7..0)
I/O stage with input function: A high level at IOx generates a high signal at Dx (selection of functions: read inputs) during the course of the digital hysteresis.
I/O stage with output function: A high level at IOx generates a low signal at Dx (selection of functions: read feedback of the outputs).
The inversion while reading back the outputs (I/O stage with output function) occurs so that the same signal is applied to Dx as was programmed for switching the output stage on or off, for example: switching on the final stage with Dx = high results in low level at IOx. After the digital hysteresis ends, Q becomes low, the microprocessor interface inverts this message and a high signal can be read back via Dx. The microprocessor can check the output state in this manner.

Test
The test circuit consists of registers which can be set via the microprocessor interface (test pattern). Its content is applied via constantly active OR gates to the counting direction inputs UP/DOWN (D7..0 to UP/DOWN7..0). In response to a reset (low signal at RESN) the registers are set to low; as a result, there is no effect on the UP/DOWN inputs.
In the test mode (control word 2, bit 2 and 6 at high) the comparators of the I/O stages are switched off and only the test registers continue to operate the UP/DOWN inputs. Any desired input signals can be entered to test all digital functions; the microprocessor can also conduct a system test in this manner.

Interrupt enable
The interrupt generation can be activated separately for every I/O stage with input function. The interrupt enable is programmed via the data word DO..7 (function selection IR enable: 1 = stage relevant, 0 = stage not relevant). If a signal change is recognized for an I/O stage with input function - after the digital hysteresis due to change at Qx - and if this stage is enabled for interrupt generation, this is indicated with INTN = low. The interrupt message as well as the interrupt register which shows the stages with signal changes are reset via control word 2 (writing bit 0 = 1 is sufficient; bit 0 = 0 is set by the chip automatically).

Signal changes which would be relevant for an interrupt generation could occur in the read-out phase following an interrupt message. These signal changes are lost when the interrupt register is deleted. As an alternative, the read-out of the interrupt register is possible (functional selection: read IR inputs). The registers can then be reset separately by blocking the IR enable for each reporting stage singly and then releasing it (functional selection: IR enable).

Filter periods

The input comparator of each I/O stage switches the counting direction of a 3 bit counter. The counter output Q does not change until the final status is reached (to high for high level at IOx, to low for low level at IOx if constantly applied during the filter period).
The counter is clocked externally (pin CLK); the divisor for the clock frequency can be programmed separately for both nibbles. A low signal at reset input RESN resets the counters to the value 3. Due to the digital hysteresis, the change of an input signal is therefore not recognized until the selected filter period has elapsed.

Pulse enable and pulse times

The flashing or pulsing function can be switched on separately for each I/O stage with output function. The programming of the divisors for the flashing frequency input BLFQ (control word 1, bits 0,1 and 4,5) is conducted for each nibble. The clock signal at BLFQ is transfered with the slope of CLK (synchronized). For this reason the clock frequency for CLK must be higher than the clock frequency for BLFQ, e. g. 2 MHz for CLK and 50 Hz for BLFQ.

Control Word 1								
	higher nibble				**lower nibble**			
Bit Name	7 FH0	6 FH1	5 PH0	4 PH1	3 FL0	2 FL1	1 PL0	0 PL1

Control Word 1 (lower nibble)						
Filtering Time				Flashing Pulse Duration		
Bit 3 FLO	Bit 2 FL1			Bit 1 PLO	Bit 0 PL1	
0 1 0 1	0 0 1 1	14.5 * CLK 896.5 * CLK 3584.5 * CLK 7168.5 * CLK	± 1 * CLK ± 64 * CLK ± 256 * CLK ± 512 * CLK	0 1 0 1	0 0 1 1	BLFQ BLFQ * 2 BLFQ * 4 BLFQ * 16

Control Word 1 (higher nibble)						
Filtering Time				Flashing Pulse Duration		
Bit 7 FHO	Bit 6 FH1			Bit 5 PHO	Bit 4 PH1	
0 1 0 1	0 0 1 1	14.5 * CLK 896.5 * CLK 3584.5 * CLK 7168.5 * CLK	± 1 * CLK ± 64 * CLK ± 256 * CLK ± 512 * CLK	0 1 0 1	0 0 1 1	BLFQ BLFQ * 2 BLFQ * 4 BLFQ * 16

Control Word 2								
	higher nibble				**lower nibble**			
Bit Name	7 NIOH	6 TSTH	5 IBH	4 not used	3 NIOL	2 TSTL	1 IBL	0 EOI

Control Word 2 (lower nibble)		
Interrupt		
Bit 0 (EOI)	0 1	Interrupt is not cancelled Clearing Interrupt
Current Sources at I/O Pins		
Bit 1 (IBL)	0 1	Pull-Down Current 200 µA Pull-Down Current 2 mA
Test		
Bit 2 (TSTL)	0 1	Feedback of I/O stages active (OR gated with test pattern) Test pattern activated, feedback of I/O stages switched off
Input/Output Mode		
Bit 3 (NIOL)	0 1	Input Mode Output Mode

Control Word 2 (higher nibble)		
Bit 4	-	not used
Current Source at I/O Pins		
Bit 5 (IBH)	0 1	Pull-Down Current 200 µA Pull-Down Current 2 mA
Test		
Bit 6 (TSTH)	0 1	Feedback of I/O stages active (OR gated with test pattern) Test pattern activated, feedback of I/O stages switched off
Input/Output Mode		
Bit 7 (NIOH)	0 1	Input Mode Output Mode

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VCCA VCCD	Supply Voltage			-0.3	6	V
G201	V(COM)	Voltage at COM			-0.3	49	V
G202	Vact(IO)	Voltage at IOx	IOx= Io (* see below)		-0.3	49	V
G203	Idc(COM)	Current in COM			-500	0	mA
G204	Ipk(COM)	Peakcurrent in COM	τ= 2ms, T≥ 2s	2	-1000	-	mA
G205	Isc(COM)	Free-Wheeling Current in COM			-1.3		A
G206	Idc(COM)	Current in IOx			-1		mA
G207	Ipk(IOx)	Peakcurrent in IOx	IOx= Io, τ= 2ms, T≥ 2s	2	-1	600	mA
G208	Ipsc (Iox)	Peakcurrent in IOx	IOx= Io, Overload current protection		-1.3		A
G301	V(IOx)	Voltage at IO0..3, IO4..7	IBL= 0, IBH= 0 (current source 200µA)		-0.3	49	V
G302	V(IOx)	Voltage at IO0..3, IO4..7	IBL= 1, IBH= 1 (current source 2mA)		-0.3	26	V
			τ= 2ms, T≥ 2s		-0.3	49	V
G401	Imx (VCCD)	Current in VCCD, GNDD			-50	50	mA
G402	Ic()	Current in Clamping Diodes at CSN, WRN, RDN, A0, A1, D0..7, RESN, CLK, BLFQ	D0..7 set to inputs		-20	20	mA
G402	I()	Current in D0..7,INTN	D0..7 set to outputs			25	mA
G404	Ilu()	Peakcurrent in CSN, WRN, RDN, A0, A1, D0..7, RESN, CLK, BLFQ, INTN (Latch-Up Strength)	pulse duration ≤ 10µs		-100	100	mA
EG1	Vd()	ESD Susceptibility, all Inputs and Outputs	MIL-STD-883, Method 3015, HBM 100pF discharged through 1.5kΩ			2	kV
TG1	Tj	Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature			-40	150	°C

(*) IOx= Io : pin set to output, active low, x ∈ 0..7

THERMAL DATA

Operating Conditions: VCC= VCCA= VCCD= 5V ±10%

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range			0		70	°C
T2	Rthja	Thermal Resistance Chip to Ambient	PLCC44 surface mounted on PCB			55		K/W

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VCCA= VCCD= 5V ±10%, Tj= 0..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VCCA VCCD	Permissible Supply Voltage Range				4.5		5.5	V
002	I(VCCA)	Supply Current in VCCA, power section	IO0..7= lo, unloaded	0 27 70 125		5 5 5 5		65 60 55 55	mA mA mA mA
003	I(VCCD)	Supply Current in VCCD, digital section	all logic inputs lo= 0V or hi= VCC			0		10	mA
004	I(VCCD)	Supply Current in VCCD, digital section	all logic inputs lo= 0.8V				80		mA
005	I(VCCD)	Supply Current in VCCD, digital section	all logic inputs lo= 2.0V				100		mA
Bias, Thermal Shutdown and Low Voltage Detection									
101	VCCon	Turn-on Threshold VCC				3.6	4	4.4	V
102	VCCoff	Undervoltage Threshold at VCC	decreasing Supply VCC			3.5	3.9	4.3	V
103	VCChys	Hysteresis	VCChys= VCCon-VCCoff			40	100	250	mV
104	Toff	Thermal Shutdown Threshold				120	135	150	°C
105	Thys	Thermal Shutdown Hysteresis	Thys= Toff - Ton			4	8	12	°C
I/O Stages: Low-side Driver									
201	Ilk(COM)	Leakage Current in COM	V(COM)= 25V, V(IOx)= 0V					100	µA
202	Vf(COM)	Forward Voltage of the Free-Wheeling Diodes	Vf()= V(IOx)-V(COM); I(IOx→COM)= 100mA, IOx= hi or set to Inputs			0.5		1.5	V
203	Vs(IO)	Saturation Voltage lo at IOx	I(IOx)= 10mA, IO0..7= lo		1			0.4	V
204	Vs(IO)	Saturation Voltage lo at IOx	I(IOx)= 100mA, IO0..7= lo		1			0.6	V
205	Vs(IO)	Saturation Voltage lo at IOx for pulse load	I(IOx)= 500mA, IO0..7= lo, τ= 2ms, T≥ 2s		1			1.5	V
206	Ioff(IO)	Threshold Current in IOx for Overcurrent Cut-off	IOx= lo, V(IOx)= 0..25V			0.5		1.3	A
207	Ion(IO)	Free-Wheeling Current I(IOx→COM) for Cut-off release	IOx= lo, V(IOx)= 0..25V			0.1		20	mA
208	f(IO)	Cut-off Oscillation Frequency	depends on Load			0.1		20	MHz
209	Iav(IO)	Mean Current in IOx during Cut-off	IOx= lo, V(IOx)= 0..25V			50		700	mA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VCCA= VCCD= 5V ±10%, Tj= 0..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
I/O Stages: Comparator									
301	Idwn(IO)	Pull-down Current in IOx	V(IOx)= 3..48V, IBL= 0, IBH= 0, IO0..7= hi or set to Inputs			120	200	280	µA
302	Idwn(IO)	Pull-down Current in IOx	V(IOx)= 3..25V, IBL= 1, IBH= 1, IO0..7= hi or set to Inputs			1.4	2	2.6	mA
303	V0(IO)	Open-Circuit Voltage at IOx	IOx open, IO0..7= hi or set to Inputs					1	V
304	Vt()hi	Threshold Voltage hi at IOx						4.6	V
305	Vt()lo	Threshold Voltage lo at IOx				3			V
µP-Interface, I/O-Logic, Frequency Divider, Interrupt									
401	Ilk(Dx)	Leakage Current in Dx	D0..7 set to Inputs			-5		5	µA
402	Ilk(Dx)	Leakage Current in Schmitt Trigger Inputs CSN, WRN, RDN, A0, A1, RESN, CLK, BLFQ				-1		1	µA
403	Vt()hi	Threshold Voltage hi at Schmitt Trigger Inputs CSN, WRN, RDN, A0, A1, RESN, CLK, BLFQ, D0..7	D0..7 set to Inputs					2.3	V
404	Vt()lo	Threshold Voltage lo at Schmitt Trigger Inputs CSN, WRN, RDN, A0, A1, RESN, CLK, BLFQ, D0..7	D0..7 set to Inputs			0.7			V
405	Vt()hys	Hysteresis at Schmitt Trigger Inputs CSN, WRN, RDN, A0, A1, RESN, CLK, BLFQ, D0..7	Vt()hys= Vt()hi-Vt()lo; D0..7 set to Inputs			0.3			V
406	Vs()hi	Saturation Voltage hi at INTN	Vs()hi= VCCD-V(INTN); INTN=hi, I(INTN)= -100µA					0.2	V
407	Vs()hi	Saturation Voltage hi at INTN	Vs()hi= VCCD-V(INTN); INTN=hi, I(INTN)= -2mA					0.8	V
408	Vs()lo	Saturation Voltage lo at INTN	INTN= lo, I(INTN)= 100µA					0.2	V
409	Vs()lo	Saturation Voltage lo at INTN	INTN= lo, I(INTN)= 2mA					0.49	V
410	Vs(Dx)hi	Saturation Voltage hi at Dx	Vs(Dx)hi= VCCD-V(Dx); Dx= hi, I(Dx)= -100µA					0.2	V
411	Vs(Dx)hi	Saturation Voltage hi at Dx	Vs(Dx)hi= VCCD-V(Dx); Dx= hi, I(Dx)= -4mA					0.8	V
412	Vs(Dx)lo	Saturation Voltage lo at Dx	Dx= lo, I(Dx)= 100µA					0.2	V
413	Vs(Dx)lo	Saturation Voltage lo at Dx	Dx= lo, I(Dx)= 4mA					0.49	V
414	Vc()hi	Clamp Voltage hi at CSN, WRN, RDN, A0, A1, RESN, CLK,BLFQ, D0..7, INTN, CERR	Vc()hi= V()-VCC, I()= 20mA			0.4		2.5	V
415	Vc()lo	Clamp Voltage lo at CSN, WRN, RDN, A0, A1, RESN, CLK, BLFQ, D0..7, INTN, CERR	I()= -20mA			-1.8		-0.4	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VCCA= VCCD= 5V ±10%, Tj= 0..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Switching Characteristics									
501	tc(CLK)	Permissible Cycle Duration CLK				400			ns
502	tw(CLK)	Permissible Pulse Width lo at CLK				200			ns
503	tc(BLFQ)	Permissible Cycle Duration BLFQ				100			ms
504	tw(BLFQ)	Permissible Pulse Width lo at BLFQ				50			ms
505	tphl()	Propagation Delay until IOx= lo	Write Cycle, WRN: hi→lo					2	µs
506	tplh()	Propagation Delay until IOx= off	Write Cycle, WRN: hi→lo					3	µs
507	tp()Ion	Current Source Enable Time at IOx	Write Cycle, WRN: hi→lo					5	µs
508	tp()Ioff	Current Source Disable Time at IOx	Write Cycle, WRN: hi→lo					5	µs
509	tp(IOx→ up/dwn)	Propagation Delay Input IOx to Up/Dwn Filter Input						5	µs

ELECTRICAL CHARACTERISTICS: WAVEFORMS

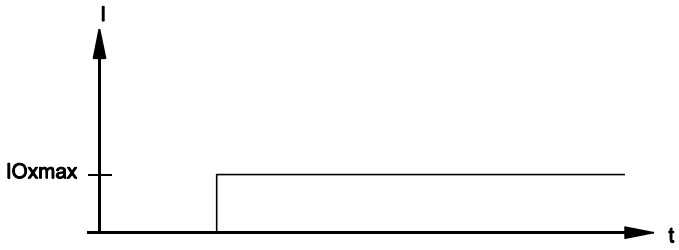


Figure 1: DC load

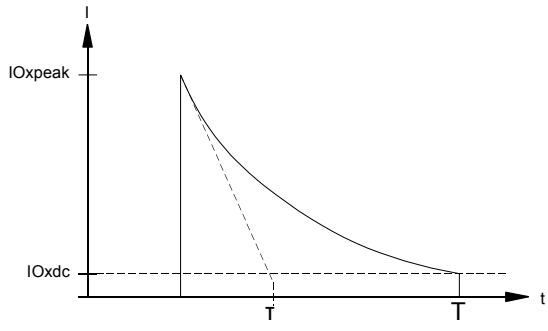


Figure 2: Pulse load, Pulse duration 2 ms

OPERATING REQUIREMENTS: µP INTERFACE

Operating Conditions: VCC= VCCA= VCCD= 5V ±10%, Ta= 0..70°C, CL()= 150pF,
input levels lo= 0..0.45V, hi= 2.4V..VCC, see Fig. 3 for reference levels and waveforms

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
Data Word Read Timing							
I1	t_{AR}	Setup Time: CSN, A0, A1 set before RDN hi→lo		4	30		ns
I2	t_{RA}	Hold Time: CSN, A0, A1 stable after RDN lo→hi		4	10		ns
I3	t_{RD}	Read Data Access Time: Data valid after RDN hi→lo		4		120	ns
I4	t_{DF}	Read Data Hold Time: Ports high impedance after RDN lo→hi		4		65	ns
I5	t_{RW}	Recovery Time between Read/Write Cycles		4	165		ns
Data Word Write Timing							
I6	t_{AW}	Setup Time: CSN, A0, A1 set before WRN hi→lo		4	30		ns
I7	t_{DW}	Write Data Setup Time: Data valid before WRN lo→hi		4	100		ns
I8	t_{WA}	Hold Time: CSN, A0, A1 stable after WRN lo→hi		4	10		ns
I9	t_{WD}	Write Data Hold Time: Data valid after WRN lo→hi		4	10		ns

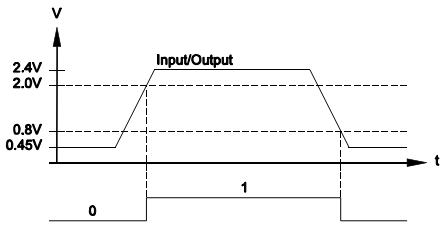


Figure 3: Reference levels

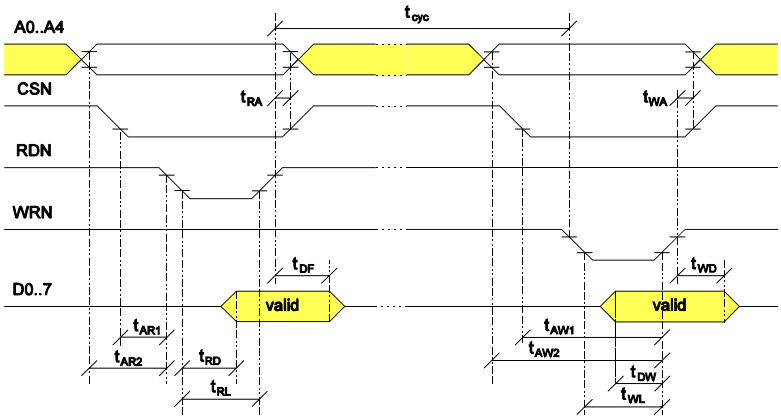


Figure 4: Data word read/write timing

ORDERING INFORMATION

Type	Package	Order designation
iC-VR	PLCC44	iC-VR PLCC44

For information about prices, terms of delivery, options for other case types, etc., please contact:

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