16Mb (512K x 36 & 1M x 18) SRAM

Features

- 512K x 36 or 1M x 18 organization
- CMOS technology
- Double-data-rate and single-data-rate synchronous mode of operation
- Pipeline mode of operation
- Self-timed late write with full data coherency
- Single differential clock
- 1.8V high-speed transceiver logic (HSTL) I/O
- 2.5V power supply, 1.8V V_{DDQ}
- Registered addresses, controls, and data-ins
- Burst mode of operation
- Common I/O
- Asynchronous output enable
- Boundary scan using a limited set of JTAG 1149.1 functions
- 9 x 17 bump ball grid array package with SRAM JEDEC standard pinout and boundary SCAN order
- Programmable impedance output driver

Description

The IBM043616CBLBC and IBM041816CBLBC 16Mb SRAMs are synchronous pipeline-mode, high-performance CMOS static random-access memories that have wide I/O and achieve 2.2ns cycle times. Single differential CK clocks are used to initialize the read/write operation, and all internal operations are self-timed. At the rising edge of the CK clock, addresses and controls are registered internally. Data-outs are updated from output registers on the next rising and falling edges of the CK clock, hence the double data rate. Internal write buffers allow write data to follow one cycle after addresses and controls. The SRAM is operated with a single 2.5V power supply and is compatible with HSTL I/O interfaces.

x36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA13	SA11	ZQ	SA10	SA8	V_{DDQ}	V_{SS}
B	DQ23	DQ20	SA14	V_{SS}	B1	V_{SS}	SA7	DQ15	DQ12
C	V_{SS}	V_{DDQ}	SA15	SA12	$\overline{G}$	SA9	SA6	V_{DDQ}	V_{SS}
D	DQ24	DQ21	SA18	V_{SS}	V_{DD}	V_{SS}	SA5	DQ14	DQ11
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	DQ25	CQ	DQ18	V_{DD}	V_{DD}	V_{DD}	DQ17	CQ	DQ10
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ26	DQ22	DQ19	V_{DD}	$\overline{CK}$	V_{DD}	DQ16	DQ13	DQ9
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	DQ27	DQ31	DQ34	V_{SS}	B2	V_{SS}	DQ1	DQ4	DQ8
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3	MODE[1]	V_{SS}	V_{DDQ}	V_{SS}
M	DQ28	$\overline{CQ}$	DQ35	V_{DD}	V_{DD}	V_{DD}	DQ0	$\overline{CQ}$	DQ7
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	DQ29	DQ32	NC	V_{SS}	V_{DD}	V_{SS}	SA4	DQ3	DQ6
R	V_{SS}	V_{DDQ}	V_{DD}	SA17	SA1	SA2	V_{DD}	V_{DDQ}	V_{SS}
T	DQ30	DQ33	SA16	V_{SS}	SA0	V_{SS}	SA3	DQ2	DQ5
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC[2]	V_{DDQ}	V_{SS}

1. Connect the Mode pin to V_{SS}. The Mode pin has a very small pull down, less than 5µA current at V_{DD} input.
2. ESD protection diodes reside on this NC bump.

x18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA13	SA11	ZQ	SA10	SA8	V_{DDQ}	V_{SS}
B	NC	DQ10	SA14	V_{SS}	B1	V_{SS}	SA7	NC	DQ5
C	V_{SS}	V_{DDQ}	SA15	SA12	$\overline{G}$	SA9	SA6	V_{DDQ}	V_{SS}
D	DQ11	NC	SA18	V_{SS}	V_{DD}	V_{SS}	SA5	DQ7	NC
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	NC	CQ	NC	V_{DD}	V_{DD}	V_{DD}	DQ8	NC	DQ4
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ12	NC	DQ9	V_{DD}	$\overline{CK}$	V_{DD}	NC	DQ6	NC
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	NC	DQ15	NC	V_{SS}	B2	V_{SS}	DQ0	NC	DQ3
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3	MODE[1]	V_{SS}	V_{DDQ}	V_{SS}
M	DQ13	NC	DQ17	V_{DD}	V_{DD}	V_{DD}	NC	$\overline{CQ}$	NC
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	NC	DQ16	SA19	V_{SS}	V_{DD}	V_{SS}	SA4	NC	DQ2
R	V_{SS}	V_{DDQ}	V_{DD}	SA17	SA1	SA2	V_{DD}	V_{DDQ}	V_{SS}
T	DQ14	NC	SA16	V_{SS}	SA0	V_{SS}	SA3	DQ1	NC
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC[2]	V_{DDQ}	V_{SS}

1. Connect the Mode pin to V_{SS}. The Mode pin has a very small pull down, less than 5µA current at V_{DD} input.
2. ESD protection diodes reside on this NC bump.

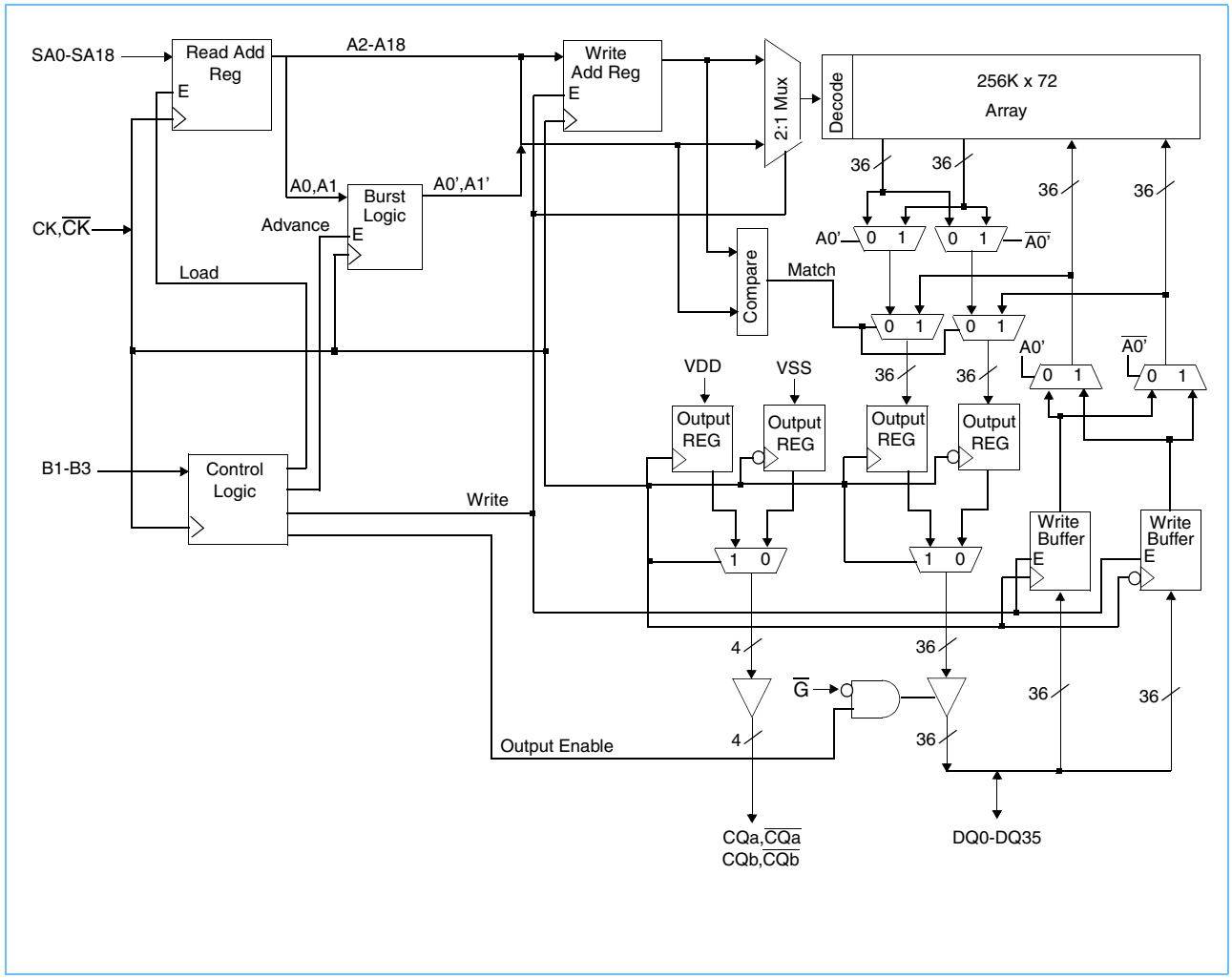
Pin Description

SA0–SA19	Address Input (SA0–SA1 burst-control starting addresses)	TDO	IEEE® 1149.1 Test Output (LVTTL level)
DQ0–DQ35	Data I/O	$\overline{G}$	Asynchronous Output Enable
CQ, $\overline{CQ}$	Differential Echo Clocks	MODE	Mode Pin. Connect to V_{SS}. A waiver to float Mode may be obtained; contact your field applications engineer (FAE).
CK, $\overline{CK}$	Differential Input Register Clocks	V_{REF}	HSTL Input Reference Voltage
B1	B1 = 0 initiates a Load operation	V_{DD}	Power Supply (2.5V)
B2	B2 = 0 initiates a Write operation	V_{SS}	Ground
B3	B3 = 0 Double Data Rate, B3 = 1 Single Data Rate	V_{DDQ}	Output Power Supply
$\overline{LBO}$	Linear Burst Order ($\overline{LBO}$ = 1, interleave mode; $\overline{LBO}$ = 0, linear mode), (can be tied to V_{DD} or V_{SS})	ZQ	Output Driver Impedance Control
TMS, TDI, TCK	IEEE 1149.1 Test Inputs (LVTTL levels)	NC	No Connect

Ordering Information

Part Number	Organization	Cycle Time (ns)	Package
IBM043616CBLBC-22	512K x 36	2.2	9 x 17 BGA
IBM043616CBLBC-24	512K x 36	2.4	9 x 17 BGA
IBM043616CBLBC-27	512K x 36	2.7	9 x 17 BGA
IBM043616CBLBC-30	512K x 36	3.0	9 x 17 BGA
IBM041816CBLBC-22	1M x 18	2.2	9 x 17 BGA
IBM041816CBLBC-24	1M x 18	2.4	9 x 17 BGA
IBM041816CBLBC-27	1M x 18	2.7	9 x 17 BGA
IBM041816CBLBC-30	1M x 18	3.0	9 x 17 BGA

Block Diagram (x36 Double Data Rate Mode)



SRAM Features

Double Data Rate (DDR) and Single Data Rate (SDR) Modes

The timing diagram on page 6 shows input and output data placements for both DDR and SDR modes. In DDR read mode, two sets of data-outs are generated from the second rising and falling edges of the CK clock, assuming the first rising edge of the CK clock samples the base address. The first of the two data-out sets (DOUT-A) is generated from the sampled base address (Base-A). The second data-out set (DOUT-A') is generated from the next burst-order address, according to the burst-order definition. Similarly, a DDR write requires data-in placement on the second rising and falling CK edges. In SDR read mode, only one set of data-outs is generated from the second rising CK edge. In SDR write mode, one set of data-ins is sampled on the second rising CK edge. The user may switch from DDR to SDR mode (or vice-versa) during any LOAD (B1 = 0) operation.

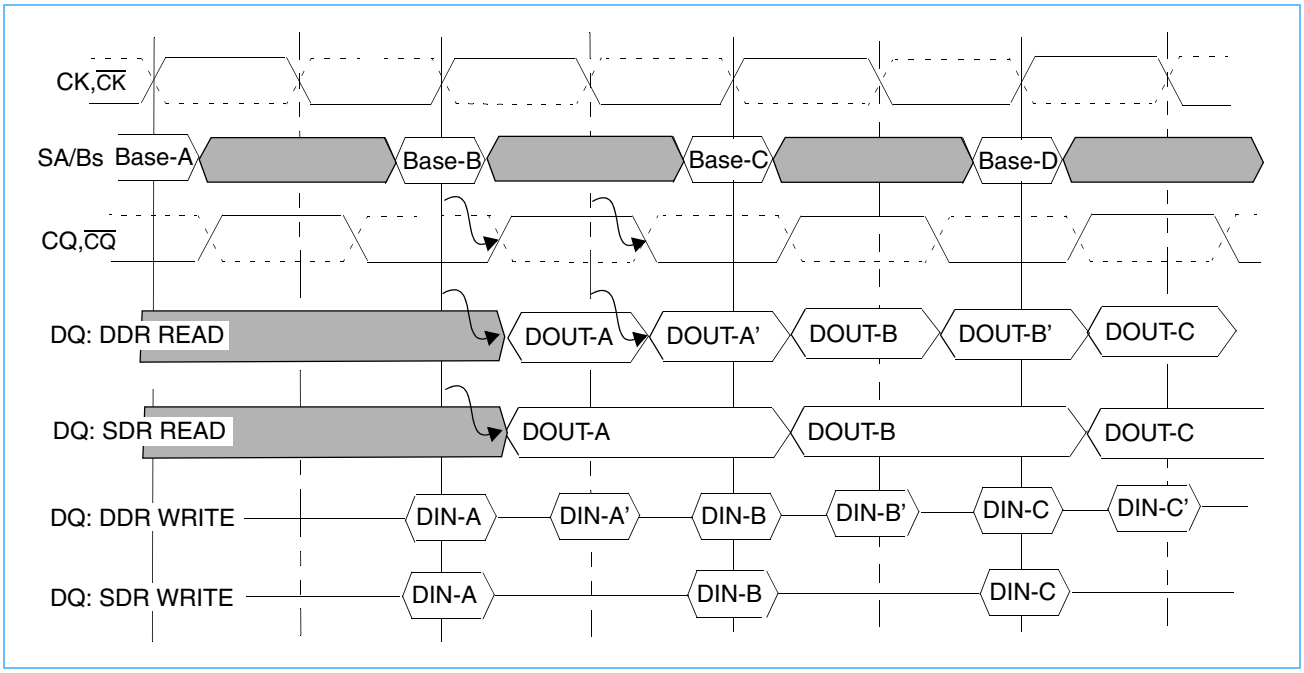
Late Write

The late-write function allows write data to be registered one cycle after addresses and controls. This feature eliminates one of two bus-turnaround cycles normally required when going from a read to a write operation. Late write is accomplished by buffering write addresses and data. The SRAM array update occurs during the third write cycle. Read-cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. Full data coherency is maintained for both DDR and SDR operations. As a result, NOP (write buffer flush) operations are not required going from write cycles to read cycles.

Echo Clocks

Echo clocks CQ and $\overline{CQ}$ are generated from rising and falling edges of the CK clock, with access times representative of the data-outs. Echo clocks keep running during write and NOP operations. Echo-clock operation is identical for both double-data-rate and single-data-rate operations. The close tracking of echo clocks and data-out timings allows the echo clocks to be used as capture clocks for the data-outs by the receiving device.

Timing Diagram: Double Data Rate and Single Data Rate Modes



Programmable Impedance and Power-Up Requirements

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary because the impedance is affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles, and each evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver has 64 discrete binary weighted steps. Impedance updates for zeros occur whenever the SRAM is driving ones for the same DQs; impedance updates for ones occur whenever SRAM is driving zeros for the same DQs. Updates of both zeros and ones occur when the SRAM is High-Z. Furthermore, to guarantee the output driver impedance, the SRAM requires 2048 clock cycles and a Read '0' and Read '1' or a Read '1' and a Read '0' across all used outputs. The RC time constant of the loaded RQ trace must be less than 3ns.

Power-Up and Power-Down Sequences

The power supplies need to be powered up in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by inputs. The power-down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}.

Initial Writes

DQ and CQ timings will not be guaranteed until at least two write cycles are performed. These cycles can be part of the programmable impedance initial cycles.

Function Control

The function control is dependent on the state of the three function control pins (B1, B2, and B3), captured when CK transitions from low to high as described in the following table ("n" refers to the current cycle and "n-1" refers to the previous SRAM cycle).

B1 (n-1)	B2 (n-1)	B3 (n-1)	B1 (n)	B2 (n)	B3 (n)	Function (n)
X	X	X	0	0	0	Load New Address, Double Data Rate (DDR) Write
X	X	X	0	0	1	Load New Address, Single Data Rate (SDR) Write
X	X	X	0	1	0	Load New Address, DDR Read
X	X	X	0	1	1	Load New Address, SDR Read
0	0	0	1	1	X	Continue Burst, DDR Write
0	0	1	1	1	X	Continue Burst, SDR Write
0	1	0	1	1	X	Continue Burst, DDR Read
0	1	1	1	1	X	Continue Burst, SDR Read
X	X	X	1	0	X	NOP (High-Z cycle n+1)
1	0	X	1	X	X	NOP (High-Z cycle n+2)

Burst Order Definition

The DC state of the $\overline{LBO}$ pin determines the burst order of the addresses, given the starting address in a Load operation (B1 = 0). The following table defines the order of addresses for the two different states of $\overline{LBO}$.

Address Sequence when $\overline{LBO}$ = V_{DD} (Interleave Burst)

	SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Starting address	0	0	0	1	1	0	1	1
Second address	0	1	0	0	1	1	1	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	1	0	0	1	0	0

Address Sequence when $\overline{LBO}$ = V_{SS} (Linear Burst)

	SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Starting address	0	0	0	1	1	0	1	1
Second address	0	1	1	0	1	1	0	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	0	0	0	1	1	0

Clock Truth Table

CK	B1 (n)	B2 (n)	B3 (n)	DQ (n)	DQ (n + 1)	DQ (n + 1.5)	MODE
L→H	L	H	H	X	D_{out} 0-35	Previous Data Held	Read Cycle SDR
L→H	L	H	L	X	D_{out} 0-35a	D_{out} 0-35b	Read Cycle DDR
L→H	L	L	H	X	D_{IN} 0-35	X	Write Cycle SDR
L→H	L	L	L	X	D_{IN} 0-35a	D_{IN} 0-35b	Write Cycle DDR
L→H	H	L	X	X	High-Z	High-Z	NOP (Deselect) Cycle
L→H	H	H	X				Continue Burst Operation

Output Enable Truth Table

Operation (n, n + 1)	$\overline{G}$ (n)	$\overline{G}$ (n + 1)	DQ (n)	DQ (n + 1)
Read	L	L	X	D_{OUT} 0-35
Read	H	H	High-Z	High-Z
Write	L	L	X	High-Z
NOP	L	L	X	High-Z

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-0.5 to 2.825	V	1
V_{DDQ}	Power Supply Voltage	-0.5 to 2.825	V	1
V_{IN}	Input Voltage	-0.5 to 2.825	V	1
V_{OUT}	Output Voltage	-0.5 to 2.825	V	1
T_J	Operating Temperature	0 to +110	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
I_{OUT}	Short Circuit Output Current	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Supply Voltage	2.5V - 5%	2.5	2.5V + 5%	V	1
V_{DDQ}	Output Driver Supply Voltage	1.4	1.8	1.9	V	1
V_{IH}	Input High Voltage	V_{REF} +0.1		V_{DDQ} + 0.3	V	1, 2
V_{IL}	Input Low Voltage	-0.3		V_{REF} - 0.1	V	1, 3
V_{REF}	Input Reference Voltage	0.68	.9	1.0	V	1, 6
$V_{IN - CLK}$	Clocks Signal Voltage	-0.3		V_{DDQ} + 0.3	V	1, 4
$V_{DIF - CLK}$	Differential Clocks Signal Voltage	0.1		V_{DDQ} + 0.6	V	1, 5
$V_{CM - CLK}$	Clocks Common Mode Voltage	0.55		1.0	V	1

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3V, V_{IH}(Max) AC = V_{DDQ} +0.85 (pulse width ≤ 2ns).
3. V_{IL}(Min)DC = -0.3 V, V_{IL}(Min)AC = -1.5V (pulse width ≤ 2ns).
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (CK, $\overline{CK}$).
5. $V_{DIF-CLK}$ specifies the minimum clock differential voltage required for switching.
6. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%) (Page 1 of 2)

Symbol	Parameter			Min.	Max.	Units	Notes
I_{DD}	Average Power Supply Operating Current (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL})	x36	-22		800	mA	1
			-24		750		
			-27		700		
			-30		640		
		x18	-22		625	mA	1
			-24		540		
			-27		515		
			-30		470		
I_{SB}	Power Supply Standby Current ($\overline{SS}$ = VIH. All other inputs = V_{IH} or V_{IL}. I_{OUT} = 0)				200	mA	1
I_{LI}	Input Leakage Current, any input (V_{IN} = V_{SS} or V_{DDQ})			-2	+2	µA	
I_{LO}	Output Leakage Current (V_{OUT} = V_{SS} or V_{DDQ}, DQ in High-Z)			-5	+5	µA	

1. I_{OUT} = Chip Output Current.
2. Minimum Impedance Output Driver.
3. For JTAG inputs only.
4. JTAG output current leakage is not provided since it is not driven; it is an output only.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%) (Page 2 of 2)

Symbol	Parameter			Min.	Max.	Units	Notes
V_{OH}	Output High Level Voltage (I_{OH} = -6mA)			V_{DDQ} -0.4	V_{DDQ}	V	2
V_{OL}	Output Low Level Voltage (I_{OL} = +6mA)			V_{SS}	V_{SS} +0.4	V	2
I_{LIJTAG}	JTAG Leakage Input Current (V_{IN} = V_{SS} or V_{DD})			-70	+10	µA	3
I_{LOJTAG}	JTAG Leakage Output Current						4

1. I_{OUT} = Chip Output Current.
2. Minimum Impedance Output Driver.
3. For JTAG inputs only.
4. JTAG output current leakage is not provided since it is not driven; it is an output only.

Programmable Impedance Output Driver DC Electrical Characteristics

(T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OH}	Output High Voltage	V_{DDQ} / 2	V_{DDQ}	V	1, 3
V_{OL}	Output Low Voltage	V_{SS}	V_{DDQ}/2	V	2, 3

1. I_{OH} = (V_{DDQ} / 2) / (RQ / 5) ± 15% @ V_{OH} = V_{DDQ} / 2 (for: 175Ω ≤ RQ ≤ 350Ω).
2. I_{OL} = (V_{DDQ} / 2) / (RQ / 5) ± 15% @ V_{OL} = V_{DDQ} / 2 (for: 175Ω ≤ RQ ≤ 350Ω).
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.8 V.

PBGA Thermal Characteristics

Symbol	Parameter	Rating	Units
RΘJC	Thermal Resistance Junction to Case	1	°C/W

Capacitance (T_A = 0 to +85°C, V_{DD} = 2.5V ±5%, f = 1MHz)

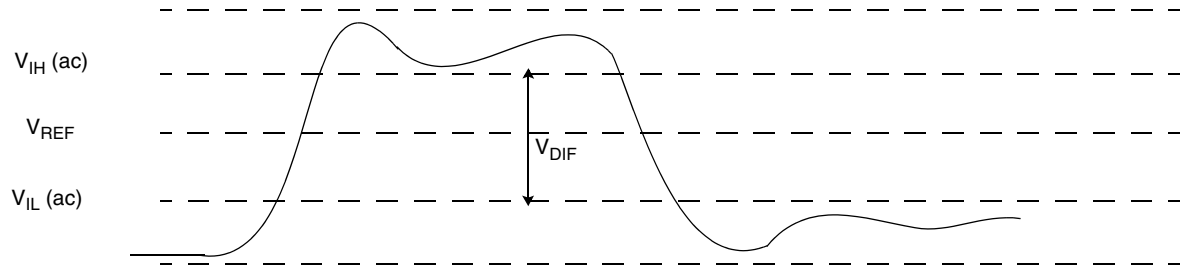
Symbol	Parameter	Test Condition	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_{OUT}	Data I/O Capacitance (DQ0–DQ35)	V_{OUT} = 0V	5	pF

AC Input Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%)

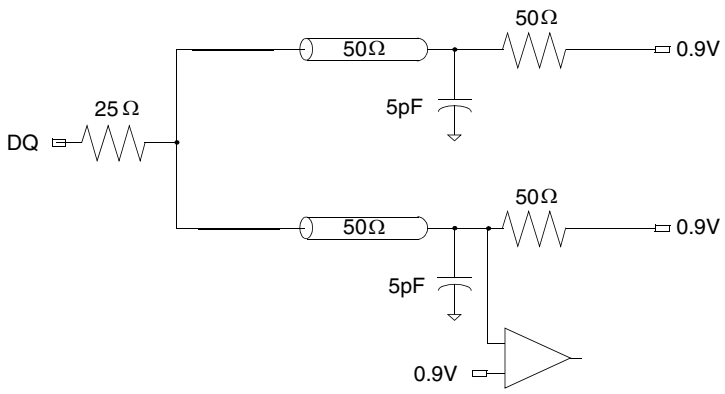
Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (ac)	AC Input Logic High	V_{REF} + 400		mV	3, 4
V_{IL} (ac)	AC Input Logic Low		V_{REF} - 400	mV	3, 4
V_{DIF} (ac)	Clock Input Differential Voltage	800		mV	2, 3
V_{REF} (ac)	V_{REF} Peak-to-Peak AC Voltage		5% V_{REF} (dc)	mV	1

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{DIF}).
3. To guarantee AC characteristics; V_{IH}, V_{IL}, T_{rise}, and T_{fall} of the inputs and clocks must be within 20% of each other. If these conditions are not met then:
   - Setup time is measured from clock crossing to inputs at their switched V_{IHAC}, V_{ILAC} levels.
   - Hold time is measured from clock crossing to inputs switching out of their valid V_{IHAC}, V_{ILAC} levels.
4. See *AC Test Loading* on page 12.

AC Input Definition



AC Test Loading



AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%, V_{DDQ} = 1.8V)

Symbol	Parameter	Conditions	Units	Notes
V_{IH}	Input High Level	1.5	V	2
V_{IL}	Input Low Level	0.3	V	2
V_{REF}	Input Reference Voltage	0.9	V	2
$V_{DIF-CLK}$	Differential Clocks Voltage	1.2	V	2
V_{CM-CLK}	Clocks Common Mode Voltage	0.9	V	2
T_R	Input Rise Time	0.5	ns	2
T_F	Input Fall Time	0.5	ns	2
	I/O Signals Reference Level (except CK clocks)	0.9	V	2
	Clocks Reference Level	Differential Cross Point	V	2
	Output Load Conditions			1

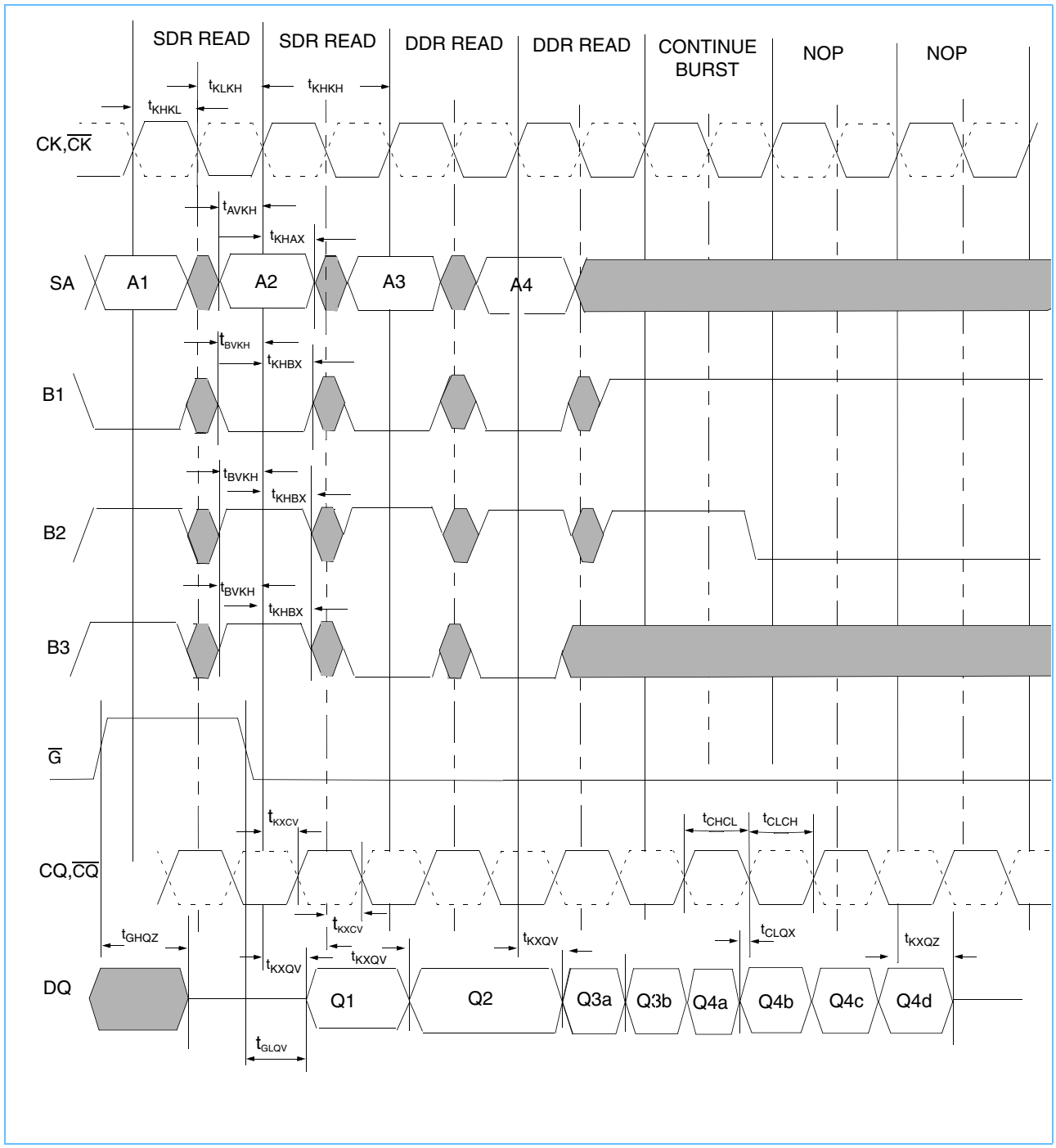
1. See *AC Test Loading* on page 12.
2. Due to tester limitations and applied guardbands, the part is tested to AC test conditions and not worst-case specification conditions. For application robustness, it is recommended that at a minimum AC test conditions are applied.

AC Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5 V +10/– 5%)

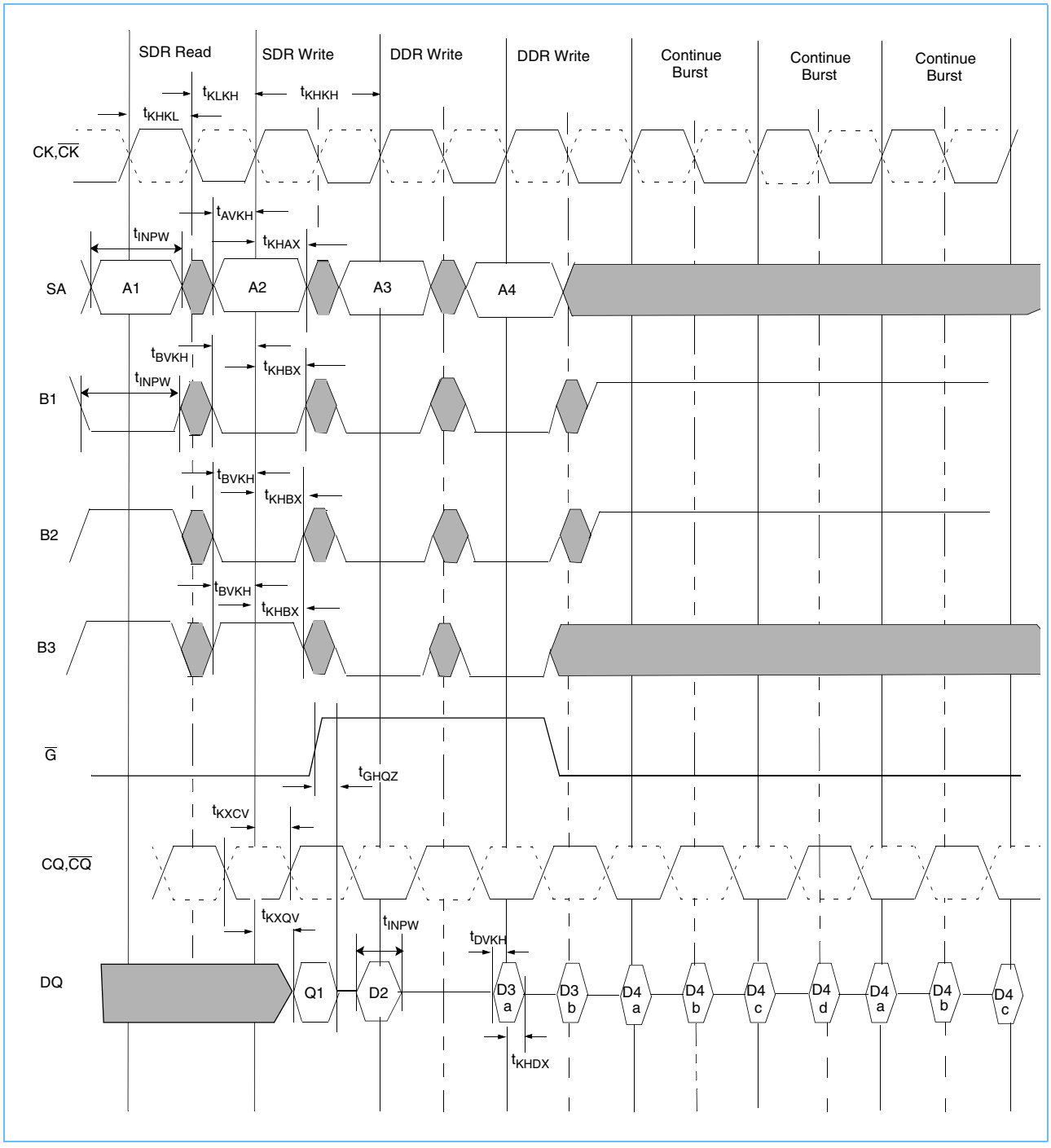
Symbol	Parameter	-22		-24		-27		-30		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	2.2		2.4		2.7		3.0		ns	
t_{KHKL}	Clock High Pulse Width	1.0		1.0		1.3		1.4		ns	
t_{KLKH}	Clock Low Pulse Width	1.0		1.0		1.3		1.4		ns	
t_{AVKH}	Address Setup Time	0.25		0.25		0.3		0.3		ns	1, 8, 5, 7
t_{KHAX}	Address Hold Time	0.25		0.25		0.3		0.3		ns	1, 8, 5, 7
t_{BVKH}	Function Control (B1, B2, B3) Setup Time	0.25		0.25		0.3		0.3		ns	1, 8, 5, 7
t_{KHBX}	Function Control (B1, B2, B3) Hold Time	0.25		0.25		0.3		0.3		ns	1, 8, 5, 7
t_{DVKH}	Data In Setup Time	0.21		0.21		0.25		0.25		ns	1, 8, 5, 7
t_{KHDX}	Data In Hold Time	0.21		0.21		0.25		0.25		ns	1, 8, 5, 7
t_{INPW}	Input Pulse Width	0.8		0.8		1.0		1.0			6
t_{CHCL}	Echo Clock (CQ) High Pulse Width	t_{KHKL}- 0.1	t_{KHKL}+ 0.1	t_{KHKL}- 0.1	t_{KHKL}+ 0.1	t_{KHKL}- 0.1	t_{KHKL}+ 0.1	t_{KHKL}- 0.1	t_{KHKL}+ 0.1	ns	1, 2, 5
t_{CLCH}	Echo Clock (CQ) Low Pulse Width	t_{KLKH}- 0.1	t_{KLKH}+ 0.1	t_{KLKH}- 0.1	t_{KLKH}+ 0.1	t_{KLKH}- 0.1	t_{KLKH}+ 0.1	t_{KLKH}- 0.1	t_{KLKH}+ 0.1	ns	1, 2 5
t_{KXCV}	Clock (CK) crossing to Echo Clock (CQ) Valid	0.8	2.1	0.8	2.1	0.8	2.0	0.8	1.7	ns	1, 3, 5
t_{KXQV}	Clock (CK) crossing to Output Valid	0.8	2.1	0.8	2.1	0.8	2.0	0.8	1.7	ns	1, 5
t_{KXQZ}	Clock (CK) crossing to Output High-Z	0.8	2.1	0.8	2.1	0.8	2.0	0.8	1.7	ns	1, 5
t_{KXQLZ}	Clock (CK) crossing to Output Active	0.8	2.1	0.8	2.1	0.8	2.0	0.8	1.7	ns	1, 5
t_{QVTRK}	Echo Clock (CQ) Valid to Output Valid Tracking (t_{KXCV} - t_{KXQV})	-0.15	0.15	-0.15	0.15	-0.15	0.15	-0.2	0.2	ns	1, 2, 4, 5
t_{QZTRK}	Echo Clock (CQ) Valid to Output High-Z Tracking (t_{KXCV} - t_{KXQZ})	-0.15	0.15	-0.15	0.15	-0.15	0.15	-0.2	0.2	ns	1, 2, 4, 5
t_{QLZTRK}	Echo Clock (CQ) Valid to Output Active Tracking (t_{KXCV} - t_{KXQLZ})	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	ns	1, 2, 4, 5
t_{GHQZ}	Output Enable ($\overline{G}$) High to High-Z	0.3	1.7	0.3	1.7	0.3	1.7	0.3	2.0	ns	2
t_{GLQV}	Output Enable ($\overline{G}$) Low to Output Valid	0.3	1.7	0.3	1.7	0.3	1.7	0.3	2.0	ns	2

1. See *AC Test Loading* on page 12.
2. These parameters may not be tested at the values shown in this table, and may only be guaranteed by design.
3. Echo Clock (CQ) Valid refers to CQ and $\overline{CQ}$ rising and falling edges.
4. The tracking between echo-clock access times and DQ access times is across all cycle boundaries for any given SRAM address and function pattern.
5. CK and $\overline{CK}$ clocks must be used differentially in order to meet specification.
6. Inputs to switch a maximum of once per applied cycle. For example, Data equals (T_{KHKH})/2; Address and Controls equal T_{KHKH}.
7. To guarantee AC characteristics; V_{IH}, V_{IL}, T_{rise}, and T_{fall} of inputs and clocks must be within 20% of each other. If these conditions are not met then:
   - Setup time is measured from clock crossing to inputs at their switched V_{IHAC}, V_{ILAC} levels.
   - Hold time is measured from clock crossing to inputs switching out of their valid V_{IHAC}, V_{ILAC} levels.
8. Guaranteed by design and tested without guardband.

Timing Diagram (Read and NOP Cycles)



Timing Diagram (Read, Write Cycles)



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from the I/O pins to the RAM core.

In conformance with IEEE standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power up; therefore, a TRST signal is not required.

Signal List:

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG Recommended DC Operating Conditions (T_A = 0 to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH1}	JTAG Input High Voltage	1.7	—	2.8	V	
V_{IL1}	JTAG Input Low Voltage	-0.3	—	0.8	V	
V_{OH1}	JTAG Output High Level	2.1	—	—	V	2
V_{OL1}	JTAG Output Low Level	—	—	0.2	V	1

1. $_{OH1}$ = -2mA at 2.1V.
2. $_{OL1}$ = +2mA at 0.2V.

JTAG AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%)

Symbol	Parameter	Conditions	Units	Notes
V_{IH1}	Input Pulse High Level	2.0	V	
V_{IL1}	Input Pulse Low Level	0.0	V	
T_{R1}	Input Rise Time	2.0	ns	
T_{F1}	Input Fall Time	2.0	ns	
	Input and Output Timing Reference Level	1.0	V	1

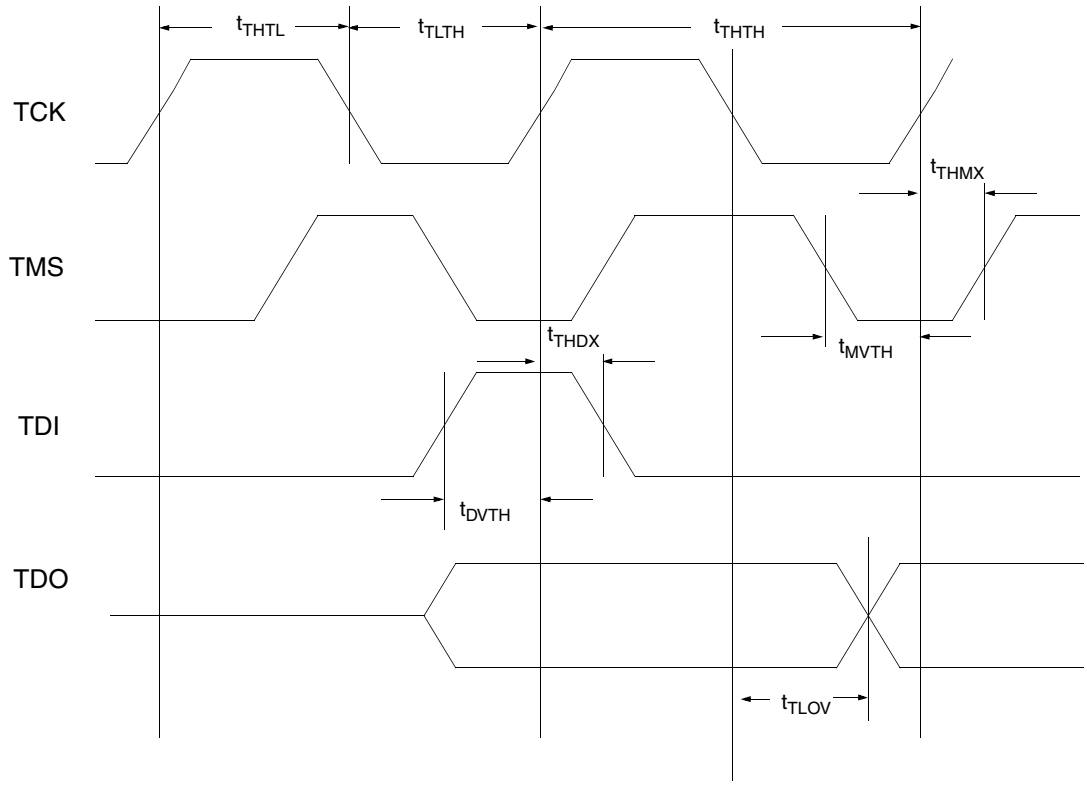
1. See *AC Test Loading* on page 12.

JTAG AC Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{THTH}	TCK Cycle Time	20		ns	
t_{THTL}	TCK High Pulse Width	7		ns	
t_{TLTH}	TCK Low Pulse Width	7		ns	
t_{MVTH}	TMS Setup	4		ns	
t_{THMX}	TMS Hold	4		ns	
t_{DVTH}	TDI Setup	4		ns	
t_{THDX}	TDI Hold	4		ns	
t_{TLOV}	TCK Low to Valid Data		7	ns	1

1. See *AC Test Loading* on page 12.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan[1, 2]	49	68

1. The boundary-scan chain consists of the following bits:
   - 36 or 18 bits for data inputs depending on x36 or x18 configuration
   - 19 bits for SA0–SA18 for x36; 20 bits for SA0–SA19 for x18
   - 4 or 2 bits for CQ and $\overline{CQ}$ clocks depending on x36 or x18 configuration
   - 9 bits for CK, $\overline{CK}$, ZQ, $\overline{LBO}$, B1, B2, B3, MODE and $\overline{G}$
2. CK and $\overline{CK}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for boundary-scan sampling. CQ and $\overline{CQ}$ clocks are sampled from the CK and $\overline{CK}$ boundary-scan register inputs.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28) IBM Internal Use	Device Density and Configuration (27:19)	Vendor Definition (18:12)	Manufacture JEDEC Code (11:1)	Start Bit(0)
1M x 18	XXXX	011100001	0110011	00010100100	1
512K x 36	XXXX	011011110	0110011	00010100100	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	1
010	SAMPLE-Z	1
011	PRIVATE	4
100	SAMPLE	3
101	PRIVATE	4
110	PRIVATE	4
111	BYPASS	2

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. BYPASS register is initialized to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially-loaded TDI when exiting the Shift DR state.
3. SAMPLE instruction does not place DQs in High-Z.
4. PRIVATE is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

This part has not been designed to comply with the following sections of IEEE 1149.1:

- 7.2.1.b, e
- 7.7.1.a–f
- 10.1.1.b, e
- 10.7.1.a–d

Boundary Scan Order (x36)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	SA1	5R	24	CQ	8F	47	CQ	2F
2	SA0	5T	25	DQ11	9D	48	DQ25	1F
3	SA2	6R	26	DQ17	7F	49	DQ19	3H
4	SA3	7T	27	DQ14	8D	50	DQ22	2H
5	SA4	7P	28	DQ12	9B	51	DQ26	1H
6	DQ2	8T	29	DQ15	8B	52	ZQ	5A
7	DQ5	9T	30	SA5	7D	53	B1	5B
8	DQ3	8P	31	SA6	7C	54	B2	5K
9	DQ0	7M	32	SA7	7B	55	B3	5L
10	DQ6	9P	33	SA8	7A	56	$\overline{LBO}$	4L
11	$\overline{CQ}$	8M	34	SA9	6C	57	DQ27	1K
12	DQ7	9M	35	SA10	6A	58	DQ31	2K
13	DQ1	7K	36	SA11	4A	59	DQ34	3K
14	DQ4	8K	37	SA12	4C	60	DQ28	1M
15	DQ8	9K	38	SA13	3A	61	$\overline{CQ}$	2M
16	MODE[1]	6L	39	SA14	3B	62	DQ29	1P
17	$\overline{CK}$	5H	40	SA15	3C	63	DQ35	3M
18	CK	5G	41	SA18	3D	64	DQ32	2P
19	$\overline{G}$	5C	42	DQ20	2B	65	DQ30	1T
20	DQ9	9H	43	DQ23	1B	66	DQ33	2T
21	DQ13	8H	44	DQ21	2D	67	SA16	3T
22	DQ16	7H	45	DQ18	3F	68	SA17	4R
23	DQ10	9F	46	DQ24	1D			

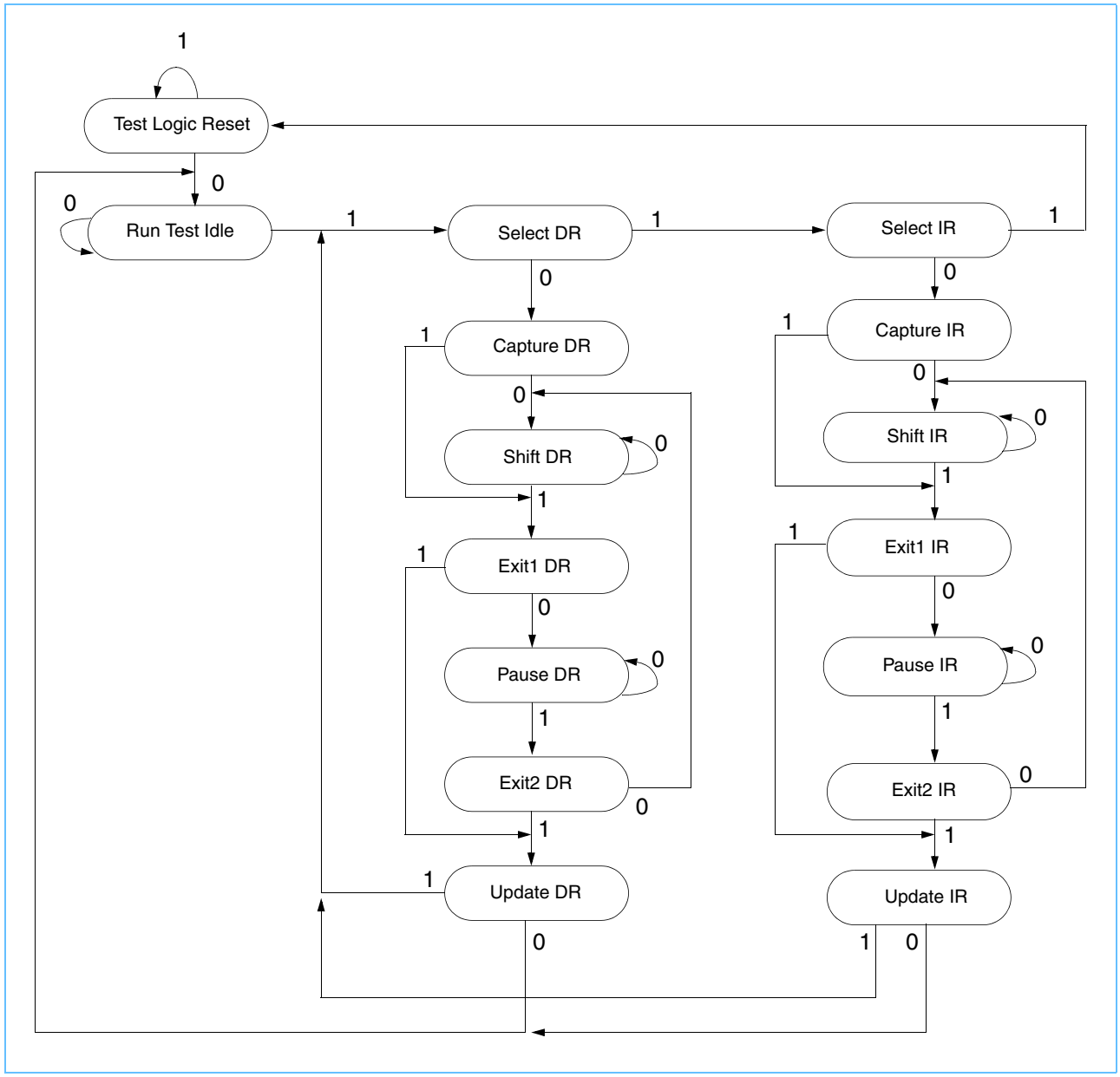
1. Mode will scan out the value placed on the Mode pin, or if the Mode pin is floated, Mode will scan V_{SS}.

Boundary Scan Order (x18)

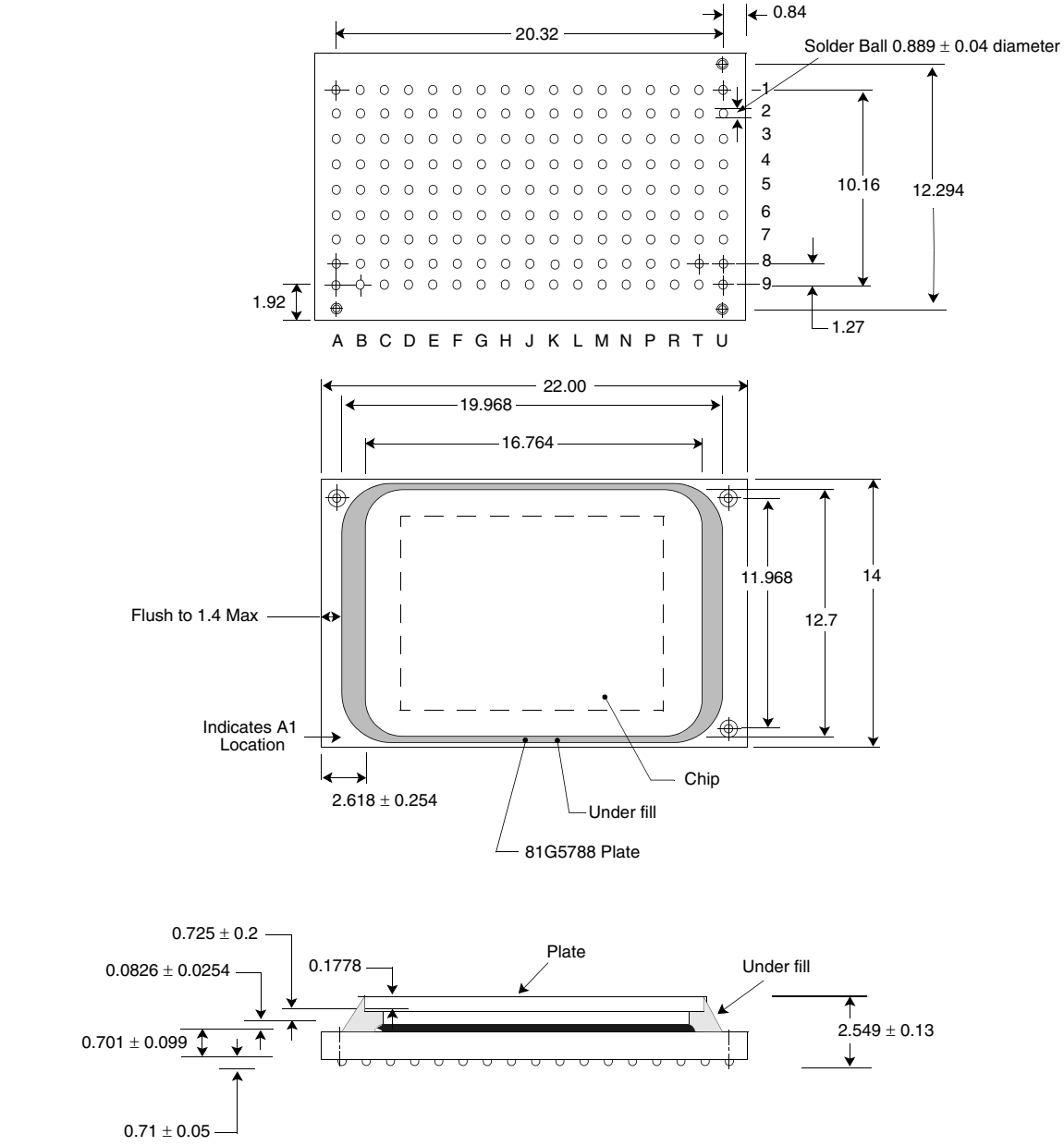
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	SA1	5R	26	SA11	4A
2	SA0	5T	27	SA12	4C
3	SA2	6R	28	SA13	3A
4	SA3	7T	29	SA14	3B
5	SA4	7P	30	SA15	3C
6	DQ1	8T	31	SA18	3D
7	DQ2	9P	32	DQ10	2B
8	$\overline{CQ}$	8M	33	DQ11	1D
9	DQ0	7K	34	CQ	2F
10	DQ3	9K	35	DQ9	3H
11	MODE[1]	6L	36	DQ12	1H
12	$\overline{CK}$	5H	37	ZQ	5A
13	CK	5G	38	B1	5B
14	$\overline{G}$	5C	39	B2	5K
15	DQ6	8H	40	B3	5L
16	DQ4	9F	41	$\overline{LBO}$	4L
17	DQ8	7F	42	DQ15	2K
18	DQ7	8D	43	DQ13	1M
19	DQ5	9B	44	DQ17	3M
20	SA5	7D	45	DQ16	2P
21	SA6	7C	46	DQ14	1T
22	SA7	7B	47	SA19	3P
23	SA8	7A	48	SA16	3T
24	SA9	6C	49	SA17	4R
25	SA10	6A			

1. Mode will scan out the value placed on the Mode pin, or if the Mode pin is floated, Mode will scan V_{SS}.

TAP Controller State Machine



9 x 17 BGA Dimensions



Note: All dimensions are in millimeters.

Revision Log

Rev	Contents of Modification
June 3, 2002	Initial release (00).

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction,
NY 12533-6351

The IBM home page can be found at http://www.ibm.com

The IBM Microelectronics Division home page can be found at http://www.chips.ibm.com

June 3, 2002