*Multi*GEN™ GF9103 Over-Sampling Color Space Converter for Video Monitoring

DATA SHEET

GF9103

NOT RECOMMENDED FOR NEW DESIGNS

FEATURES

- **4:2:2 to over-sampled RGB or YC_BC_R conversion in a single device**
- **single 10 bit 4:2:2 input**
- **internal 4:2:2 de-multiplexer**
- **4:2:2 to 8:8:8 interpolation filters**
- **internal YC_BCR to RG_B color space conversion**
- **optional YC_BC_R (8:8:8) output mode**
- **setup insertion in Luminance channel under user control**
- **user selectable digital SIN X/X correction**
- **rounding to 10/8 bit resolution per output channel**
- **40 MHz maximum clock rate**
- **single +5 V power supply**

APPLICATIONS

- Over-Sampling 4:2:2 to Analog RGB Conversions for video monitoring
- Over-Sampling 4:2:2 to Analog YCBCR Conversions for video monitoring

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
GF9103-CPS	68 pin PLCC	0° to 70° C
GF9103-CTS	68 pin PLCC Tape	0° to 70° C

DEVICE DESCRIPTION

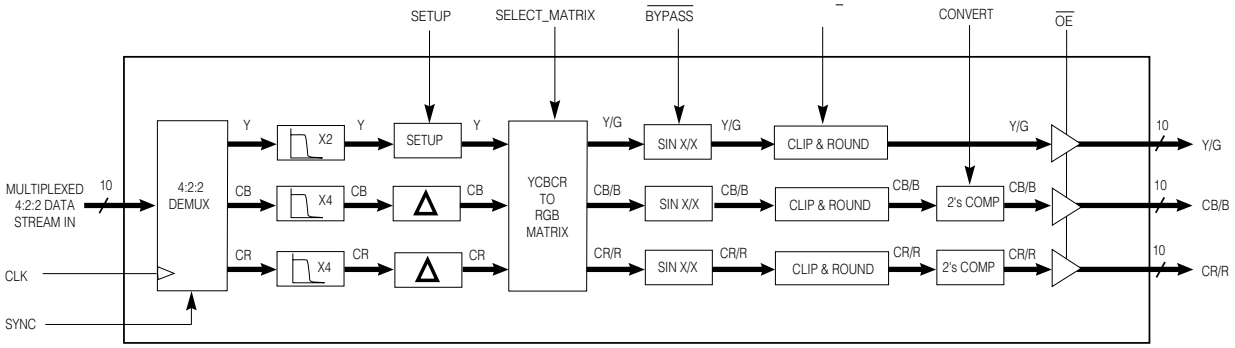
The GF9103 is specifically designed to simplify conversions from 4:2:2 component digital video to analog RGB or analog YC_BC_R component video. The GF9103 simplifies this process by performing 4:2:2 to 8:8:8 interpolation, digital color space conversion and digital SIN X/X correction in a single device. Immediately following the GF9103, three over-sampled channels of RGB or YC_BC_R data may be passed through Digital to Analog converters and simplified analog reconstruction filters.

The GF9103 accepts a single 10 bit stream of 4:2:2 data and internally de-multiplexes it into three 10 bit channels of YC_BC_R data. The YC_BC_R data is then passed through three linear phase FIR filters that over-sample the Y data by a factor of 2 and the C_B and C_R data by a factor of 4.

While operating in an over-sampled RGB output mode, the interpolated YC_BC_R data is passed through the internal color space converter to convert the YC_BC_R data to RGB data according to CCIR-601. Alternatively, the color space converter may be bypassed to obtain over-sampled YC_BC_R (8:8:8) output data. While operating in YC_BC_R output mode, setup may be dynamically inserted into the Luminance channel.

Prior to output rounding, over-sampled YC_BC_R or RGB data may be corrected for SIN X/X characteristics of D/A conversion. Output data may be rounded to 10 or 8 bit resolution per channel. C_B and C_R may be presented as signed or unsigned data.

The GF9103 is packaged in a 68 pin PLCC package, operates with a single +5 V power supply and typically consumes only 85 mA of current when operated at 27 MHz.



FUNCTIONAL BLOCK DIAGRAM

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PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
10, 18, 27, 36, 44, 52, 61, 68	V_{DD}	±5 V ± 5% power supply.
1, 6, 7, 9, 26, 30, 35, 40, 43, 60, 64	GND	Ground.
3	SCAN_EN	Set Low.
8, 11-17, 19, 20	$SI_{9..0}$	Input Data Port: Input data port with internal pull-downs. Input data is assumed to be a multiplexed stream of C_BYC_R [Y] C_B..., where [Y] denotes an isolated Luminance sample. SI_9 is the Most Significant Bit and SI_0 is the Least Significant Bit.
4	$\overline{OE}$	Output Enable: Active low input with internal pull-up. When $\overline{OE}$ is high, the output data ports are in high impedance state.
59-53, 51-49	$SOA_{9..0}$	Output Data Port A: Depending on device configuration, $SOA_{9..0}$ may output over-sampled Y or G video. SOA_9 is the Most Significant Bit and SOA_0 is the Least Significant Bit.
48-45, 42, 41, 39-37, 34	$SOB_{9..0}$	Output Data Port B: Depending on device configuration, $SOB_{9..0}$ may output over-sampled C_B or B video. SOB_9 is the Most Significant Bit and SOB_0 is the Least Significant Bit.
33-31, 29, 28, 25-21	$SOC_{9..0}$	Output Data Port C: Depending on device configuration, $SOC_{9..0}$ may output over-sampled C_R or R video. SOC_9 is the Most Significant Bit and SOC_0 is the Least Significant Bit.
2	CLK	System Clock: All timing information relative to rising edge of clock.
5	SYNC	Synchronization: Control signal input with internal pull-up. This input is used to synchronize the incoming data by holding SYNC high on clock period N and low on clock period N+1 when the first C_B sample is presented to the $SI_{9..0}$ inputs. SYNC may be held low until re-synchronization is desired or may be toggled at every occurrence of a C_B sample.
65	SELECT_MATRIX	Select Color Space Conversion: Control signal input with internal pull-down. SELECT_MATRIX is used to enable and disable the internal YC_BC_R to RGB color space converter. Color space conversion is enabled while SELECT_MATRIX is high and is disabled while SELECT_MATRIX is low.
66	$\overline{BYPASS}$	Bypass SIN X/X Correction: Control signal input with internal pull-up. When $\overline{BYPASS}$ is high, SIN X/X correction for the three output channels is enabled. While $\overline{BYPASS}$ is low, SIN X/X correction is by-passed.
63	SETUP	Setup: Control signal input with internal pull-down. SETUP is used to enable and disable setup insertion in the Luminance channel.
62	CONVERT	Two's Complement Conversion: Control signal input with internal pull-up. While CONVERT is high, $SOB_{9..0}$ and $SOC_{9..0}$ output signed (two's complement) digital data. While CONVERT is low, $SOB_{9..0}$ and $SOC_{9..0}$ output unsigned (offset binary) data. When operating in RGB output mode, the CONVERT pin is over-ridden and both $SOB_{9..0}$ and $SOC_{9..0}$ output unsigned digital data. $SOA_{9..0}$ outputs unsigned digital data in all operating modes.
67	RND10/$\overline{8}$	Output Rounding: Control signal input with internal pull-up. RND10/$\overline{8}$ selects rounding to 10 bit resolution per channel when high and rounding to 8 bit resolution per channel when low.

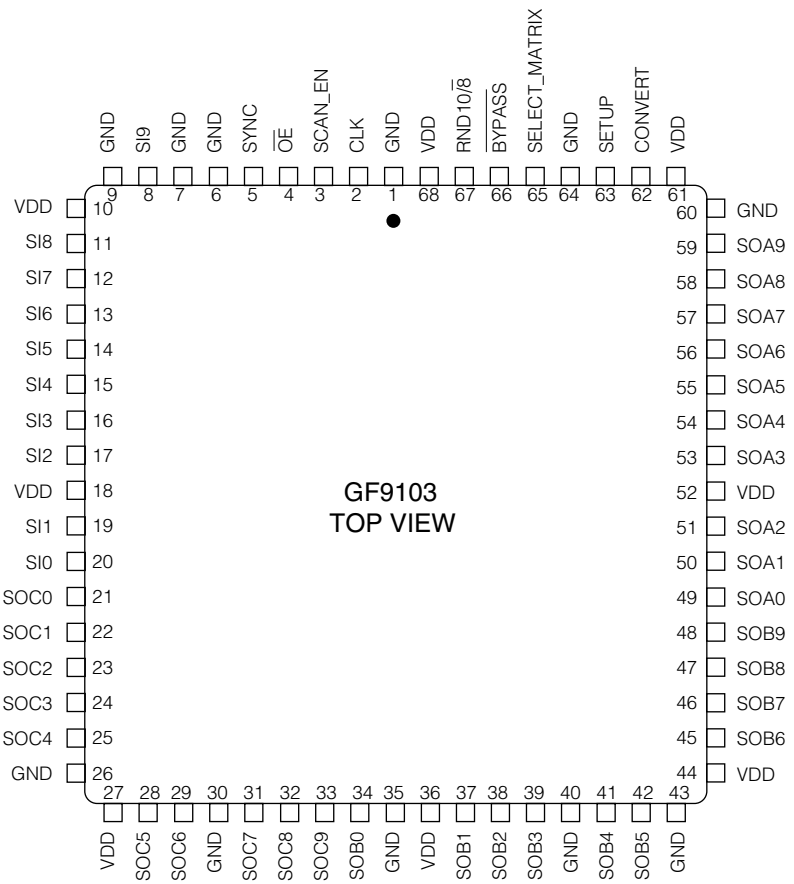

Fig. 1 GF9103 Pin Connections

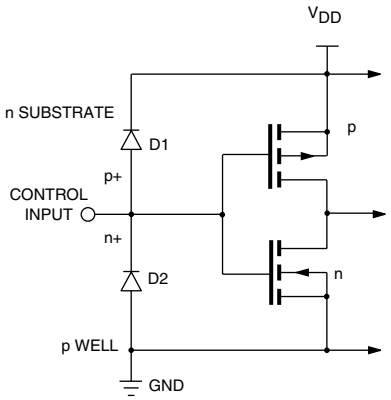

Fig. 2a Equivalent Input Circuit

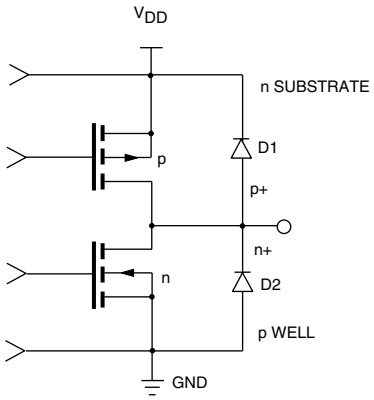

Fig. 2b Equivalent Output Circuit

DEVICE DESCRIPTION

The GF9103 is composed of five main sections:

1. 4:2:2 De-Multiplexer
2. FIR Filtering and Setup Insertion
3. Color Space Conversion
4. Digital SIN X/X Correction
5. Output Processing

4:2:2 DE-MULTIPLEXER

The de-multiplexer accepts data multiplexed in a SMPTE 125M compliant format from the $SI_{9..0}$ input data port. SI_9 is the Most Significant Bit and SI_0 is the Least Significant Bit. The input data stream is assumed to be a multiplexed stream of C_B Y C_R [Y] C_B..., where the three words C_B Y C_R refer to cosited samples and where [Y] refers to an isolated Luminance sample. When operating the GF9103 with 8 bit input data, $SI_{9..2}$ should be used to present data to the device and $SI_{1..0}$ should be set low.

At least once during a power cycle, the GF9103 must be synchronized to the incoming data stream. The GF9103 is synchronized by holding SYNC high on clock period N and low on clock period N+1 when the first C_B sample is presented to the $SI_{9..0}$ inputs. SYNC may be held low until re-synchronization is desired, or it may be toggled at every occurrence of a C_B sample. Refer to the timing diagram in Figure 9 for required operation of the SYNC control signal.

The internal de-multiplexer will de-multiplex all data in the input data stream including any ancillary, EDH,VITC, and EAV/SAV ... signals that may be present. Since this data is passed directly to the interpolation filters in the same way that active video would be, it is recommended that such data be replaced with appropriate blanking levels prior to entering the GF9103.

The output of the 4:2:2 de-multiplexer consists of three 10 bit channels of YC_BC_R data. All three channels are then fed to their respective interpolation filter.

INTERPOLATION FILTERS

Within the interpolation stage, the Luminance data is over-sampled by a factor of two and the C_B and C_R data is over-sampled by a factor of four so that the 4:2:2 data is converted to 8:8:8 data. By over-sampling the 4:2:2 data to 8:8:8 data, the size, cost and complexity of the analog reconstruction filters following Digital to Analog converters are reduced.

The Luminance data is over-sampled by a linear phase FIR filter providing 0.0 dB DC gain, +0.038/-0.025 pass- band ripple [0.0 fs to 0.21 fs], 6 dB attenuation at $fs/4$, and 47 dB stopband attenuation [0.30 fs to 0.50 fs]. Figure 3 and Figure 4 present the frequency response of the Luminance interpolation filter.

The C_B and C_R data is over-sampled by a linear phase FIR filter providing 0.0 dB DC gain, passband ripple of +0.2 dB/-0.2 dB [0.0 to 0.07 fs], 6 dB attenuation at $fs/8$ and a stopband attenuation of 28 dB [0.17fs to 0.50 fs].

Figure 5 and Figure 6 present the frequency response of the C_B and C_R interpolation filters.

Following the interpolation process, a DC offset may be introduced into the Luminance channel. Setup insertion is enabled and disabled by the SETUP control signal. While SETUP is high, the Luminance data is scaled by a factor of +947/1024 and an offset of +71 (decimal) is added. While SETUP is low, no scaling or offset is applied and the data passes through the stage unmodified. The timing diagram in Figure 10 demonstrates the operation of the SETUP control signal.

COLOR SPACE CONVERSION

Two operating modes exist for the color space converter section. These two modes are controlled by the SELECT_MATRIX control signal. While SELECT_MATRIX is low, the de-matrixing 3 x 3 multiplier is bypassed so that over-sampled Y C_B C_R data is passed through the stage unmodified. While SELECT_MATRIX is high, the 3 x 3 multiplier implements the following color space conversion:

$$\begin{bmatrix} G \\ B \\ R \end{bmatrix} = \begin{bmatrix} 1 & -689/2048 & -1430/2048 \\ 1 & 3548/2048 & 0 \\ 1 & 0 & 2807/2048 \end{bmatrix} \begin{bmatrix} Y \\ C_B \\ C_R \end{bmatrix}$$

SIN X/X CORRECTION

While $\overline{\text{BYPASS}}$ is high, SIN X/X correction is enabled on each of the three output channels. SIN X/X correction is implemented by passing the data through a FIR filter with the frequency response shown in Figure 7. While $\overline{\text{BYPASS}}$ is low, the FIR filter is bypassed and each channel is passed directly to the output processing section. Total latency through the device is 22 clock cycles when $\overline{\text{BYPASS}}$ is low and 24 clock cycles when BYPASS is high.

OUTPUT PROCESSING

Output data may be rounded to 10 or 8 bit accuracy. RND10/$\overline{8}$ should be set high for 10 bit output rounding and set low for 8 bit output rounding. Rounding to 8 bit accuracy is accomplished by adding a rounding bit to SO_1 and then zeroing both SO_0 and SO_1.

C_B and C_R data may be output as signed (two's complement) or unsigned (offset binary) data depending on the state of the CONVERT control signal. When CONVERT is set high, the C_B and C_R channels are output as signed (two's complement) data. When CONVERT is set low, C_B and C_R are output as unsigned (offset binary) data, obtained by inverting the sign bit of the two's complement number. When operating in RGB output mode, the CONVERT pin is over-ridden and RGB data is always output as unsigned (offset binary) data.

CONTROL SIGNAL/OPERATING MODE SUMMARY

SYNC

The SYNC control signal provides synchronization for the internal 4:2:2 de-multiplexer. SYNC should be held high on clock period N and low on clock period N+1 when the first C_B sample is presented to the $SI_{9..0}$ inputs. SYNC may be held low until re-synchronization is desired or may be toggled at every occurrence of a C_B sample.

SELECT_MATRIX AND SETUP

SELECT_MATRIX and SETUP select the color space conversion and offset insertions which the GF9103 is to perform. The following chart presents the available color space conversions and the corresponding states of the SELECT_MATRIX and SETUP control pins. SETUP is a dynamic pin that may be modified every clock cycle.

SELECT_MATRIX	SETUP	DESCRIPTION
0	0	Selects output to be over-sampled YC_BC_R with no setup in Y channel.
0	1	Selects output to be over-sampled YC_BC_R with a scaling factor of +947/1024 and an offset of +71 (decimal) applied to the Y channel.
1	X	Selects output to be over-sampled RGB with no setup.

SIN X/X CORRECTION

$\overline{BYPASS}$	DESCRIPTION
1	SIN X/X correction enabled on all output data channels. Latency through the device is 24 clock cycles.
0	SIN X/X correction disabled. Latency through the device is 22 clock cycles.

OUTPUT ROUNDING

RND10/$\overline{8}$	DESCRIPTION
1	Output data rounded to 10 bit resolution per channel.
0	Output data rounded to 8 bit resolution per channel.

TWO'S COMPLEMENT OUTPUT CONVERSION

CONVERT	SELECT_MATRIX	DESCRIPTION
1	0	$SOB_{9..0}$ and $SOC_{9..0}$ output signed (two's complement) C_B and C_R data.
0	0	$SOB_{9..0}$ and $SOC_{9..0}$ output unsigned (offset binary) C_B and C_R data.
X	1	$SOB_{9..0}$ and $SOC_{9..0}$ output unsigned B and R data.

OUTPUT ENABLE

$\overline{OE}$	DESCRIPTION
0	All output data ports are enabled.
1	All output data ports are in high impedance state.

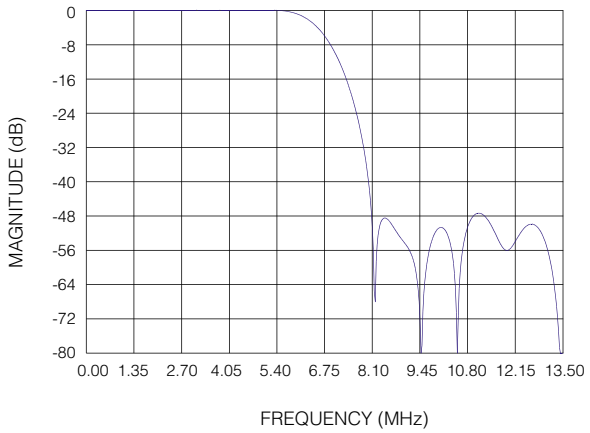

Fig. 3 Frequency Response of Luminance Interpolation Filter (Sampling at fs=27MHz)

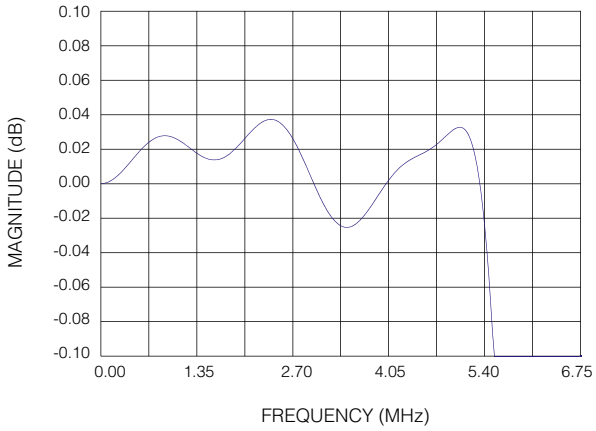

Fig. 4 Frequency Response of Luminance Interpolation Filter (Sampling at fs=27MHz)

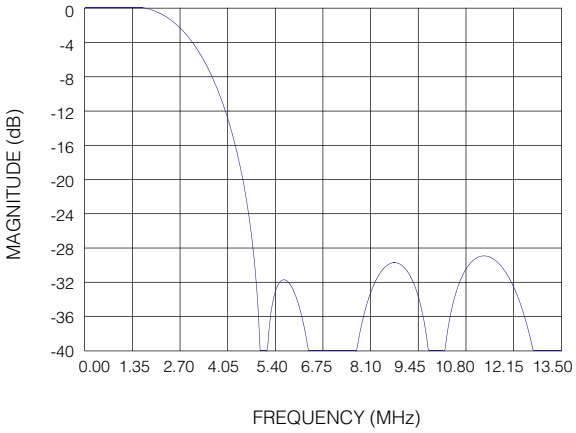

Fig. 5 Frequency Response of Chrominance Interpolation Filter (Sampling at fs=27MHz)

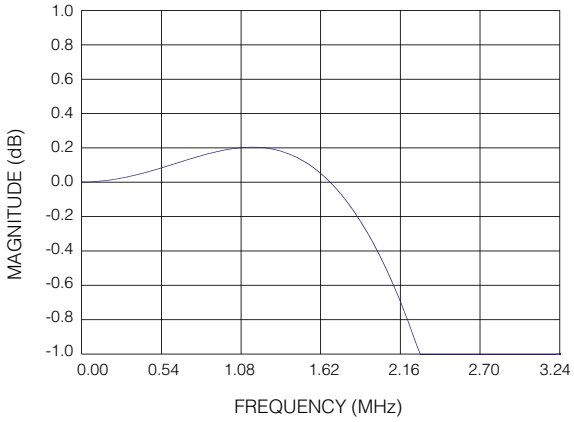

Fig. 6 Frequency Response of Chrominance Interpolation Filter (Sampling at fs=27MHz)

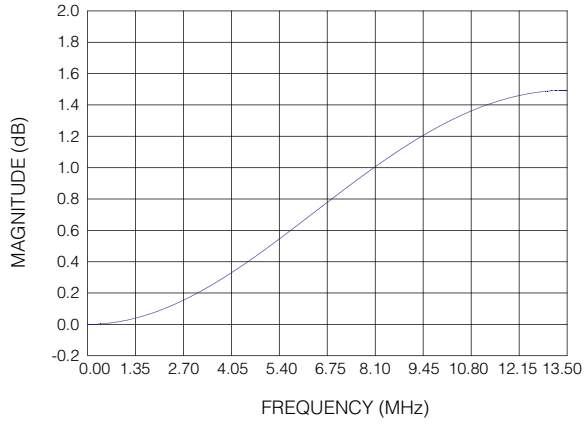

Fig. 7 SIN X/X Compensation Filter Frequency Response (Sampling at fs=27MHz)

PARAMETER	LUMINANCE FILTER	CHROMINANCE FILTER
Filter Order	31	15
Pass Band Ripple	+0.038 / -0.025 dB ($0.0\ f$s to $0.21\ f$s)	+0.2 / -0.2 dB ($0.0\ f$s to $0.21\ f$s)
DC Gain	0.0 dB	0.0 dB
Attenuation	-6.00 dB (at $f_S/4$)	-6.00 dB (at $f_S/8$)
Stop Band Attenuation	-47 dB ($0.30\ f$s to $0.50\ f$s)	-28 dB ($0.17\ f$s to $0.50\ f$s)

fig. 8 luminance and chrominance filter characteristics

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.3 to +7.0 V
Input Voltage Range (any input)	+0.5 to (V_{DD} +0.5) V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-65°C ≤ T_S ≤ 150°C
Lead Temperature Range (soldering 10 seconds)	260°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 0°C, R_L = 150 Ω to GND and 144 Ω AC coupled unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current Quiescent	I_{DDQ}	V_{DD} = Max, V_{IN} = 0V	-	5	9	mA
Supply Current Unloaded	I_{DDU}	V_{DD} = Max, $\overline{OE}$ = V_{DD}, f = 27MHz	-	85	150	mA
Input Voltage, Logic Low	V_{IL}		-	-	0.2V_{DD}	V
Input Voltage, Logic High	V_{IH}		0.7V_{DD}	-	-	V
Switching Threshold	V_T	CMOS	-	2.5	-	V
Input Current: (CMOS Inputs)	I_{IN}	V_{IN} = V_{DD} or GND	-10	±1	10	µA
Inputs with Pulldown Resistors		V_{IN} = V_{DD}	35	115	222	µA
Inputs with Pullup Resistors		V_{IN} = GND	-35	-115	-214	µA
Output Voltage, Logic Low	V_{OL}	V_{DD} = Min, I_{OL} = 4mA	-	0.2	0.4	V
Output Voltage, Logic High	V_{OH}	V_{DD} = Min, I_{OH} = -4mA	2.4	4.5	-	V
Hi-Z Output Leakage Current	I_{OZ}	V_{DD} = Max, $\overline{OE}$ = 1	-10	±1	10	µA
Short Circuit Output Current	I_{OS}	V_{DD} = Max, output high one pin to ground, one second duration max	-	-	140	mA
Input Capacitance	C_{IN}	T_A = 25°C, f = 1MHz	-	-	10	pF
Output Capacitance	C_{OUT}	T_A = 25°C, f = 1MHz	-	-	10	pF

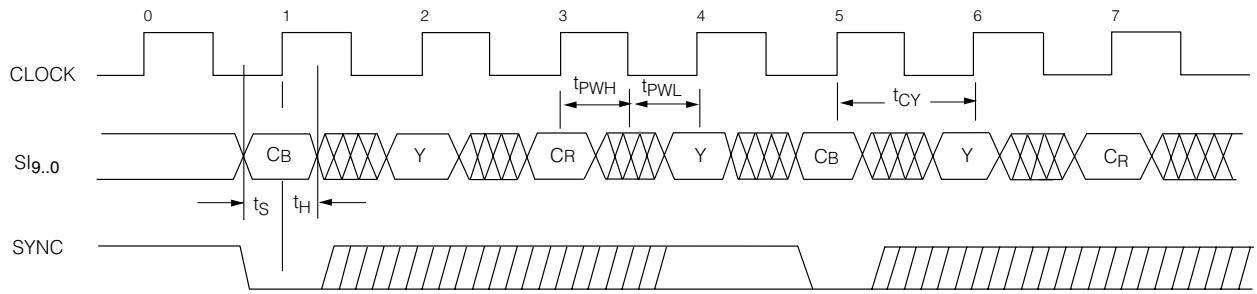

Fig. 9 Operation of SYNC Control Signal

SWITCHING CHARACTERISTICS

T_A from 0°C to 70°C unless otherwise specified.

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_D	Output delay	V_{DD} = Min, C_L = 25pF	8	9	10	ns
t_{OH}	Output hold time	V_{DD} = Max, C_L = 25pF	1	-	-	ns
t_{EN}	Output enable	V_{DD} = Min, C_L = 25pF	-	-	8	ns
t_{DIS}	Output disable	V_{DD} = Min, C_L = 25pF	-	-	8	ns
t_{CY}	Cycle time		25	-	-	ns
t_{PWL}	Clock pulse width low		10	-	-	ns
t_{PWH}	Clock pulse width high		10	-	-	ns
t_S	Input setup time		8	-	-	ns
t_H	Input hold time		1	-	-	ns

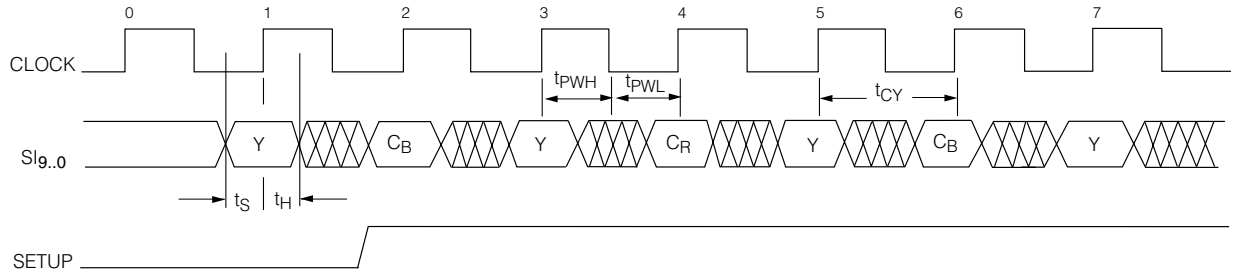

Fig. 10 Operation of SETUP Control Signal

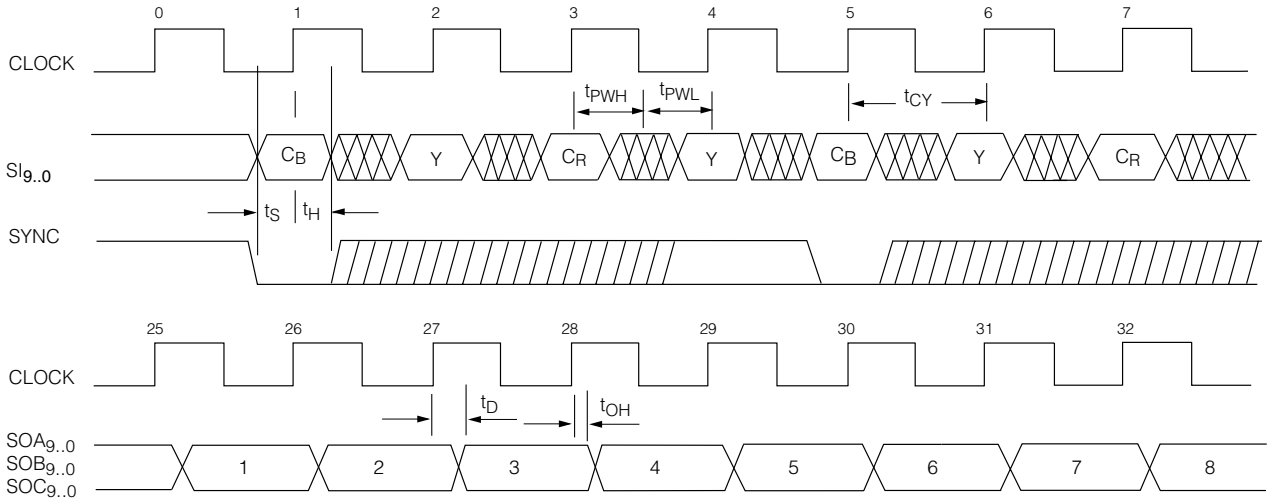

Fig. 11 Input/Output Timing, $\overline{\text{BYPASS}}$ = 1

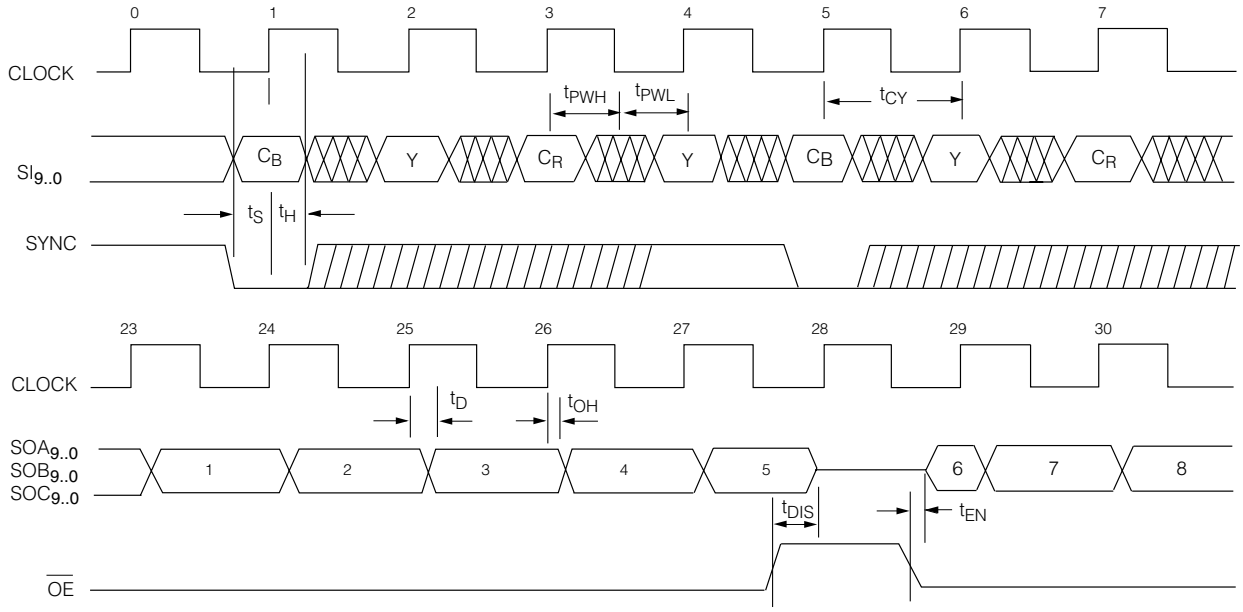

Fig. 12 Input/Output Timing, $\overline{\text{BYPASS}}$ = 0

CAUTION

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SENSITIVE DEVICES

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DOCUMENT IDENTIFICATION

DATA SHEET

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REVISION NOTES:

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