



### DESCRIPTION

The ES4318 Digital Video Disc (DVD) processor is a single-chip solution for a DVD player that integrates MPEG video decoding, DVD system navigation, Content Scrambling System (CSS), and Dolby™ Digital (AC-3) and MPEG audio decoding. The fully programmable ES4318 is based on a proprietary ESS architecture. It offers the best feature set in comparison to any currently existing DVD chip, and a glueless interface to various peripheral components. The ES4318 is the most cost effective solution in its class with an integration level and quality that set new benchmarks.

The ES4318 processor is capable of decoding Dolby™ Digital (AC-3) or DTS digital surround, simultaneously with MPEG-1 or MPEG-2 video. For embedded applications, the ES4318's internal RISC processor can be used in place of a microcontroller to provide all system control, DVD system navigation, CSS decryption, and many other features. On-chip, multi-tap filters provide arbitrary scaling with state of the art SmartScale™ technology useful for video standards conversion. SmartStream™ technology from ESS provides video error concealment and video post-processing, leading to the highest playability and video quality. Other features included in the ES4318 are video letterbox display, DVD Sub-Picture overlay, and On-Screen Display.

The ES4318 provides a glueless 8/16-bit parallel interface to most DVD servo/loaders. It connects directly with 8/16-bit ROM and 16-bit SDRAM/EDO. An 8-bit YUV video interface supports many TV encoders. General purpose auxiliary pins are provided to control various peripheral devices. A standard I²S interface supports popular audio DACs and ADCs. The ES4318 also features a direct S/PDIF output. A block diagram of a typical stand-alone system using the ES4318 with the glueless SDRAM interface appears below.

The DVD system stream from a DVD disc is passed to the ES4318 through the 8-bit/16-bit parallel host interface. The ES4318 parses the system layer and demultiplexes the audio and video streams. Audio is decoded and passed through the I²S audio serial bus to an external audio DAC and then to the speakers. Video is decoded and output as YUV pixels to an NTSC or PAL video encoder. System control and housekeeping functions (keypad and remote control) are also provided on-chip.

### FEATURES

- Single-chip DVD video decoder in a 208-pin PQFP package
- MPEG-1 system and MPEG-2 program streams parsing supported
- Programmable multimedia processor architecture
- Compatible with Audio CD, VideoCD, VCD 3.0, and Super VideoCD (SVCD)
- DVD Navigation 1
- Built-in Content Scrambling System (CSS) circuitry

#### Video

- Pan & Scan and Letter-Box conversions
- Trick modes include Slow, Fast Forward, Fast Reverse, Step, and Goto
- Sub-Picture decoder supports karaoke/subtitling functions
- 4-bit On-Screen Display (OSD) with 4-bit blending
- 8-bit YUV component video output

#### Audio

- Built-in Karaoke key-shift function
- Dolby™ Digital 2-channel downmix audio output for Dolby™
- Dolby Pro Logic
- Linear PCM streams for 24 bit/96KHz
- Concurrent S/PDIF out and 2-channel audio output
- Sensaura Dolby Digital Virtual Surround
- DTS Digital Surround 2-channel downmix stereo output
- S/PDIF output for encoded AC-3, DTS Digital output or Linear PCM

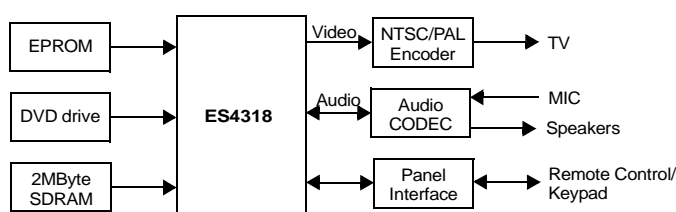
#### Peripheral

- Glueless interface to DVD loaders (ATAPI or A/V bus I/F)
- Bidirectional I²S audio interface
- Direct servo/loader interface
- 8 general-purpose auxiliary ports
- Single 27 MHz clock input

#### Smart Technology

- SmartZoom™ for motion zoom and pan
- SmartScale™ for NTSC to PAL conversion and vice versa
- SmartStream™ for video error concealment; supports Microsoft Windows™ Sound System®

### BLOCK DIAGRAM



PINOUT

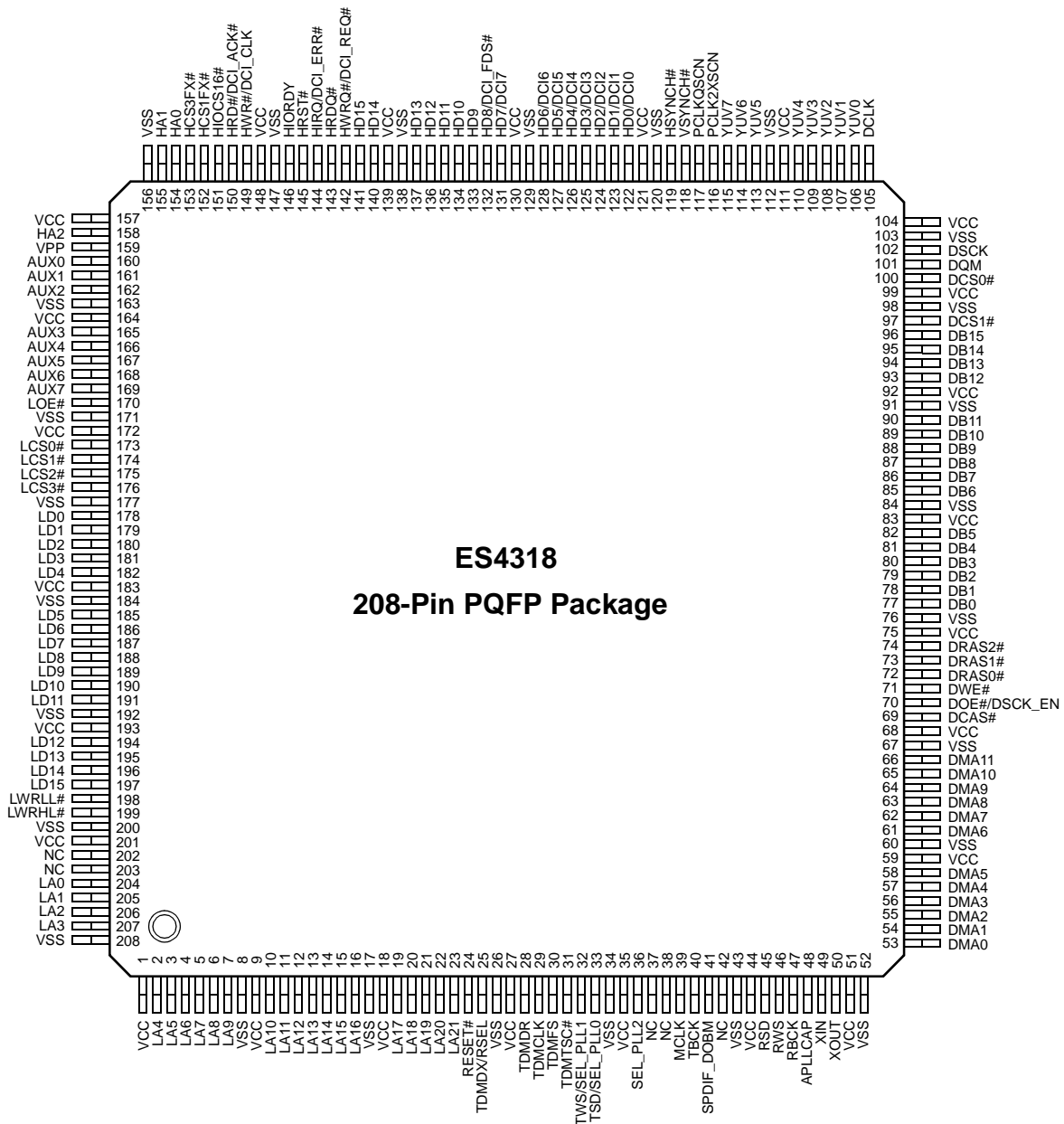


Figure 1 ES4318 Device Pinout

PIN DESCRIPTION

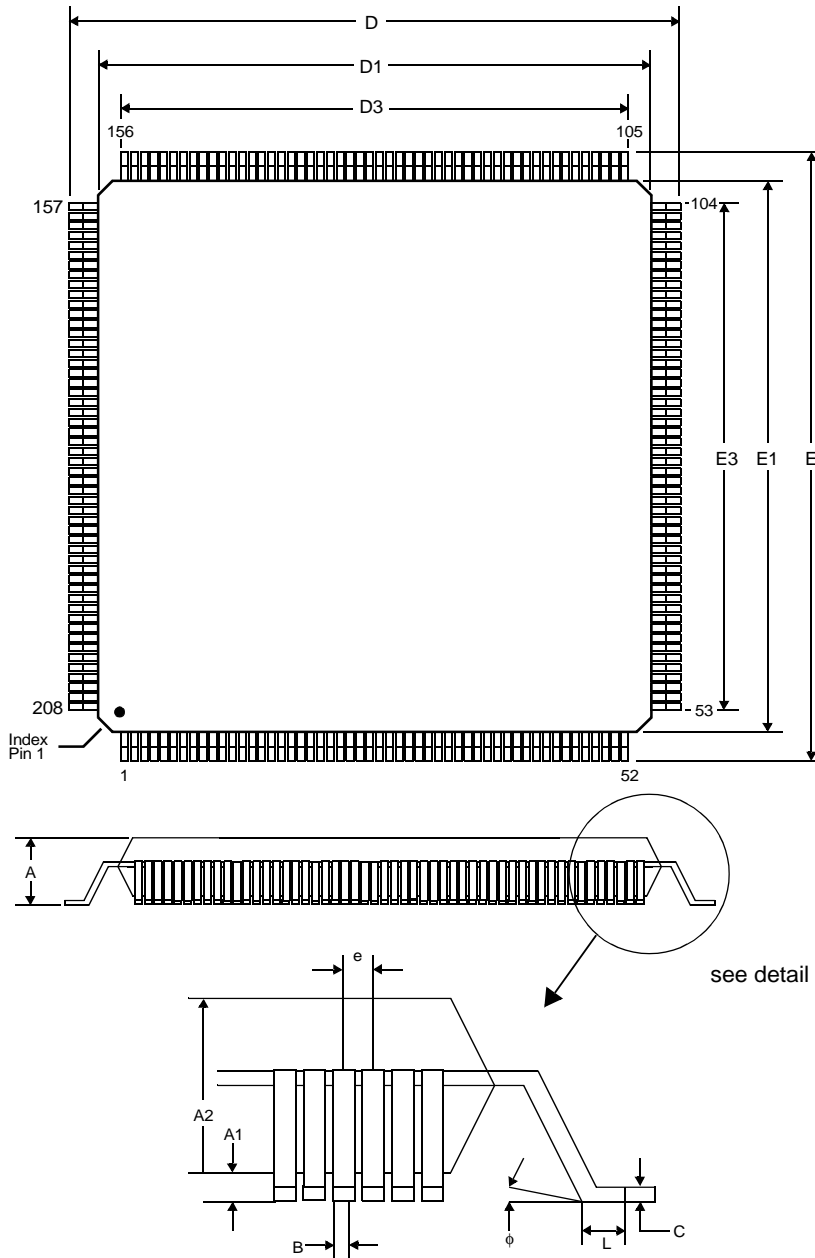
Name	Number	I/O	Definition
VCC	1, 9, 18, 27, 35, 44, 51, 59, 68, 75, 83, 92, 99, 104, 111, 121, 130, 139, 148, 157, 164, 172, 183, 193, 201	I	3.65 V ± 150 mv.
LA[21:0]	23:19,16:10,7:2,207:204	O	Device address output.
VSS	8,17,26,34,43,52,60,67,76,84,91,98,103,112,120,129,138,147,156,163,171,177,184,192,200,208	I	Ground.
RESET#	24	I	Reset input, active low.



Name	Number	I/O	Definition															
TDMDX RSEL	25	O	TDM transmit data.															
		I	ROM Select <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>RSEL</th> <th>Selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>16-bit ROM</td> </tr> <tr> <td>1</td> <td>8-bit ROM</td> </tr> </tbody> </table>	RSEL	Selection	0	16-bit ROM	1	8-bit ROM									
RSEL	Selection																	
0	16-bit ROM																	
1	8-bit ROM																	
TDMDR	28	I	TDM receive data.															
TDMCLK	29	I	TDM clock input.															
TDMFS	30	I	TDM frame synch.															
TDMTSC#	31	O	TDM output enable, active low.															
TWS	32	O	Audio transmit frame sync.															
SEL_PLL1		I	Select PLL1.															
TSD	33	O	Audio transmit serial data port.															
SEL_PLL0		I	Select PLL0. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SEL_PLL2</th> <th>SEL_PLL0</th> <th>Clock Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>2.5 x DCLK</td> </tr> <tr> <td>0</td> <td>1</td> <td>3 x DCLK</td> </tr> <tr> <td>1</td> <td>0</td> <td>3.5 x DCLK</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 x DCLK</td> </tr> </tbody> </table>	SEL_PLL2	SEL_PLL0	Clock Output	0	0	2.5 x DCLK	0	1	3 x DCLK	1	0	3.5 x DCLK	1	1	4 x DCLK
SEL_PLL2		SEL_PLL0	Clock Output															
0	0	2.5 x DCLK																
0	1	3 x DCLK																
1	0	3.5 x DCLK																
1	1	4 x DCLK																
SEL_PLL2			Select PLL2. See the table for pin number 33.															
MCLK	39	I/O	Audio master clock for audio DAC.															
TBCK	40	I/O	Audio transmit bit clock.															
SPDIF_DOBM	41	O	S/PDIF (IEC958) Format Output.															
RSD	45	I	Audio receive serial data.															
RWS	46	I	Audio receive frame synch.															
RBCK	47	I	Audio receive bit clock.															
APLLCAP	48	I	Analog PLL Capacitor.															
XIN	49	I	Crystal input.															
XOUT	50	O	Crystal output.															
DMA[11:0]	66:61,58:53	O	DRAM address bus.															
DCAS#	69	O	Column address strobe, active low.															
DOE#	70	O	Output enable, active low.															
DSCK_EN		I	Clock Enable, active low.															
DWE#	71	O	DRAM write enable, active low.															
DRAS[2:0]#	74:72	O	Row address strobe, active low.															
DB[15:0]	96:93,90:85,82:77	I/O	DRAM data bus.															
DCS[1:0]#	97,100	O	SDRAM chip select [1:0], active low.															
DQM	101	O	Data input/output mask.															
DSCK	102	O	Clock to SDRAM.															
DCLK	105	I	Clock Input (27 MHz)															
YUV[7:0]	115:113,110:106	O	8-bit YUV output.															
PCLK2XSCN	116	I/O	2X pixel clock.															
PCLKQSCN	117	I/O	Pixel clock.															
VSYNCH#	118	I/O	Vertical sync for screen video interface, programmable for rising or falling edge, active low.															
HSYNCH#	119	I/O	Horizontal sync for screen video interface, programmable for rising or falling edge, active low.															
HD[15:0]	141:140,137:131,128:122	O	Host data bus															
HCS1FX#	152	O	Host select 1.															
HCS3FX#	153	O	Host select 3.															
HIOCS16#	151	I	Device 16-bit data transfer.															
HA[2:0]	158, 155:154	I/O	Host address bus.															
VPP	159	I	Peripheral protection voltage.															
HWR#/DCI_ACK#	149	I,I	Host write/DCI Interface Acknowledge Signal, active low.															
HRD#/DCI_CLK	150	I,I	Host read/DCI Interface Clock.															
HD[15:0]	141:140,137:131,128:122	I/O	Host data bus.															
HWRQ#	142	O	Host write request.															
HRDQ#	143	O	Host read request.															
HIRO	144	I/O	Host interrupt.															
HRST#	145	O	Host reset.															
HIORDY	146	I	Host I/O ready.															
HWR#	149	O	Host write request.															
AUX[7:0]	169:165,162:160	I/O	Auxiliary ports.															
LOE#	170	O	Device output enable, active low.															
LCS[3:0]#	176:173	O	Chip select [3:0], active low.															
LD[15:0]	197:194, 191:185, 182:178	I/O	Device data bus.															
LWRLL#	198	O	Device write enable, active low.															
LWRHL#	199	O	Device write enable, active low.															
NC	37,38,42,203:202		No connect.															

**ORDERING INFORMATION**

Part Number	Description	Package
ES4318	DVD Processor	208-pin TQFP



Note:  
 1. All dimensions are in inches (millimeter).  
 2. Actual package used has millimeter native dimensions – take care with rounding from metric to imperial.

Symbol	Min	Nom	Max
A	–	–	0.165
A1	0.010 (0.25)	–	–
A2	0.130 (3.30)	0.134 (3.40)	0.138 (3.50)
B	0.007 (0.18)	0.009 (0.23)	0.011 (0.28)
C	0.005 (0.12)	0.006 (0.16)	0.008 (0.20)
D	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
D1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
D3	1.004 (25.50) REF		
e	0.0197 (0.50) BASIC		
E	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
E1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)



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