



**CY28435**

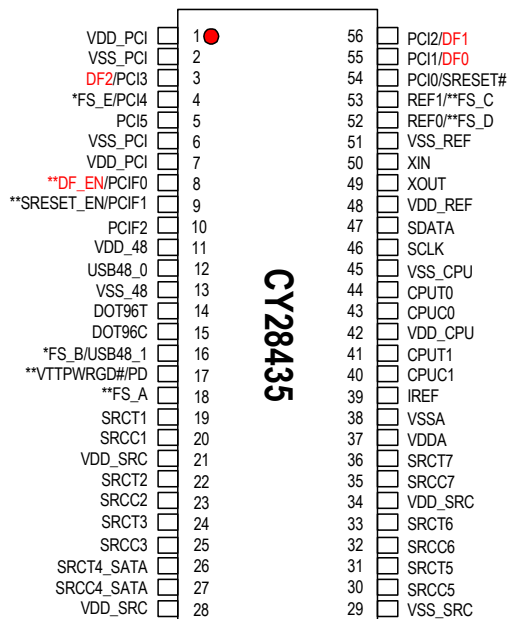
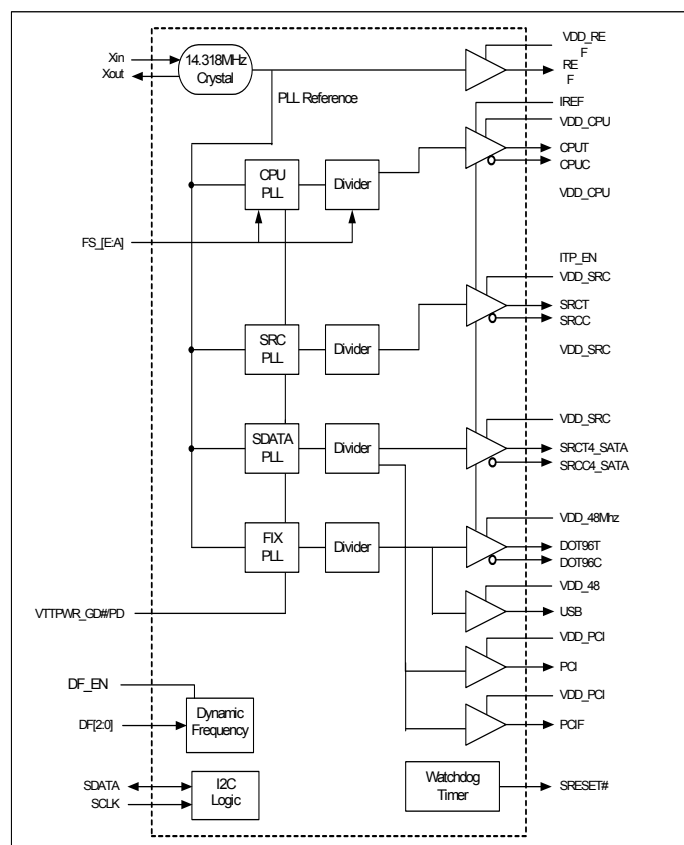
# Clock Generator for Intel® Grantsdale Chipset

- Compliant to Intel® CK410
- Supports Intel Prescott and Tejas CPUs
- Selectable CPU frequencies
- Differential CPU clock pairs
- 100-MHz differential SRC clocks
- 96-MHz differential dot clock
- 48-MHz USB clocks
- 33-MHz PCI clock
- Dynamic Frequency Control

- **Dial-A-Frequency®**
- **Watchdog**
- **Two Independent Overclocking PLLs**
- **Low-voltage frequency select input**
- **I<sup>2</sup>C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **3.3V power supply**
- **56-pin SSOP and TSSOP packages**

|     |     |     |     |       |     |
|-----|-----|-----|-----|-------|-----|
| CPU | SRC | PCI | REF | DOT96 | USB |
| x 2 | x 7 | x 9 | x 2 | x 1   | x 2 |

## Pin Configuration



\* indicates internal pull-up  
\*\* indicates internal pull-down

**Pin Description**

| Pin No.                                | Name                   | Type        | Description  |
|--|------------------------|-------------|--|
| 1,7                                    | VDD_PCI                | PWR         | <b>3.3V power supply for outputs.</b>  |
| 2,6                                    | VSS_PCI                | GND         | <b>Ground for outputs.</b>   |
| 3,55,56                                | DF/PCI                 | I/O, SE     | <b>3.3V LVTTTL input to enable Dynamic Frequency input/33-MHz clock output.</b>  |
| 4                                      | FS_E/PCI4              | I/O,PU, SE  | <b>3.3V-tolerant input for CPU frequency selection/33-MHz clock.</b><br><i>Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</i>   |
| 5                                      | PCI                    | O, SE       | <b>33-MHz clock.</b>   |
| 8                                      | DF_EN/PCIF0            | I/O,SE, PD  | <b>3.3V LVTTTL input to enable Dynamic Frequency input/33-MHz clock output.</b><br>(sampled on the VTT_PWRGD# assertion).<br>1 = Enable, 0 = Disable   |
| 9                                      | SRESET_EN/PCIF1        | I/O,SE, PD  | <b>3.3V LVTTTL input to enable Watchdog/33-MHz clocks.</b><br>1 = Enable, 0 = Disable  |
| 10                                     | PCIF2                  | O, SE       | <b>33-MHz clocks.</b>  |
| 17                                     | VTT_PWRGD#/PD          | I, PD       | <b>3.3V LVTTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, FS_D and FS_E inputs.</b> After VTT_PWRGD# (active LOW) assertion, this pin becomes a real-time input for asserting power down (active HIGH). |
| 11                                     | VDD_48                 | PWR         | <b>3.3V power supply for outputs.</b>  |
| 12                                     | USB48_0                | O           | <b>48-MHz clock output.</b>  |
| 18                                     | FS_A                   | I, PD       | <b>3.3V-tolerant input for CPU frequency selection.</b><br><i>Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</i>  |
| 13                                     | VSS_48                 | GND         | <b>Ground for outputs.</b>   |
| 14,15                                  | DOT96T, DOT96C         | O, DIF      | <b>Fixed 96-MHz clock output.</b>  |
| 16                                     | FS_B/USB48_1           | I/O,PU, SE  | <b>3.3V-tolerant input for CPU frequency selection/fixed 48-MHz clock output.</b><br><i>Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</i>  |
| 19,20,22,23, 24,25,30,31, 32,33,36, 35 | SRCT/C                 | O, DIF      | <b>Differential serial reference clocks.</b> Outputs have overclocking capability.   |
| 21,28,34                               | VDD_SRC                | PWR         | <b>3.3V power supply for outputs.</b>  |
| 26,27                                  | SRC4_SATAT, SRC4_SATAC | O, DIF      | <b>Differential serial reference clock.</b> Recommended output for SATA.   |
| 29                                     | VSS_SRC                | GND         | <b>Ground for outputs.</b>   |
| 37                                     | VDDA                   | PWR         | <b>3.3V power supply for PLL.</b>  |
| 38                                     | VSSA                   | GND         | <b>Ground for PLL.</b>   |
| 39                                     | IREF                   | I           | <b>A precision resistor is attached to this pin,</b> which is connected to the internal current reference.   |
| 42                                     | VDD_CPU                | PWR         | <b>3.3V power supply for outputs.</b>  |
| 41,40,44,43                            | CPUT/C                 | O, DIF      | <b>Differential CPU clock outputs.</b>   |
| 45                                     | VSS_CPU                | GND         | <b>Ground for outputs.</b>   |
| 46                                     | SCLK                   | I           | <b>SMBus-compatible SCLOCK.</b>  |
| 47                                     | SDATA                  | I/O         | <b>SMBus-compatible SDATA.</b>   |
| 48                                     | VDD_REF                | PWR         | <b>3.3V power supply for outputs.</b>  |
| 49                                     | XOUT                   | O, SE       | <b>14.318-MHz crystal output.</b>  |
| 50                                     | XIN                    | I           | <b>14.318-MHz crystal input.</b>   |
| 51                                     | VSS_REF                | GND         | <b>Ground for outputs.</b>   |
| 52                                     | FS_D/REF0              | I/O, SE, PD | <b>3.3V-tolerant input for CPU frequency selection/Reference clock.</b><br><i>Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</i>  |

**Pin Description (continued)**

| Pin No. | Name         | Type    | Description   |
|---------|--------------|---------|---|
| 53      | FS_C/REF1    | I/O, PD | <b>3.3V-tolerant input for CPU frequency selection/Reference clock.</b><br>Selects test mode if pulled to $V_{IHFS\_C}$ when VTT_PWRGD# is asserted LOW.<br><i>Refer to DC Electrical Specifications table for <math>V_{ILFS\_C}</math>, <math>V_{IMFS\_C}</math>, <math>V_{IHFS\_C}</math> specifications.</i> |
| 54      | SRESET#/PCIO | O, PU   | <b>3.3V LVTTTL output for Watchdog reset/33-MHz clock output.</b><br>When configured as SRESET# output this output becomes open drain type with a high (>100 k $\Omega$ ) internal pull-up resistor.  |

**Frequency Select Pins (FS\_[A:E])**

Host clock frequency selection is achieved by applying the appropriate logic levels to FS\_A, FS\_B, FS\_C, FS\_D and FS\_E inputs prior to VTT\_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT\_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS\_A, FS\_B, FS\_C, FS\_D and FS\_E input values. For all logic levels of FS\_A, FS\_B, FS\_C, FS\_D and FS\_E, VTT\_PWRGD# employs a one-shot functionality in that once a valid low on VTT\_PWRGD# has

been sampled, all further VTT\_PWRGD#, FS\_A, FS\_B, FS\_C, FS\_D and FS\_E transitions will be ignored, except in test mode.

FS\_C is a three level input, when sampled at a voltage greater than 2.1V by VTT\_PWRGD#, the device will enter test mode as selected by the voltage level on the FS\_B input.

**Serial Data Interface**

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial

**No Spread Spectrum and Center spread spectrum on CPU PLL**

|                      | FS_E    | Input Conditions |        |        |        | Output Frequency |             |                        |               |               |                               | SRC PLL Gear Constants | SRC M divider (not changeable by user) |
|----------------------|---------|------------------|--------|--------|--------|------------------|-------------|------------------------|---------------|---------------|-------------------------------|------------------------|--|
|                      |         | FS_D             | FS_C   | FS_B   | FS_A   | CPU              | SRC         | CPU PLL Gear Constants | CPU M divider | CPU N DEFAULT | CPU N allowable range for DAF |                        |  |
| FS_5 (byte 16 bit 5) | HW only | FSEL_3           | FSEL_2 | FSEL_1 | FSEL_0 | (MHz)            | (MHz)       | (G)                    |               |               |                               |                        |  |
| 0                    | 1       | 0                | 1      | 0      | 1      | 100              | 100         | 30                     | 60            | 200           | 200 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 0                | 0      | 0      | 1      | 133.3333333      | 100         | 40                     | 60            | 200           | 200 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 0                | 0      | 1      | 1      | 166.6666667      | 100         | 60                     | 63            | 175           | 175 - 262                     | 30                     | 60                                     |
| 0                    | 1       | 0                | 0      | 1      | 0      | 200              | 100         | 60                     | 60            | 200           | 200 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 0                | 0      | 0      | 0      | 266.6666667      | 100         | 80                     | 60            | 200           | 200 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 0                | 1      | 0      | 0      | 333.3333333      | 100         | 120                    | 63            | 175           | 175 - 262                     | 30                     | 60                                     |
| 0                    | 1       | 0                | 1      | 1      | 0      | 400              | 100         | 120                    | 60            | 200           | 200 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 1      | 0      | 1      | 100.952381       | 100         | 30                     | 63            | 212           | 212 - 262                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 0      | 0      | 1      | 133.968254       | 100         | 40                     | 63            | 211           | 211 - 262                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 0      | 1      | 1      | 167              | 100         | 60                     | 60            | 167           | 167 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 0      | 1      | 0      | 200.952381       | 100         | 60                     | 63            | 211           | 211 - 262                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 0      | 0      | 0      | 266.6666667      | 100         | 80                     | 60            | 200           | 200 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 1      | 0      | 0      | 334              | 100         | 120                    | 60            | 167           | 167 - 250                     | 30                     | 60                                     |
| 0                    | 1       | 1                | 1      | 1      | 0      | 400.6451613      | 100         | 120                    | 62            | 207           | 207 - 258                     | 30                     | 60                                     |
| 0                    | 0       | 0                | 1      | 0      | 1      | 100              | 111.3333333 | 30                     | 60            | 200           | 200 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 0                | 0      | 0      | 1      | 133.33           | 111.3333333 | 40                     | 60            | 200           | 200 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 0                | 0      | 1      | 1      | 166.67           | 111.3333333 | 60                     | 63            | 175           | 175 - 262                     | 40                     | 60                                     |
| 0                    | 0       | 0                | 0      | 1      | 0      | 200              | 111.3333333 | 60                     | 60            | 200           | 200 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 0                | 0      | 0      | 0      | 266.67           | 111.3333333 | 80                     | 60            | 200           | 200 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 0                | 1      | 0      | 0      | 333.33           | 111.3333333 | 120                    | 63            | 175           | 175 - 262                     | 40                     | 60                                     |
| 0                    | 0       | 0                | 1      | 1      | 0      | 400              | 111.3333333 | 120                    | 60            | 200           | 200 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 1      | 0      | 1      | 100.95           | 111.3333333 | 30                     | 63            | 212           | 212 - 262                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 0      | 0      | 1      | 133.97           | 111.3333333 | 40                     | 63            | 211           | 211 - 262                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 0      | 1      | 1      | 166.98           | 111.3333333 | 60                     | 60            | 167           | 167 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 0      | 1      | 0      | 200.95           | 111.3333333 | 60                     | 63            | 211           | 211 - 262                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 0      | 0      | 0      | 266.67           | 111.3333333 | 80                     | 60            | 200           | 200 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 1      | 0      | 0      | 333.97           | 111.3333333 | 120                    | 60            | 167           | 167 - 250                     | 40                     | 60                                     |
| 0                    | 0       | 1                | 1      | 1      | 0      | 400.65           | 111.3333333 | 120                    | 62            | 207           | 207 - 258                     | 40                     | 60                                     |
| 1                    | X       | 0                | 1      | 0      | 1      | 100              | 167         | 30                     | 60            | 200           | 200 - 250                     | 60                     | 60                                     |
| 1                    | X       | 0                | 0      | 0      | 1      | 133.33           | 167         | 40                     | 60            | 200           | 200 - 250                     | 60                     | 60                                     |
| 1                    | X       | 0                | 0      | 1      | 1      | 166.67           | 167         | 60                     | 63            | 175           | 175 - 262                     | 60                     | 60                                     |
| 1                    | X       | 0                | 0      | 1      | 0      | 200              | 167         | 60                     | 60            | 200           | 200 - 250                     | 60                     | 60                                     |
| 1                    | X       | 0                | 0      | 0      | 0      | 266.67           | 167         | 80                     | 60            | 200           | 200 - 250                     | 60                     | 60                                     |
| 1                    | X       | 0                | 1      | 0      | 0      | 333.33           | 167         | 120                    | 63            | 175           | 175 - 262                     | 60                     | 60                                     |
| 1                    | X       | 0                | 1      | 1      | 0      | 400              | 167         | 120                    | 60            | 200           | 200 - 250                     | 60                     | 60                                     |
| 1                    | X       | 1                | 1      | 0      | 1      | 100.95           | 167         | 30                     | 63            | 212           | 212 - 262                     | 60                     | 60                                     |
| 1                    | X       | 1                | 0      | 0      | 1      | 133.97           | 167         | 40                     | 63            | 211           | 211 - 262                     | 60                     | 60                                     |

**Figure 1. CPU and SRC Frequency Select Tables**

Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For

block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 1. Command Code Definition**

| Bit   | Description   |
|-------|---|
| 7     | 0 = Block read or block write operation, 1 = Byte read or byte write operation  |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol |  | Block Read Protocol |                                     |
|----------------------|--|---------------------|-------------------------------------|
| Bit                  | Description  | Bit                 | Description                         |
| 1                    | Start  | 1                   | Start                               |
| 8:2                  | Slave address – 7 bits   | 8:2                 | Slave address – 7 bits              |
| 9                    | Write  | 9                   | Write                               |
| 10                   | Acknowledge from slave   | 10                  | Acknowledge from slave              |
| 18:11                | Command Code – 8 bits  | 18:11               | Command Code – 8 bits               |
| 19                   | Acknowledge from slave   | 19                  | Acknowledge from slave              |
| 27:20                | Byte Count – 8 bits<br>(Skip this step if I <sup>2</sup> C_EN bit set) | 20                  | Repeat start                        |
| 28                   | Acknowledge from slave   | 27:21               | Slave address – 7 bits              |
| 36:29                | Data byte 1 – 8 bits   | 28                  | Read = 1                            |
| 37                   | Acknowledge from slave   | 29                  | Acknowledge from slave              |
| 45:38                | Data byte 2 – 8 bits   | 37:30               | Byte Count from slave – 8 bits      |
| 46                   | Acknowledge from slave   | 38                  | Acknowledge                         |
| ....                 | Data Byte /Slave Acknowledges  | 46:39               | Data byte 1 from slave – 8 bits     |
| ....                 | Data Byte N – 8 bits   | 47                  | Acknowledge                         |
| ....                 | Acknowledge from slave   | 55:48               | Data byte 2 from slave – 8 bits     |
| ....                 | Stop   | 56                  | Acknowledge                         |
|                      |  | ....                | Data bytes from slave / Acknowledge |
|                      |  | ....                | Data Byte N from slave – 8 bits     |
|                      |  | ....                | NOT Acknowledge                     |
|                      |  | ....                | Stop                                |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                        | Byte Read Protocol |                        |
|---------------------|------------------------|--------------------|------------------------|
| Bit                 | Description            | Bit                | Description            |
| 1                   | Start                  | 1                  | Start                  |
| 8:2                 | Slave address – 7 bits | 8:2                | Slave address – 7 bits |
| 9                   | Write                  | 9                  | Write                  |
| 10                  | Acknowledge from slave | 10                 | Acknowledge from slave |

**Table 3. Byte Read and Byte Write Protocol (continued)**

| Byte Write Protocol |                        | Byte Read Protocol |                          |
|---------------------|------------------------|--------------------|--------------------------|
| Bit                 | Description            | Bit                | Description              |
| 18:11               | Command Code – 8 bits  | 18:11              | Command Code – 8 bits    |
| 19                  | Acknowledge from slave | 19                 | Acknowledge from slave   |
| 27:20               | Data byte – 8 bits     | 20                 | Repeated start           |
| 28                  | Acknowledge from slave | 27:21              | Slave address – 7 bits   |
| 29                  | Stop                   | 28                 | Read                     |
|                     |                        | 29                 | Acknowledge from slave   |
|                     |                        | 37:30              | Data from slave – 8 bits |
|                     |                        | 38                 | NOT Acknowledge          |
|                     |                        | 39                 | Stop                     |

## Control Registers

### Byte 0: Control Register 0

| Bit | @Pup | Name           | Description   |
|-----|------|----------------|---|
| 7   | 1    | SRC[T/C]7      | SRC[T/C]7 Output Enable<br>0 = Disable (Tri-state), 1 = Enable      |
| 6   | 1    | SRC[T/C]6      | SRC[T/C]6 Output Enable<br>0 = Disable (Tri-state), 1 = Enable      |
| 5   | 1    | SRC[T/C]5      | SRC[T/C]5 Output Enable<br>0 = Disable (Tri-state), 1 = Enable      |
| 4   | 1    | SRC[T/C]4_SATA | SRC[T/C]4_SATA Output Enable<br>0 = Disable (Tri-state), 1 = Enable |
| 3   | 1    | SRC[T/C]3      | SRC[T/C]3 Output Enable<br>0 = Disable (Tri-state), 1 = Enable      |
| 2   | 1    | SRC[T/C]2      | SRC[T/C]2 Output Enable<br>0 = Disable (Tri-state), 1 = Enable      |
| 1   | 1    | SRC[T/C]1      | SRC[T/C]1 Output Enable<br>0 = Disable (Tri-state), 1 = Enable      |
| 0   | 1    | RESERVED       | RESERVED, Set = 1   |

### Byte 1: Control Register 1

| Bit | @Pup | Name      | Description  |
|-----|------|-----------|--|
| 7   | 1    | PCIF0     | PCIF0 Output Enable<br>0 = Disabled, 1 = Enabled                       |
| 6   | 1    | DOT_96T/C | DOT_96 MHz Output Enable<br>0 = Disable (Tri-state), 1 = Enabled       |
| 5   | 1    | USB48_0   | USB48_0 MHz Output Enable<br>0 = Disabled, 1 = Enabled                 |
| 4   | 1    | REF0      | REF0 Output Enable<br>0 = Disabled, 1 = Enabled                        |
| 3   | 0    | RESERVED  | RESERVED, Set = 0  |
| 2   | 1    | CPU[T/C]1 | CPU[T/C]1 Output Enable<br>0 = Disable (Tri-state), 1 = Enabled        |
| 1   | 1    | CPU[T/C]0 | CPU[T/C]0 Output Enable<br>0 = Disable (Tri-state), 1 = Enabled        |
| 0   | 0    | CPU       | PLL1 (CPU PLL) Spread Spectrum Enable<br>0 = Spread off, 1 = Spread on |

**Byte 2: Control Register 2**

| Bit | @Pup | Name  | Description                                      |
|-----|------|-------|--|
| 7   | 1    | PCI5  | PCI5 Output Enable<br>0 = Disabled, 1 = Enabled  |
| 6   | 1    | PCI4  | PCI4 Output Enable<br>0 = Disabled, 1 = Enabled  |
| 5   | 1    | PCI3  | PCI3 Output Enable<br>0 = Disabled, 1 = Enabled  |
| 4   | 1    | PCI2  | PCI2 Output Enable<br>0 = Disabled, 1 = Enabled  |
| 3   | 1    | PCI1  | PCI1 Output Enable<br>0 = Disabled, 1 = Enabled  |
| 2   | 1    | PCI0  | PCI0 Output Enable<br>0 = Disabled, 1 = Enabled  |
| 1   | 1    | PCIF2 | PCIF2 Output Enable<br>0 = Disabled, 1 = Enabled |
| 0   | 1    | PCIF1 | PCIF1 Output Enable<br>0 = Disabled, 1 = Enabled |

**Byte 3: Control Register 3**

| Bit | @Pup | Name           | Description  |
|-----|------|----------------|--|
| 7   | 0    | SRC[T/C]7      | Allow control of SRC[T/C]7 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#      |
| 6   | 0    | SRC[T/C]6      | Allow control of SRC[T/C]6 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#      |
| 5   | 0    | SRC[T/C]5      | Allow control of SRC[T/C]5 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#      |
| 4   | 0    | SRC[T/C]4_SATA | Allow control of SRC[T/C]4_SATA with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP# |
| 3   | 0    | SRC[T/C]3      | Allow control of SRC[T/C]3 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#      |
| 2   | 0    | SRC[T/C]2      | Allow control of SRC[T/C]2 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#      |
| 1   | 0    | SRC[T/C]1      | Allow control of SRC[T/C]1 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#      |
| 0   | 0    | RESERVED       | RESERVED, Set = 0  |

**Byte 4: Control Register 4**

| Bit | @Pup | Name       | Description  |
|-----|------|------------|--|
| 7   | HW   | FS_E       | FS_E Reflects the value of the FS_E pin sampled on power-up. 0 = FS_E was LOW during VTT_PWRGD# assertion. |
| 6   | 0    | DOT96[T/C] | DOT_PWRDWN Drive Mode<br>0 = Driven in PWRDWN, 1 = Tri-state   |
| 5   | 0    | PCIF2      | Allow control of PCIF2 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#        |
| 4   | 0    | PCIF1      | Allow control of PCIF1 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#        |
| 3   | 0    | PCIF0      | Allow control of PCIF0 with assertion of SW PCI_STP#<br>0 = Free running, 1 = Stopped with PCI_STP#        |
| 2   | 1    | RESERVED   | RESERVED, Set = 1  |
| 1   | 1    | RESERVED   | RESERVED, Set = 1  |
| 0   | 1    | RESERVED   | RESERVED, Set = 1  |

**Byte 5: Control Register 5**

| Bit | @Pup | Name          | Description   |
|-----|------|---------------|---|
| 7   | 0    | SRC[T/C]      | SRC[T/C] Stop Drive Mode<br>0 = Driven when SW PCI_STP# asserted, 1 = Tri-state when SW PCI_STP# asserted |
| 6   | 0    | RESERVED      | RESERVED, Set = 0   |
| 5   | 0    | RESERVED      | RESERVED, Set = 0   |
| 4   | 0    | RESERVED      | RESERVED, Set = 0   |
| 3   | 0    | SRC[T/C][7:1] | SRC[T/C][7:1] PWRDWN Drive Mode<br>0 = Driven when PD asserted, 1 = Tri-state when PD asserted            |
| 2   | 0    | RESERVED      | RESERVED, Set = 0   |
| 1   | 0    | CPU[T/C]1     | CPU[T/C]1 PWRDWN Drive Mode<br>0 = Driven when PD asserted, 1 = Tri-state when PD asserted                |
| 0   | 0    | CPU[T/C]0     | CPU[T/C]0 PWRDWN Drive Mode<br>0 = Driven when PD asserted, 1 = Tri-state when PD asserted                |

**Byte 6: Control Register 6**

| Bit | @Pup | Name   | Description  |
|-----|------|--|--|
| 7   | 0    | TEST_SEL   | REF/N or Tri-state Select<br>0 = Tri-state, 1 = REF/N Clock  |
| 6   | 0    | TEST_MODE  | Test Clock Mode Entry Control<br>0 = Normal operation, 1 = REF/N or Tri-state mode,  |
| 5   | HW   | FS_D   | FS_D reflects the value of the FS_D pin sampled on power-up.<br>0 = FS_D was LOW during VTT_PWRGD# assertion   |
| 4   | 1    | REF0   | REF Output Drive Strength<br>0 = High, 1 = Low   |
| 3   | 1    | PCI, PCIF and SRC clock outputs except those set to free running | SW PCI_STP# Function<br>0 = SW PCI_STP# assert, 1 = SW PCI_STP# deassert<br>When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses.<br>When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses. |
| 2   | HW   | FS_C   | FS_C Reflects the value of the FS_C pin sampled on power-up<br>0 = FS_C was LOW during VTT_PWRGD# assertion  |
| 1   | HW   | FS_B   | FS_B Reflects the value of the FS_B pin sampled on power-up<br>0 = FS_B was LOW during VTT_PWRGD# assertion  |
| 0   | HW   | FS_A   | FS_A Reflects the value of the FS_A pin sampled on power-up<br>0 = FS_A was LOW during VTT_PWRGD# assertion  |

**Byte 7: Vendor ID**

| Bit | @Pup | Name                | Description         |
|-----|------|---------------------|---------------------|
| 7   | 0    | Revision Code Bit 3 | Revision Code Bit 3 |
| 6   | 0    | Revision Code Bit 2 | Revision Code Bit 2 |
| 5   | 0    | Revision Code Bit 1 | Revision Code Bit 1 |
| 4   | 0    | Revision Code Bit 0 | Revision Code Bit 0 |
| 3   | 1    | Vendor ID Bit 3     | Vendor ID Bit 3     |
| 2   | 0    | Vendor ID Bit 2     | Vendor ID Bit 2     |
| 1   | 0    | Vendor ID Bit 1     | Vendor ID Bit 1     |
| 0   | 0    | Vendor ID Bit 0     | Vendor ID Bit 0     |

**Byte 8: Control Register 8**

| Bit | @Pup | Name       | Description  |
|-----|------|------------|--|
| 7   | 0    | CPU_SS     | Spread Selection for CPU PLL<br>0: -0.5% (peak to peak)<br>1: -1.0% (peak to peak) |
| 6   | 0    | CPU_DWN_SS | Spread Selection for CPU PLL<br>0: Down spread.<br>1: Center spread                |
| 5   | 0    | SRC_SS_OFF | SRC Spread Spectrum Enable<br>0 = Spread off, 1 = Spread on                        |
| 4   | 0    | SRC_SS     | Spread Selection for SRC PLL<br>0: -0.5% (peak to peak)<br>1: -1.0% (peak to peak) |
| 3   | 0    | RESERVED   | RESERVED, Set = 0  |
| 2   | 1    | USB        | 48-MHz Output Drive Strength<br>0 = 2x, 1 = 1x                                     |
| 1   | 1    | PCI        | 33-MHz Output Drive Strength<br>0 = 2x, 1 = 1x                                     |
| 0   | 0    | RESERVED   | RESERVED, Set = 0  |

**Byte 9: Control Register 9**

| Bit | @Pup | Name      | Description  |
|-----|------|-----------|--|
| 7   | 0    | DF_Limit2 | Dynamic Frequency Max threshold. These three bits will set the max allowed CPU frequency for Dynamic Frequency |
| 6   | 0    | DF_Limit1 |  |
| 5   | 0    | DF_Limit0 |  |
| 4   | 0    | DF_EN     | Dynamic Frequency Enable<br>0 = Disable, 1 = Enable  |
| 3   | 0    | FSEL_D    | SW Frequency selection bits. See <i>Table 1</i> .  |
| 2   | 0    | FSEL_C    |  |
| 1   | 0    | FSEL_B    |  |
| 0   | 0    | FSEL_A    |  |

**Byte 10: Control Register 10**

| Bit | @Pup | Name               | Description   |
|-----|------|--------------------|---|
| 7   | 0    | Recovery_Frequency | This bit allows selection of the frequency setting that the clock will be restored to once the system is rebooted<br>0: Use HW settings 1: Recovery N[8:0]  |
| 6   | 0    | Timer_SEL          | Timer_SEL selects the WD reset function at SRESET pin when WD time out.<br>0 = Reset and Reload Recovery_Frequency<br>1 = Only Reset  |
| 5   | 1    | Time_Scale         | Time_Scale allows selection of WD time scale<br>0 = 294 ms 1 = 2.34 s   |
| 4   | 0    | WD_Alarm           | WD_Alarm is set to "1" when the watchdog times out. It is reset to "0" when the system clears the WD_TIMER time stamp.  |
| 3   | 0    | WD_TIMER2          | Watchdog timer time stamp selection<br>000: Reserved (test mode)<br>001: 1 * Time_Scale<br>010: 2 * Time_Scale<br>011: 3 * Time_Scale<br>100: 4 * Time_Scale<br>101: 5 * Time_Scale<br>110: 6 * Time_Scale<br>111: 7 * Time_Scale |
| 2   | 0    | WD_TIMER1          |   |
| 1   | 0    | WD_TIMER0          |   |
|     |      |                    |   |



**Byte 10: Control Register 10 (continued)**

| Bit | @Pup | Name  | Description  |
|-----|------|-------|--|
| 0   | 0    | WD_EN | Watchdog timer enable, when the bit is asserted, Watchdog timer is triggered and time stamp of WD_Timer is loaded<br>0 = Disable, 1 = Enable |

**Byte 11: Control Register 11**

| Bit | @Pup | Name       | Description   |
|-----|------|------------|---|
| 7   | 0    | CPU_DAF_N7 | If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[E:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used. |
| 6   | 0    | CPU_DAF_N6 |   |
| 5   | 0    | CPU_DAF_N5 |   |
| 4   | 0    | CPU_DAF_N4 |   |
| 3   | 0    | CPU_DAF_N3 |   |
| 2   | 0    | CPU_DAF_N2 |   |
| 1   | 0    | CPU_DAF_N1 |   |
| 0   | 0    | CPU_DAF_N0 |   |

**Byte 12: Control Register 12**

| Bit | @Pup | Name       | Description  |
|-----|------|------------|--|
| 7   | 0    | CPU_DAF_N8 | If Prog_CPU_EN is set, the values programmed is in CPU_FSEL_N[8:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[E:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used. |
| 6   | 0    | CPU_DAF_M6 |  |
| 5   | 0    | CPU_DAF_M5 |  |
| 4   | 0    | CPU_DAF_M4 |  |
| 3   | 0    | CPU_DAF_M3 |  |
| 2   | 0    | CPU_DAF_M2 |  |
| 1   | 0    | CPU_DAF_M1 |  |
| 0   | 0    | CPU_DAF_M0 |  |

**Byte 13: Control Register 13**

| Bit | @Pup | Name   | Description                 |
|-----|------|--------|-----------------------------|
| 7   | 0    | SRC_N7 | SRC Dial-A-Frequency Bit N7 |
| 6   | 0    | SRC_N6 | SRC Dial-A-Frequency Bit N6 |
| 5   | 0    | SRC_N5 | SRC Dial-A-Frequency Bit N5 |
| 4   | 0    | SRC_N4 | SRC Dial-A-Frequency Bit N4 |
| 3   | 0    | SRC_N3 | SRC Dial-A-Frequency Bit N3 |
| 2   | 0    | SRC_N2 | SRC Dial-A-Frequency Bit N2 |
| 1   | 0    | SRC_N1 | SRC Dial-A-Frequency Bit N1 |
| 0   | 0    | SRC_N0 | SRC Dial-A-Frequency Bit N0 |

**Byte 14: Control Register 14**

| Bit | @Pup | Name     | Description   |
|-----|------|----------|---|
| 7   | 0    | SRC_N8   | SRC Dial-A-Frequency Bit N8   |
| 6   | 0    | SW_RESET | Software Reset.<br>When set the device will assert a reset signal on SRESET# upon completion of the block/word/byte write that set it. After asserting and deasserting the SRESET# this bit will self clear (set to 0). The SRESET# pin must be enabled by latching SRESET#_EN on VTT_PRWGD# to utilize this feature. |
| 5   | 0    | FS_[E:A] | FS_Override<br>0 = Select operating frequency by FS(E:A) input pins<br>1 = Select operating frequency by FSEL_(4:0) settings  |

**Byte 14: Control Register 14 (continued)**

| Bit | @Pup | Name        | Description   |
|-----|------|-------------|---|
| 4   | 0    | SMSW_SEL    | Smooth switch select<br>0: select CPU_PLL<br>1: select SRC_PLL. |
| 3   | 0    | RESERVED    | RESERVED, Set = 0   |
| 2   | 0    | RESERVED    | RESERVED, Set = 0   |
| 1   | 1    | PCIF        | Free running 33-MHz Output Drive Strength<br>0 = 2x, 1 = 1x     |
| 0   | 0    | Recovery_N8 | Watchdog Recovery Bit   |

**Byte 15: Control Register 15**

| Bit | @Pup | Name        | Description           |
|-----|------|-------------|-----------------------|
| 7   | 0    | Recovery N7 | Watchdog Recovery Bit |
| 6   | 0    | Recovery N6 | Watchdog Recovery Bit |
| 5   | 0    | Recovery N5 | Watchdog Recovery Bit |
| 4   | 0    | Recovery N4 | Watchdog Recovery Bit |
| 3   | 0    | Recovery N3 | Watchdog Recovery Bit |
| 2   | 0    | Recovery N2 | Watchdog Recovery Bit |
| 1   | 0    | Recovery N1 | Watchdog Recovery Bit |
| 0   | 0    | Recovery N0 | Watchdog Recovery Bit |

**Byte 16: Control Register 16**

| Bit | @Pup | Name                  | Description   |
|-----|------|-----------------------|---|
| 7   | 1    | REF1                  | REF1 Output Enable<br>0 = Disable, 1 = Enable   |
| 6   | 1    | USB48_1               | USB48_1 Output Enable<br>0 = Disable, 1 = Enable  |
| 5   | 0    | SRC_FREQ_SEL          | SRC Frequency selection<br>0: SRC frequency is selected via the FSE pin<br>1: SRC frequency is initially set to 167MHz. |
| 4   | 0    | RESERVED              | RESERVED, Set = 0   |
| 3   | 0    | SRC_SATA              | SATA PLL Spread Spectrum Enable<br>0 = Spread off, 1 = Spread on  |
| 2   | 0    | Prog_SRC_EN           | Programmable SRC frequency enable<br>0 = disabled, 1 = enabled.   |
| 1   | 0    | Prog_CPU_EN           | Programmable CPU frequency enable<br>0 = disabled, 1 = enabled.   |
| 0   | 1    | Watchdog Autorecovery | Watchdog Autorecovery Mode<br>0 = Disable (Manual), 1= Enable (Auto)  |

**Crystal Recommendations**

The CY28435 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28435 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

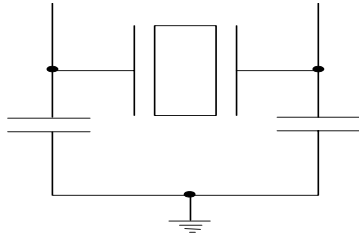
**Crystal Loading**

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 2 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

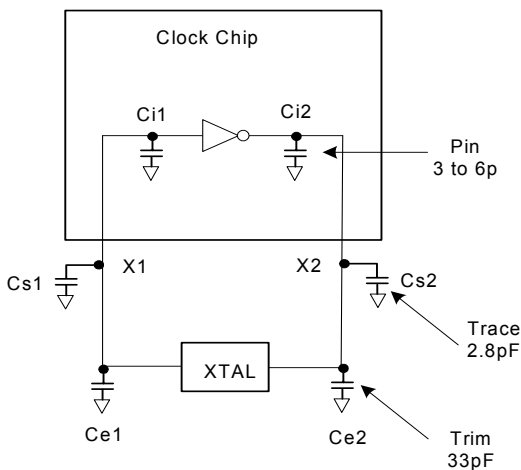
**Table 4. Crystal Recommendations**

| Frequency (Fund) | Cut | Loading  | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|------------------|-----|----------|----------|--------------|------------------|-----------------|------------------|------------------|--------------|
| 14.31818 MHz     | AT  | Parallel | 20 pF    | 0.1 mW       | 5 pF             | 0.016 pF        | 35 ppm           | 30 ppm           | 5 ppm        |


**Figure 2. Crystal Capacitive Clarification**

### Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.


**Figure 3. Crystal Loading Example**

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

#### Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

#### Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left( \frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

CL.....Crystal load capacitance

CLe.....Actual loading seen by crystal using standard value trim capacitors

Ce.....External trim capacitors

Cs.....Stray capacitance (terraced)

Ci.....Internal capacitance (lead frame, bond wires etc.)

CL.....Crystal load capacitance

CLe.....Actual loading seen by crystal using standard value trim capacitors

Ce.....External trim capacitors

Cs.....Stray capacitance (terraced)

Ci.....Internal capacitance (lead frame, bond wires etc.)

## Dynamic Frequency

**Dynamic Frequency** – Dynamic Frequency (DF) is a technique to increase the CPU frequency dynamically from any starting value. The user selects the starting point, either by HW, FSEL, or DAF then enables DF. After that, DF will dynamically change as determined by the value on the DF[2:0] pins.

**DF/PCI pin** – These PCI pins incorporate dual functions, either DF or PCI. The function is selected by the DF\_EN pin. When used as DF, these three pins will map to eight entries that correspond to different “N” values for Dynamic Frequency. Below is a table that list the combinations along with the increase in “N”.

| DOC[2:0] | DOC N value        |
|----------|--------------------|
| 000      | Original Frequency |
| 001      | +2                 |
| 010      | +6                 |
| 011      | +10                |
| 100      | +14                |
| 101      | +18                |
| 110      | +30                |
| 111      | +40                |

**DF\_EN bit** – This bit enables the DF mode. By default, it is not set. When set, the operating frequency is determined by DF[2:0] pins. Default = 0, (No DF)

**DF\_Limit bit** – There are three bits that allow the user to set an upper limit to prevent CPU runaway. In the event that the user uses DAF with DF, this feature will provide some safe guard so the CPU won't burn up.

## Dial-A-Frequency (CPU & SRC)

This feature allows the user to over clock their system by slowly stepping up the CPU or SRC frequency. When the programmable output frequency feature is enabled, the CPU and SRC frequencies are determined by the following equation

$$F_{cpu} = G * N/M \text{ or } F_{cpu} = G2 * N, \text{ where } G2 = G / M.$$

“N” and “M” are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively. “G” stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A]. See *Figure 1* for the Gear Constant for each Frequency selection. The PCI Express only allows user control of the N register, the M value is fixed and documented in *Figure 1*

In this mode, the user writes the desired N and M value into the DAF I2C registers. The user cannot change only the M value and must change both the M and the N values at the same time, if they require a change to the M value. The user may change only the N value if required.

### Associated Register Bits

**CPU\_DAF Enable** – This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU\_DAF\_N register. **Note:** the CPU\_DAF\_N and M register must contain valid values before CPU\_DAF is set. Default = 0, (No DAF).

**CPU\_DAF\_N** – There will be nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the frequency select table in *Figure 1*.

**CPU DAF M** – There will be 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, the allowable values for M are detailed in the frequency select table in section *Figure 1*

**SRC\_DAF Enable** – This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC\_DAF\_N register. **Note:** the SRC\_DAF\_N register must contain valid values before SRC\_DAF is set. Default = 0, (No DAF).

**SRC\_DAF\_N** – There is nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the frequency select table in *Figure 1*.

**Recovery** – The recovery mechanism during CPU DAF when the system locks up and the watchdog timer is enabled is determined by the “Watchdog Recovery Mode” and “Watchdog Auto recovery Enable” bits. The possible recovery methods are A) Auto, B) Manual (by Recovery N), C) HW, and D) No recovery - just send reset signal.

There is no recovery mode for SRC Dial a frequency.

## Software Frequency Select

This mode allows the user to select the CPU output frequencies using the Software Frequency select bits in the SMBUS register.

**FSEL** – There will be four bits (for 16 combinations) to select predetermined CPU frequencies from a table. The table selections are detailed in section *Figure 1*

**FS\_Override** – This bit allows the CPU frequency to be selected from HW or FSEL settings. By default, this bit is not set and the CPU frequency is selected by HW. When this bit is set, the CPU frequency is selected by the FSEL bits. Default = 0.

**Recovery** – The recovery mechanism during FSEL when the system locks up is determined by the “Watchdog Recovery Mode” and “Watchdog Auto recovery Enable” bits. The only possible recovery method is to Hardware Settings. Auto recovery or manual recovery can cause a wrong output frequency because the output divider may have changed with the selected CPU frequency and these recovery methods will not recover the original output divider setting.

## Smooth Switching

The Device contains 1 smooth switch circuit which is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by oversampling, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667  $\mu$ s. The frequency overshoot and undershoot will be less than 2%.

The Smooth Switch circuit can be assigned to either PLL via register byte 14 bit 4. By default the smooth switch circuit is assigned to the CPU PLL. Either PLL can still be overclocked when it does not have control of the smooth switch circuit but

it is not guaranteed to transition to the new frequency without large frequency glitches.

It is not recommended to enable overclocking and change the N values of both PLLs in the same SMBUS block write.

## Watchdog Timer

The Watchdog timer is used in the system in conjunction with overclocking. It is used to provide a reset to a system that has hung up due to overclocking the CPU and the Front side bus. The watchdog is enabled by the user and if the system completes its checkpoints, the system will clear the timer. However, when the timer runs out, there will be a reset pulse generated on the SRESET# pin for 20 ms that is used to reset the system.

When the Watchdog is enabled (WD\_EN = 1) the Watchdog timer will start counting down from a value of Watchdog\_timer \* time scale. If the Watchdog timer reaches 0 before the WD\_EN bit is cleared then it will assert the SRESET# signal and set the Watchdog Alarm bit to 1.

To use the watchdog the SRESET# pin must be enabled by SRESET\_EN pin being sampled LOW by VTT\_PWRGD# assertion during system boot up.

At any point if during the Watchdog timer countdown, if the time stamp or Watchdog timer bits are changed the timer will reset and start counting down from the new value.

After the Reset pulse, the watchdog will stay inactive until either:

1. A new time stamp or watchdog timer value is loaded.
2. The WD\_EN bit is cleared and then set again.

## Watchdog Register Bits

The following register bits are associated with the Watchdog timer:

**Watchdog Enable** – This bit (by default) is not set, which disables the Watchdog. When set, the Watchdog is enabled. Also, when there is a transition from LOW to HIGH, the timer reloads. Default = 0, disable

**Watchdog Timer** – There will be three bits (for seven combinations) to select the timer value. Default = 000, the value '000' is a reserved test mode.

**Watchdog Alarm** – This bit is a flag and when it is set, it indicates that the timer has expired. This bit is not set by default. When the bit is set, the user is allowed to clear. Default = 0.

**Watchdog Time Scale** – This bit selects the multiplier. When this bit is not set, the multiplier will be 250 ms. When set (by default), the multiplier will be 3s. Default = 1

**Watchdog Reset Mode** – This selects the Watchdog Reset Mode. When this bit is not set (by default), the Watchdog will send a reset pulse and reload the recovery frequency depends on Watchdog Recovery Mode setting. When set, it just send a reset pulse. Default = 0, Reset & Recover Frequency.

**Watchdog Recovery Mode** – This bit selects the location to recover from. One option is to recover from the HW settings (already stored in SMBUS registers for readback capability) and the second is to recover from a register called "Recovery N". Default = 0 (Recover from the HW setting)

**Watchdog Autorecovery Enable** – This bit by default is set and the recovered values are automatically written into the "Watchdog Recovery Register" and reloaded by the Watchdog function. When this bit is not set, the user is allowed to write to the "Watchdog Recovery Register". The value stored in the "Watchdog Recovery Register" will be used for recovery. Default = 1, Autorecovery.

**Watchdog Recovery Register** – This is a nine-bit register to store the watchdog N recovery value. This value can be written by the Auto recovery or User depending on the state of the "Watchdog Auto Recovery Enable bit".

## Watchdog Recovery Modes

There are three operating modes that require Watchdog recovery. The modes are Dial-A-Frequency (DAF), Dynamic Clocking (DF), or Frequency Select. There are 4 different recovery modes: the following diagram lists the operating mode and the recovery mode associated with it.

### *Recover to Hardware M,N, O*

When this recovery mode is selected, in the event of a Watchdog timeout, the original M,N, and O values that were latched by the HW FSEL pins at chip boot up should be reloaded.

### *Autorecovery*

When this recovery mode is selected, in the event of a Watchdog timeout, the M and N values stored in the Recovery M and N registers should be reloaded. The current values of M and N will be latched into the internal recovery M and N registers by the WD\_EN bit being set.

### *Manual Recovery*

When this recovery mode is selected, in the event of a Watchdog timeout, the N value as programmed by the user in the N recovery register, and the M value that is stored in the Recovery M register (not accessible by the user) should be restored. The current M value should be latched M recovery register by the WD\_EN bit being set.

### *No Recovery*

If no recovery mode is selected, in the event of a Watchdog time out, the device should just assert the SRESET# and keep the current values of M and N

## Software Reset

Software reset is a reset function which is used to send out a pulse from SRESET# pin. It is controlled by the SW\_RESET enable register bit. Upon completion of the byte/word/block write in which the SW\_RESET bit was set, the device will send a RESET pulse on the SRESET# pin. The duration of the SRESET# pulse should be the same as the duration of the SRESET# pulse after a Watchdog timer time out.

After the SRESET# pulse is asserted the SW\_RESET bit should be automatically cleared by the device.

## PD (Power-down) Clarification

The VTT\_PWRGD# /PD pin is a dual-function pin. During initial power-up, the pin functions as VTT\_PWRGD#. Once VTT\_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous

active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

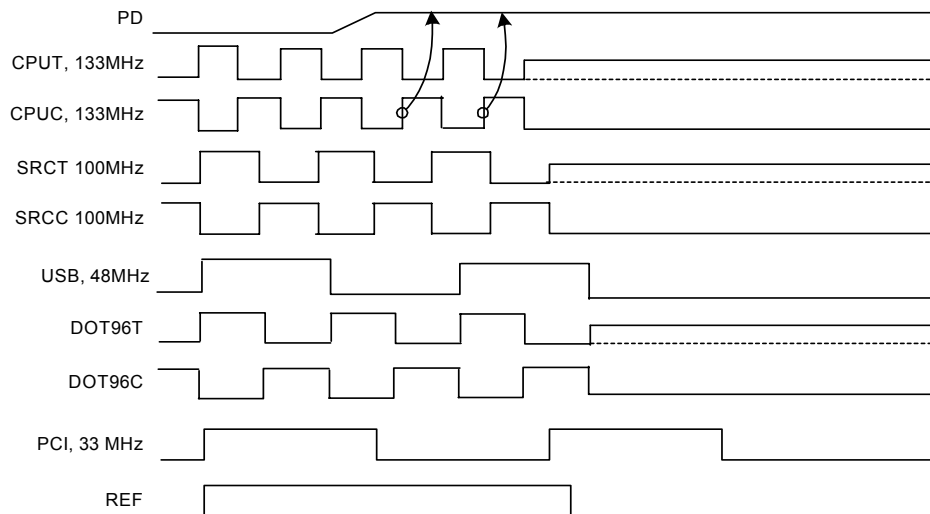
#### PD (Power-down) – Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held low on their next HIGH-to-LOW transition and differential clocks must be held high or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within four clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock output are held with "Diff clock" pin driven HIGH at  $2 \times I_{ref}$ , and "Diff clock#" tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then

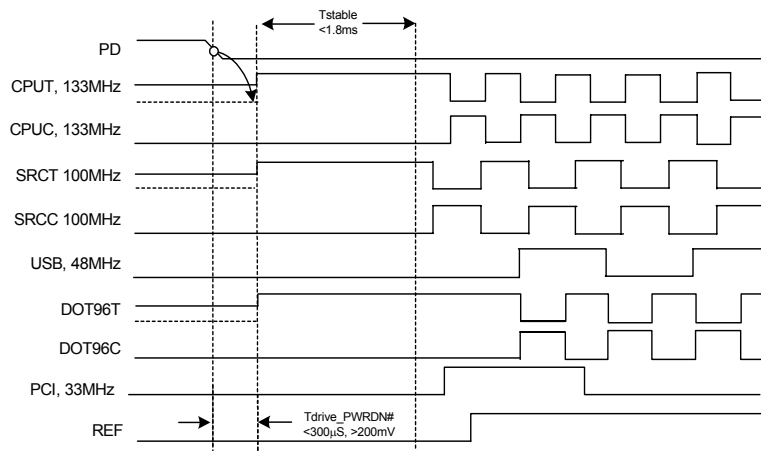
both the "Diff clock" and the "Diff clock#" are tri-state. Note the example below shows CPUC = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, 200, 266, 333 and 400 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted high in less than  $10 \mu s$  after asserting Vtt\_PwrGd#.

#### PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than  $300 \mu s$  of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. Below is an example showing the relationship of clocks coming up.

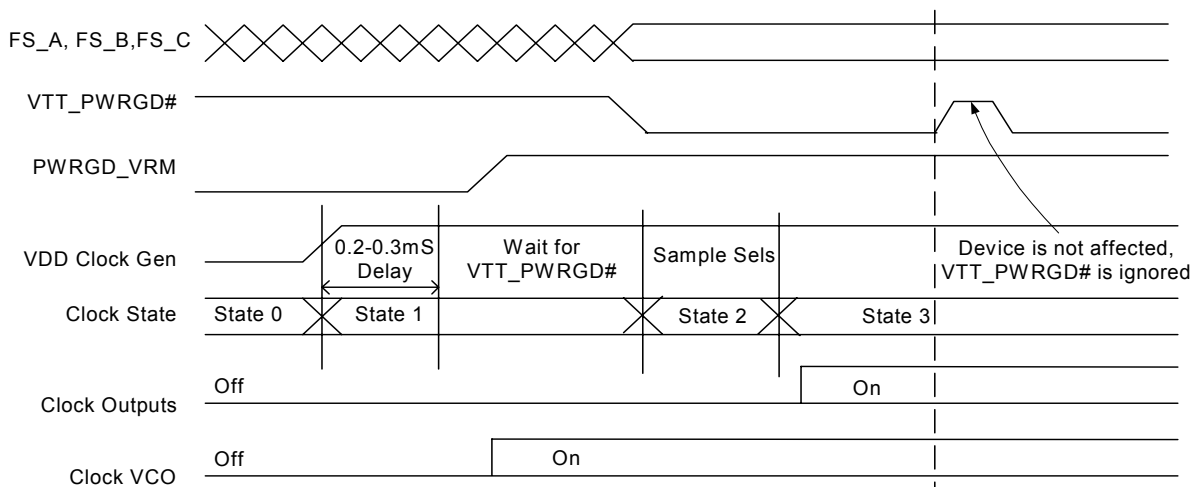


**Figure 4. Power-down Assertion Timing Waveform**

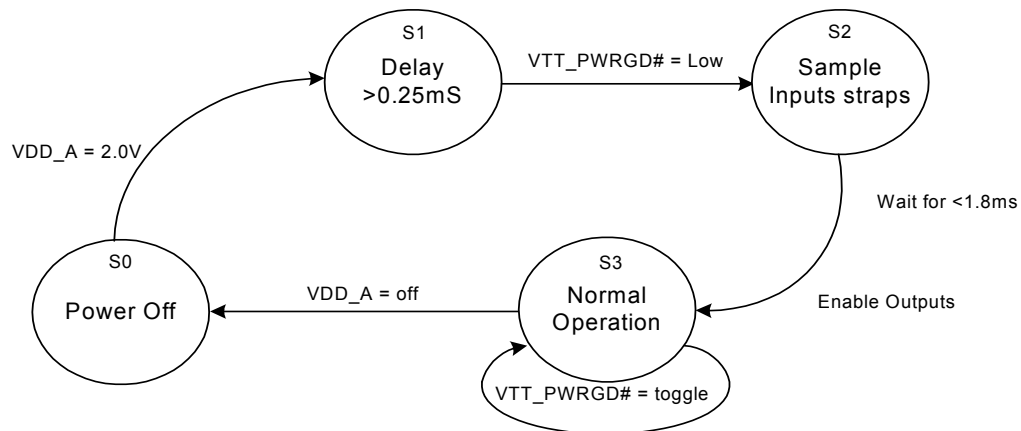


**Figure 5. Power-down Deassertion Timing Waveform**





**Figure 6. VTT\_PWRGD# Timing Diagram**



**Figure 7. Clock Generator Power-up/Run State Diagram**

**Absolute Maximum Conditions**

| Parameter     | Description                       | Condition                  | Min. | Max.           | Unit |
|---------------|-----------------------------------|----------------------------|------|----------------|------|
| $V_{DD}$      | Core Supply Voltage               |                            | -0.5 | 4.6            | V    |
| $V_{DD\_A}$   | Analog Supply Voltage             |                            | -0.5 | 4.6            | V    |
| $V_{IN}$      | Input Voltage                     | Relative to $V_{SS}$       | -0.5 | $V_{DD} + 0.5$ | VDC  |
| $T_S$         | Temperature, Storage              | Non-functional             | -65  | 150            | °C   |
| $T_A$         | Temperature, Operating Ambient    | Functional                 | 0    | 70             | °C   |
| $T_J$         | Temperature, Junction             | Functional                 | -    | 150            | °C   |
| $\theta_{JC}$ | Dissipation, Junction to Case     | Mil-STD-883E Method 1012.1 | -    | 20             | °C/W |
| $\theta_{JA}$ | Dissipation, Junction to Ambient  | JEDEC (JESD 51)            | -    | 60             | °C/W |
| $ESD_{HBM}$   | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015   | 2000 | -              | V    |
| UL-94         | Flammability Rating               | At 1/8 in.                 | V-0  |                |      |
| MSL           | Moisture Sensitivity Level        |                            | 1    |                |      |

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

| Parameter      | Description                     | Condition  | Min.           | Max.           | Unit    |
|----------------|---------------------------------|--|----------------|----------------|---------|
| All $V_{DD}$ s | 3.3V Operating Voltage          | $3.3 \pm 5\%$  | 3.135          | 3.465          | V       |
| $V_{IL2C}$     | Input Low Voltage               | SDATA, SCLK  | -              | 1.0            | V       |
| $V_{IH2C}$     | Input High Voltage              | SDATA, SCLK  | 2.2            | -              | V       |
| $V_{IL\_FS}$   | FS_[A:B,D:E] Input Low Voltage  |  | $V_{SS} - 0.3$ | 0.35           | V       |
| $V_{IH\_FS}$   | FS_[A:B,D:E] Input High Voltage |  | 0.7            | $V_{DD} + 0.5$ | V       |
| $V_{ILFS\_C}$  | FS_C Low Range                  |  | 0              | 0.35           | V       |
| $V_{IMFS\_C}$  | FS_C Mid Range                  |  | 0.7            | 1.7            | V       |
| $V_{IHFS\_C}$  | FS_C High Range                 |  | 2.1            | $V_{DD}$       | V       |
| $V_{IL}$       | 3.3V Input Low Voltage          |  | $V_{SS} - 0.3$ | 0.8            | V       |
| $V_{IH}$       | 3.3V Input High Voltage         |  | 2.0            | $V_{DD} + 0.3$ | V       |
| $I_{IL}$       | Input Low Leakage Current       | Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$   | -5             | -              | $\mu A$ |
| $I_{IH}$       | Input High Leakage Current      | Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$ | -              | 5              | $\mu A$ |
| $V_{OL}$       | 3.3V Output Low Voltage         | $I_{OL} = 1 \text{ mA}$                                    | -              | 0.4            | V       |
| $V_{OH}$       | 3.3V Output High Voltage        | $I_{OH} = -1 \text{ mA}$                                   | 2.4            | -              | V       |
| $I_{OZ}$       | High-impedance Output Current   |  | -10            | 10             | $\mu A$ |
| $C_{IN}$       | Input Pin Capacitance           |  | 3              | 5              | pF      |
| $C_{OUT}$      | Output Pin Capacitance          |  | 3              | 5              | pF      |
| $L_{IN}$       | Pin Inductance                  |  | -              | 7              | nH      |
| $V_{XIH}$      | Xin High Voltage                |  | $0.7V_{DD}$    | $V_{DD}$       | V       |
| $V_{XIL}$      | Xin Low Voltage                 |  | 0              | $0.3V_{DD}$    | V       |
| $I_{DD3.3V}$   | Dynamic Supply Current          | At max. load and freq. per <i>Figure 10</i>                | -              | 500            | mA      |
| $I_{PD3.3V}$   | Power-down Supply Current       | PD asserted, Outputs Driven                                | -              | 70             | mA      |
| $I_{PT3.3V}$   | Power-down Supply Current       | PD asserted, Outputs Tri-state                             | -              | 2              | mA      |



**AC Electrical Specifications**

| Parameter  | Description                                 | Condition   | Min.     | Max.     | Unit |
|--|---|---|----------|----------|------|
| <b>Crystal</b>   |   |   |          |          |      |
| T <sub>DC</sub>  | XIN Duty Cycle                              | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5     | 52.5     | %    |
| T <sub>PERIOD</sub>                                      | XIN Period                                  | When XIN is driven from an external clock source  | 69.841   | 71.0     | ns   |
| T <sub>R</sub> / T <sub>F</sub>                          | XIN Rise and Fall Times                     | Measured between 0.3V <sub>DD</sub> and 0.7V <sub>DD</sub>  | –        | 10.0     | ns   |
| T <sub>CCJ</sub>   | XIN Cycle to Cycle Jitter                   | As an average over 1-μs duration  | –        | 500      | ps   |
| L <sub>ACC</sub>   | Long-term Accuracy                          | Over 150 ms   | –        | 300      | ppm  |
| <b>CPU at 0.7V (SSC refers to –0.5% spread spectrum)</b> |   |   |          |          |      |
| T <sub>DC</sub>  | CPUT and CPUC Duty Cycle                    | Measured at crossing point V <sub>OX</sub>  | 45       | 55       | %    |
| T <sub>PERIOD</sub>                                      | 100-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 9.997001 | 10.00300 | ns   |
| T <sub>PERIOD</sub>                                      | 133-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 7.497751 | 7.502251 | ns   |
| T <sub>PERIOD</sub>                                      | 166-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 5.998201 | 6.001801 | ns   |
| T <sub>PERIOD</sub>                                      | 200-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 4.998500 | 5.001500 | ns   |
| T <sub>PERIOD</sub>                                      | 266-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 3.748875 | 3.751125 | ns   |
| T <sub>PERIOD</sub>                                      | 333-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 2.999100 | 3.000900 | ns   |
| T <sub>PERIOD</sub>                                      | 400-MHz CPUT and CPUC Period                | Measured at crossing point V <sub>OX</sub>  | 2.499250 | 2.500750 | ns   |
| T <sub>PERIODSS</sub>                                    | 100-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 9.997001 | 10.05327 | ns   |
| T <sub>PERIODSS</sub>                                    | 133-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 7.497751 | 7.539950 | ns   |
| T <sub>PERIODSS</sub>                                    | 166-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 5.998201 | 6.031960 | ns   |
| T <sub>PERIODSS</sub>                                    | 200-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 4.998500 | 5.026634 | ns   |
| T <sub>PERIODSS</sub>                                    | 266-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 3.748875 | 3.769975 | ns   |
| T <sub>PERIODSS</sub>                                    | 333-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 2.999100 | 3.015980 | ns   |
| T <sub>PERIODSS</sub>                                    | 400-MHz CPUT and CPUC Period, SSC           | Measured at crossing point V <sub>OX</sub>  | 2.499250 | 2.513317 | ns   |
| T <sub>PERIODAbs</sub>                                   | 100-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 9.912001 | 10.08800 | ns   |
| T <sub>PERIODAbs</sub>                                   | 133-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 7.412751 | 7.587251 | ns   |
| T <sub>PERIODAbs</sub>                                   | 166-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 5.913201 | 6.086801 | ns   |
| T <sub>PERIODAbs</sub>                                   | 200-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 4.913500 | 5.086500 | ns   |
| T <sub>PERIODAbs</sub>                                   | 266-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 3.663875 | 3.836125 | ns   |
| T <sub>PERIODAbs</sub>                                   | 333-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 2.914100 | 3.085900 | ns   |
| T <sub>PERIODAbs</sub>                                   | 400-MHz CPUT and CPUC Absolute period       | Measured at crossing point V <sub>OX</sub>  | 2.414250 | 2.585750 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 100-MHz CPUT and CPUC Absolute period, SSC  | Measured at crossing point V <sub>OX</sub>  | 9.912001 | 10.13827 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 133-MHz CPUT and CPUC Absolute period, SSC  | Measured at crossing point V <sub>OX</sub>  | 7.412751 | 7.624950 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 166-MHz CPUT and CPUC Absolute period, SSC  | Measured at crossing point V <sub>OX</sub>  | 5.913201 | 6.116960 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 200-MHz CPUT and CPUC Absolute period, SSC  | Measured at crossing point V <sub>OX</sub>  | 4.913500 | 5.111634 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 266-MHz CPUT and CPU C Absolute period, SSC | Measured at crossing point V <sub>OX</sub>  | 3.663875 | 3.854975 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 333-MHz CPUT and CPUC Absolute period, SSC  | Measured at crossing point V <sub>OX</sub>  | 2.914100 | 3.100980 | ns   |
| T <sub>PERIODSSAbs</sub>                                 | 400-MHz CPUT and CPUC Absolute period, SSC  | Measured at crossing point V <sub>OX</sub>  | 2.414250 | 2.598317 | ns   |
| T <sub>SKEW</sub>  | CPU0 to CPU1                                | Measured at crossing point V <sub>OX</sub>  | –        | 100      | ps   |

**AC Electrical Specifications** (continued)

| Parameter                       | Description                                | Condition   | Min.     | Max.                    | Unit |
|---------------------------------|--|---|----------|-------------------------|------|
| T <sub>CCJ</sub>                | CPUT/C Cycle to Cycle Jitter               | Measured at crossing point V <sub>OX</sub>  | –        | 85                      | ps   |
| L <sub>ACC</sub>                | Long Term accuracy                         | Measured using frequency counter over 0.15seconds.  | –        | 300                     | ppm  |
| T <sub>R</sub> / T <sub>F</sub> | CPUT and CPUC Rise and Fall Times          | Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V                                   | 175      | 700                     | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                         | Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> ) | –        | 20                      | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                        |   | –        | 125                     | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                        |   | –        | 125                     | ps   |
| V <sub>HIGH</sub>               | Voltage High                               | Math averages <i>Figure 10</i>  | 660      | 850                     | mV   |
| V <sub>LOW</sub>                | Voltage Low                                | Math averages <i>Figure 10</i>  | –150     | –                       | mV   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing       |   | 250      | 550                     | mV   |
| V <sub>OVS</sub>                | Maximum Overshoot Voltage                  |   | –        | V <sub>HIGH</sub> + 0.3 | V    |
| V <sub>UDS</sub>                | Minimum Undershoot Voltage                 |   | –0.3     | –                       | V    |
| V <sub>RB</sub>                 | Ring Back Voltage                          | See <i>Figure 10</i> . Measure SE   | –        | 0.2                     | V    |
| <b>SRC</b>                      |  |   |          |                         |      |
| T <sub>DC</sub>                 | SRCT and SRCC Duty Cycle                   | Measured at crossing point V <sub>OX</sub>  | 45       | 55                      | %    |
| T <sub>PERIOD</sub>             | 100-MHz SRCT and SRCC Period               | Measured at crossing point V <sub>OX</sub>  | 9.997001 | 10.00300                | ns   |
| T <sub>PERIODSS</sub>           | 100-MHz SRCT and SRCC Period, SSC          | Measured at crossing point V <sub>OX</sub>  | 9.997001 | 10.05327                | ns   |
| T <sub>PERIODAbs</sub>          | 100-MHz SRCT and SRCC Absolute Period      | Measured at crossing point V <sub>OX</sub>  | 9.872001 | 10.12800                | ns   |
| T <sub>PERIODSSAbs</sub>        | 100-MHz SRCT and SRCC Absolute Period, SSC | Measured at crossing point V <sub>OX</sub>  | 9.872001 | 10.17827                | ns   |
| T <sub>SKEW</sub>               | Any SRCT/C to SRCT/C Clock Skew            | Measured at crossing point V <sub>OX</sub>  | –        | 250                     | ps   |
| T <sub>CCJ</sub>                | SRCT/C Cycle to Cycle Jitter               | Measured at crossing point V <sub>OX</sub>  | –        | 85                      | ps   |
| L <sub>ACC</sub>                | SRCT/C Long Term Accuracy                  | Measured at crossing point V <sub>OX</sub>  | –        | 300                     | ppm  |
| T <sub>R</sub> / T <sub>F</sub> | SRCT and SRCC Rise and Fall Times          | Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V                                   | 175      | 700                     | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                         | Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> ) | –        | 20                      | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                        |   | –        | 125                     | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                        |   | –        | 125                     | ps   |
| V <sub>HIGH</sub>               | Voltage High                               | Math averages <i>Figure 10</i>  | 660      | 850                     | mV   |
| V <sub>LOW</sub>                | Voltage Low                                | Math averages <i>Figure 10</i>  | –150     | –                       | mV   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing       |   | 250      | 550                     | mV   |
| V <sub>OVS</sub>                | Maximum Overshoot Voltage                  |   | –        | V <sub>HIGH</sub> + 0.3 | V    |
| V <sub>UDS</sub>                | Minimum Undershoot Voltage                 |   | –0.3     | –                       | V    |
| V <sub>RB</sub>                 | Ring Back Voltage                          | See <i>Figure 10</i> . Measure SE   | –        | 0.2                     | V    |
| <b>PCI/PCIF</b>                 |  |   |          |                         |      |
| T <sub>DC</sub>                 | PCI Duty Cycle                             | Measurement at 1.5V   | 45       | 55                      | %    |
| T <sub>PERIOD</sub>             | Spread Disabled PCIF/PCI Period            | Measurement at 1.5V   | 29.99100 | 30.00900                | ns   |
| T <sub>PERIODSS</sub>           | Spread Enabled PCIF/PCI Period, SSC        | Measurement at 1.5V   | 29.9910  | 30.15980                | ns   |
| T <sub>PERIODAbs</sub>          | Spread Disabled PCIF/PCI Period            | Measurement at 1.5V   | 29.49100 | 30.50900                | ns   |
| T <sub>PERIODSSAbs</sub>        | Spread Enabled PCIF/PCI Period, SSC        | Measurement at 1.5V   | 29.49100 | 30.65980                | ns   |
| T <sub>HIGH</sub>               | PCIF and PCI high time                     | Measurement at 2.4V   | 12.0     | –                       | ns   |
| T <sub>LOW</sub>                | PCIF and PCI low time                      | Measurement at 0.4V   | 12.0     | –                       | ns   |
| Edge Rate                       | Rising edge rate                           | Measured between 0.8V and 2.0V  | 1.0      | 4.0                     | V/ns |

**AC Electrical Specifications** (continued)

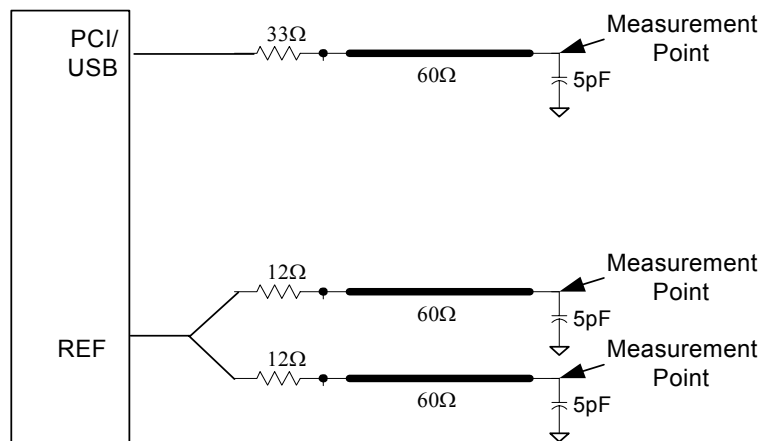
| Parameter                       | Description                           | Condition   | Min.     | Max.                    | Unit |
|---------------------------------|---------------------------------------|---|----------|-------------------------|------|
| Edge Rate                       | Falling edge rate                     | Measured between 0.8V and 2.0V  | 1.0      | 4.0                     | V/ns |
| T <sub>SKEW</sub>               | Any PCI clock to Any PCI clock Skew   | Measurement at 1.5V   | –        | 500                     | ps   |
| T <sub>CCJ</sub>                | PCIF and PCI Cycle to Cycle Jitter    | Measurement at 1.5V   | –        | 500                     | ps   |
| DOT                             |                                       |   |          |                         |      |
| T <sub>DC</sub>                 | DOT96T and DOT96C Duty Cycle          | Measured at crossing point V <sub>OX</sub>  | 45       | 55                      | %    |
| T <sub>PERIOD</sub>             | DOT96T and DOT96C Period              | Measured at crossing point V <sub>OX</sub>  | 10.41354 | 10.41979                | ns   |
| T <sub>PERIODAbs</sub>          | DOT96T and DOT96C Absolute Period     | Measured at crossing point V <sub>OX</sub>  | 10.16354 | 10.66979                | ns   |
| T <sub>CCJ</sub>                | DOT96T/C Cycle to Cycle Jitter        | Measured at crossing point V <sub>OX</sub>  | –        | 150                     | ps   |
| L <sub>ACC</sub>                | DOT96T/C Long Term Accuracy           | Measured at crossing point V <sub>OX</sub>  | –        | 100                     | ppm  |
| T <sub>LTJ</sub>                | Long Term jitter                      | Measurement taken from cross point V <sub>OX</sub> @1 μs  | –        | 700                     | ps   |
|                                 |                                       | Measurement taken from cross point V <sub>OX</sub> @10 μs   | –        | 700                     | ps   |
| T <sub>R</sub> / T <sub>F</sub> | DOT96T and DOT96C Rise and Fall Times | Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V                                   | 175      | 700                     | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                    | Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> ) | –        | 20                      | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                   |   | –        | 125                     | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                   |   | –        | 125                     | ps   |
| V <sub>HIGH</sub>               | Voltage High                          | Math averages <i>Figure 10</i>  | 660      | 850                     | mV   |
| V <sub>LOW</sub>                | Voltage Low                           | Math averages <i>Figure 10</i>  | –150     | –                       | mV   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing  |   | 250      | 550                     | mV   |
| V <sub>OVS</sub>                | Maximum Overshoot Voltage             |   | –        | V <sub>HIGH</sub> + 0.3 | V    |
| V <sub>UDS</sub>                | Minimum Undershoot Voltage            |   | –0.3     | –                       | V    |
| V <sub>RB</sub>                 | Ring Back Voltage                     | See <i>Figure 10</i> . Measure SE   | –        | 0.2                     | V    |
| USB                             |                                       |   |          |                         |      |
| T <sub>DC</sub>                 | Duty Cycle                            | Measurement at 1.5V   | 45       | 55                      | %    |
| T <sub>PERIOD</sub>             | Period                                | Measurement at 1.5V   | 20.83125 | 20.83542                | ns   |
| T <sub>PERIODAbs</sub>          | Absolute Period                       | Measurement at 1.5V   | 20.48125 | 21.18542                | ns   |
| T <sub>HIGH</sub>               | USB high time                         | Measurement at 2.4V   | 8.094    | 10.036                  | ns   |
| T <sub>LOW</sub>                | USB low time                          | Measurement at 0.4V   | 7.694    | 9.836                   | ns   |
| Edge Rate                       | Rising edge rate                      | Measured between 0.8V and 2.0V  | 1.0      | 2.0                     | V/ns |
| Edge Rate                       | Falling edge rate                     | Measured between 0.8V and 2.0V  | 1.0      | 2.0                     | V/ns |
| T <sub>CCJ</sub>                | Cycle to Cycle Jitter                 | Measurement at 1.5V   | –        | 200                     | ps   |
| T <sub>LTJ</sub>                | Long Term jitter                      | Measurement taken from cross point Vox@1us  | –        | 1.5                     | ns   |
|                                 |                                       | Measurement taken from cross point Vox@10us   | –        | 1.5                     | ns   |
|                                 |                                       | Measurement taken from cross point Vox@125us  | –        | 1.5                     | ns   |
| REF                             |                                       |   |          |                         |      |
| T <sub>DC</sub>                 | REF Duty Cycle                        | Measurement at 1.5V   | 45       | 55                      | %    |
| T <sub>PERIOD</sub>             | REF Period                            | Measurement at 1.5V   | 69.8203  | 69.8622                 | ns   |
| T <sub>PERIODAbs</sub>          | REF Absolute Period                   | Measurement at 1.5V   | 68.82033 | 70.86224                | ns   |
| T <sub>R</sub> / T <sub>F</sub> | REF Rise and Fall Times               | Measured between 0.8V and 2.0V  | 0.3      | 1.2                     | ns   |
| Edge Rate                       | Rising edge rate                      | Measured between 0.8V and 2.0V  | 1.0      | 4.0                     | V/ns |

**AC Electrical Specifications** (continued)

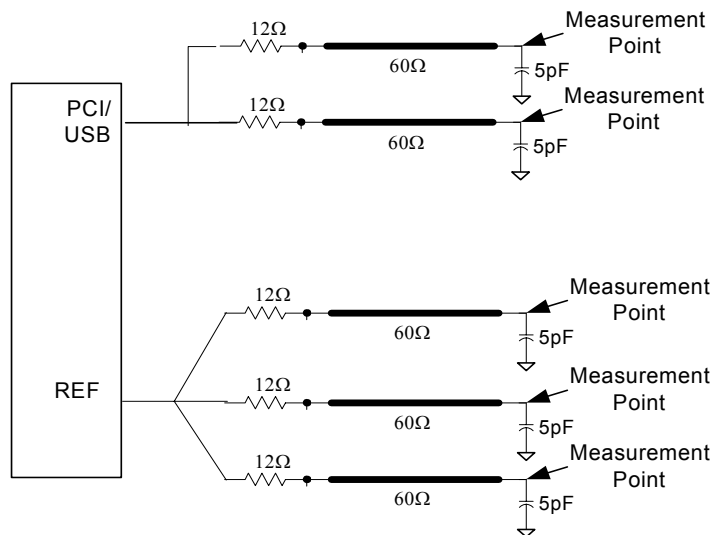
| Parameter                        | Description                       | Condition                      | Min. | Max. | Unit |
|----------------------------------|-----------------------------------|--------------------------------|------|------|------|
| Edge Rate                        | Falling edge rate                 | Measured between 0.8V and 2.0V | 1.0  | 4.0  | V/ns |
| T <sub>CCJ</sub>                 | REF Cycle to Cycle Jitter         | Measurement at 1.5V            | –    | 1000 | ps   |
| <b>ENABLE/DISABLE and SET-UP</b> |                                   |                                |      |      |      |
| T <sub>STABLE</sub>              | Clock Stabilization from Power-up |                                | –    | 1.8  | ms   |

**Test and Measurement Set-up**
**For PCI Single-ended Signals and Reference**

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.



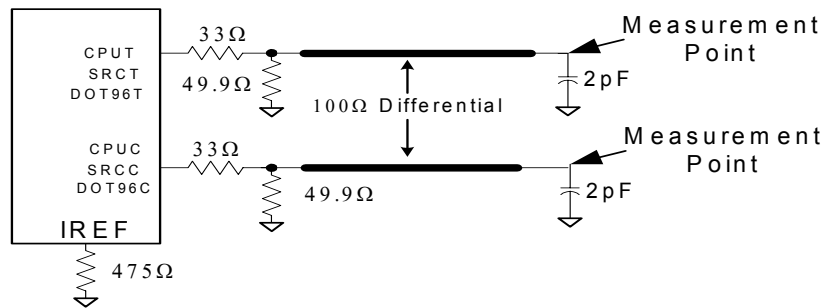
**Figure 8. Single-ended Load Configuration**



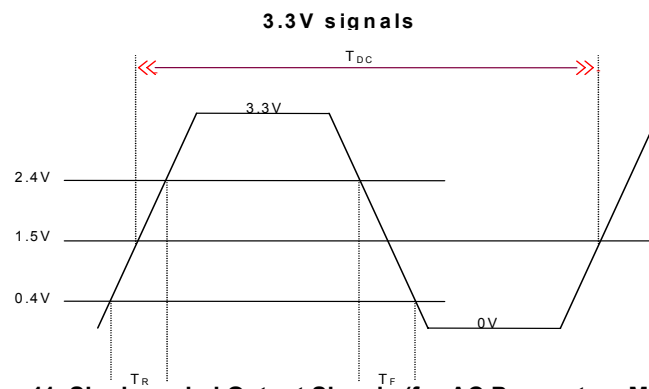
**Figure 9. Single-ended Load Configuration HIGH DRIVE OPTION**

### For Differential CPU, SRC and DOT96 Output Signals

The following diagram shows the test load configuration for the differential CPU and SRC outputs.



**Figure 10. 0.7V Single-ended Load Configuration**



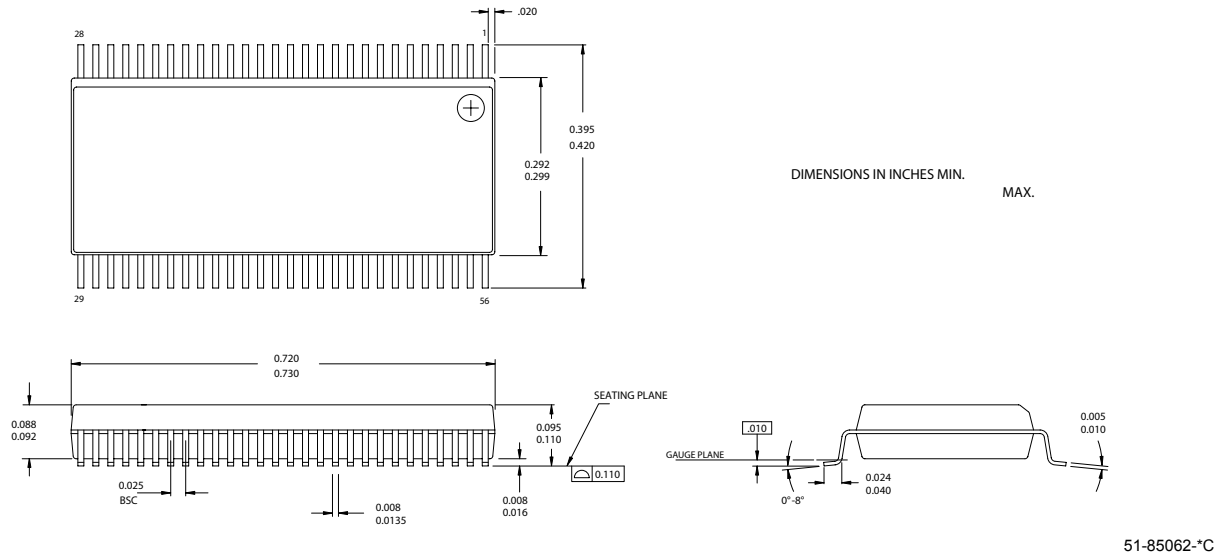
**Figure 11. Single-ended Output Signals (for AC Parameters Measurement)**

### Ordering Information

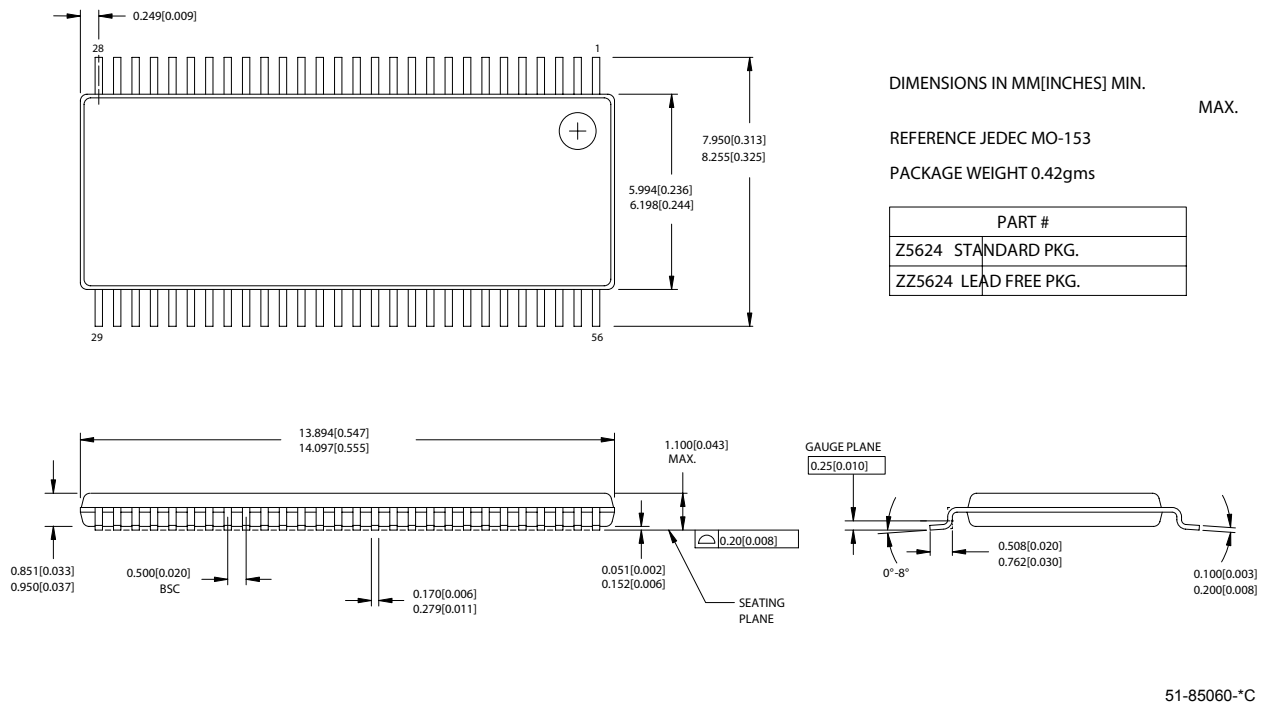
| Part Number      | Package Type                 | Product Flow           |
|------------------|------------------------------|------------------------|
| <b>Lead-free</b> |                              |                        |
| CY28435OXC       | 56-pin SSOP                  | Commercial, 0° to 85°C |
| CY28435OXCT      | 56-pin SSOP – Tape and Reel  | Commercial, 0° to 85°C |
| CY28435ZXC       | 56-pin TSSOP                 | Commercial, 0° to 85°C |
| CY28435ZXCT      | 56-pin TSSOP – Tape and Reel | Commercial, 0° to 85°C |

## Package Diagrams

### 56-Lead Shrunk Small Outline Package O56



### 56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



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**Document History Page**

| Document Title: CY28435 Clock Generator for Intel® Grantsdale Chipset<br>Document Number: 38-07664 |         |            |                 |   |
|--|---------|------------|-----------------|---|
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change   |
| **   | 214042  | See ECN    | RGL             | New Data Sheet  |
| *A   | 268575  | See ECN    | RGL             | Changed the tri-state test mode from 12 mA to 2 mA<br>Fixed the Single-ended load configuration diagram |
| *B   | 305734  | See ECN    | RGL             | Corrected the $T_{LTJ}$ for USB to 1.5 ns<br>Corrected the Frequency table values                       |