APExx12 Series

DATA SHEET

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1.0 General Description

The **APExx12** series are very low cost voice and melody synthesizer with 4-bits CPU. They have various features including 4-bits ALU, ROM, RAM, I/O ports, timers, clock generator, voice and melody synthesizer, and PWM (Direct drive) or D/A current outputs, etc. The audio synthesizer contains one voice-channel and two melody-channels. Furthermore, they consist of 27 instructions in these devices. With CMOS technology and halt function can minimize power dissipation. Their architectures are similar to RISC, with two stages of instruction pipeline. They allow all instructions to be executed in a single cycle, except for program branches and data table read instructions (which need two instruction cycles).

2.0 Features

(1) Single power supply can operate from 2.4V to 5.5V at 4MHz or 8MHz.

(2) Program ROM: 16k x 10 bits

(3) 1 set of 16-bits DPR can access up to 64k x 10 bits melody data memory space, and 1 set of 18-bits VPR can access up to 256k x 10 bits voice data memory space.

Product	Voice Duration (sec)	Voice Pointer (VPR)	ROM Size (10-bit)
APE0612	6	14-bits	20k
APE1012	10	15-bits	32k
APE1512	15	16-bits	48k
APE2012	20	16-bits	64k
APE3112	31	17-bits	96k
APE4112	41	17-bits	128k
APE5212	52	18-bits	160k
APE6312	63	18-bits	192k
APE7312	73	18-bits	224k
APE8412	84	18-bits	256k

(4) Data Registers:

a). 128 x 4-bit data RAM (00-7Fh)

b). Unbanked special function registers (SFR) range: 00h-2Fh

(5) I/O Ports:

a). PRA: 4-bits I/O Port A (10h) can be programmed to input/output individually. (Register control)

b). PRB: 4-bits I/O Port B (13h) can be configured to input/output individually. (Mask option)

c). PRD: 4-bits I/O Port D (15h) can be programmed to input/output individually. (Register control)

(6) On-chip clock generator: Resistive Clock Drive ***(RM)***

(7) Timer: 1-set Voice Interrupt (Timer0: a 9-bits auto-reload timer/counter).

(8) Stack: 2-level subroutine nesting.

(9) Built-in 4 Level Volume Control can be programmed.

(10) Built-in 8 Level DAC current output can be configured. (Mask option)

(11) Built-in IR Carry Output: Port B[1] can be configured as IR pin by 38k / 56kHz. (Mask option)

(12) External Reset: Port B[3] can be configured as reset pin. (Mask opton)

(13) HALT and Release from HALT function to reduce power consumption

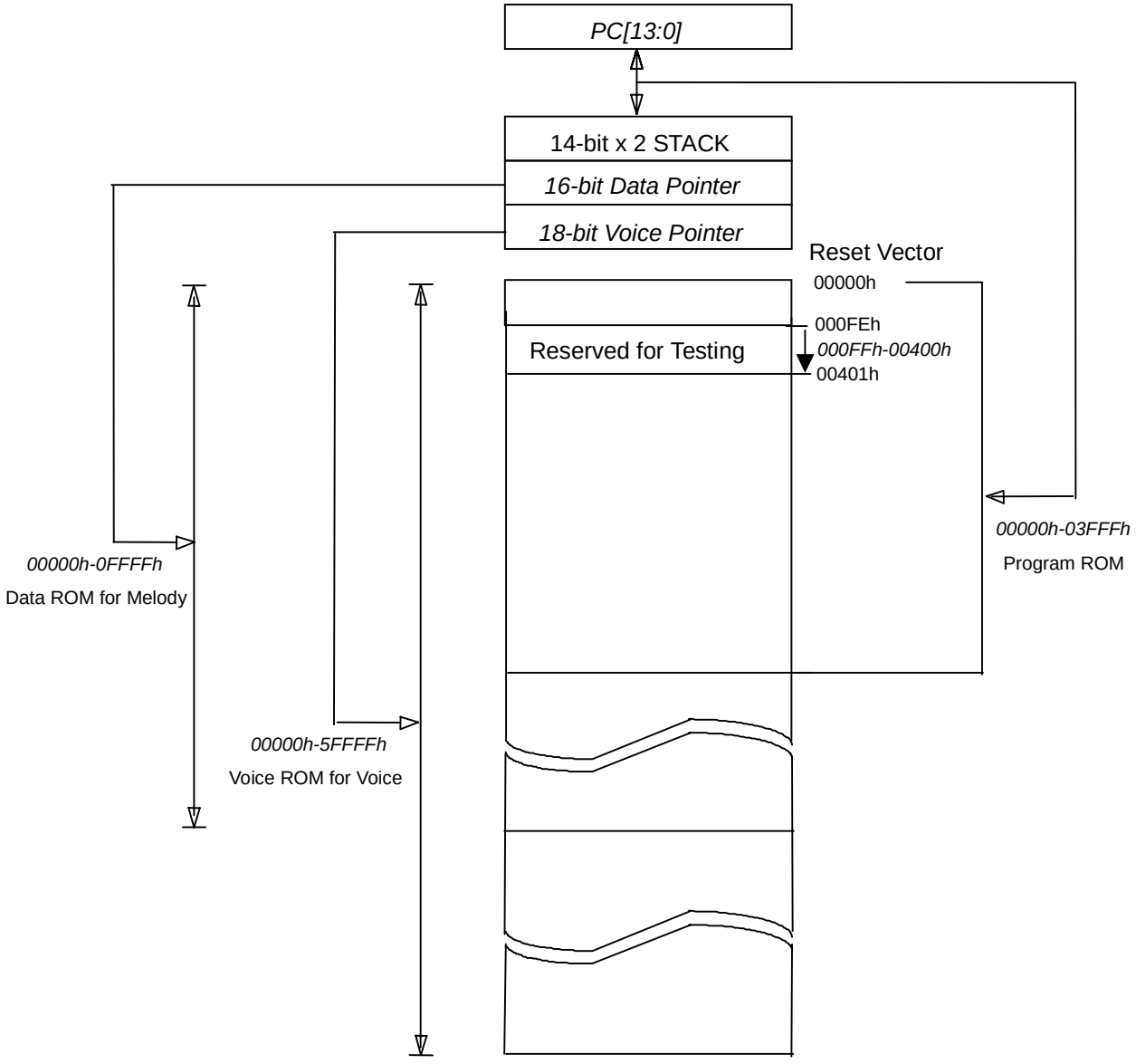
(14) Watch Dog Timer (***WDT***)

(15) Instruction: 1-cycle instruction except for table read and program branches which are 2-cycles

(16) Number of instruction: 27

(17) DAC: 1 channel voice and dual tone melody synthesizer (One 9-bits Cout or 8-bits PWM output).

FIGURE 1 : ROM Map of APExx12 Series



3.0 Pin Description

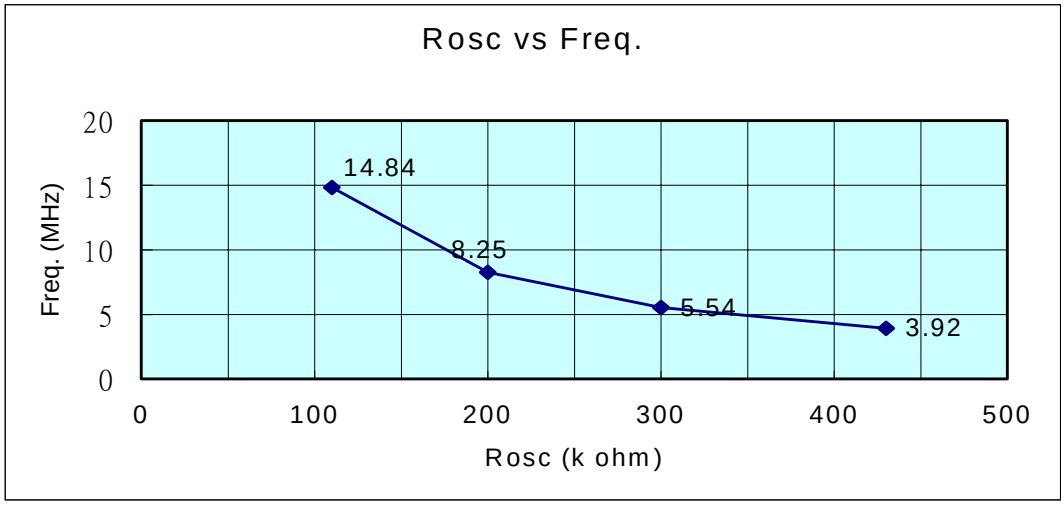
Pad Name	Pin Attr.	Description
PWM2/Cout	O	PWM2 output, or Current Output of Audio.
PWM1	O	PWM1 output.
Vdd1~2	Power	Power supply during operation.
PRA0~3 **PRD0~3**	I/O	I/O port can be programmed to input/output individually. Input type with weak pull-low or fix-input-floating capability. Buffer Output type.
PRB0, PRB2	I/O	I/O port can be configured to input/output individually. Input type with weak pull-low or fix-input-floating capability. Buffer Output type.
PRB1 / IR	I/O	I/O port can be configured to input/output individually. Input type with weak pull-low or fix-input-floating capability. Buffer Output type. *Mask option selected as an IR Carrier Output with 38k / 56kHz*
PRB3 / Reset	I/O	I/O port can be configured to input/output individually. Input type with weak pull-low or fix-input-floating capability. Buffer Output type. *Mask option selected as an external RESET pin with weak pull-low capability.*
OSC	I	RM mode Oscillator input
GND1~3	Power	Ground Potential

4.0 DC Characteristics

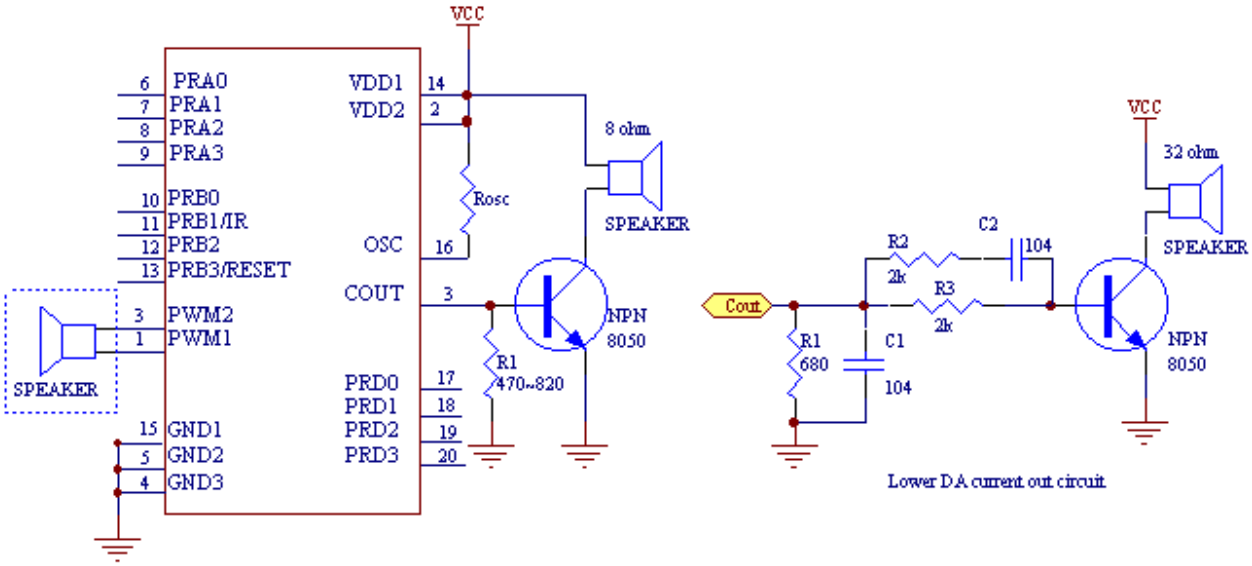
Symbol	Parameter		Vdd	Min.	Typ.	Max.	Unit	Condition
Vdd	Operating voltage			2.4	3	5.5	V	depending on Freq.
Isb	Supply current	Standby	3			1	uA	4MHz, RM, in HALT Mode
			4.5			1		
Iop		Operating	3		2		mA	4MHz, RM, IO Floating
			4.5		7			
Iih	Input current (Internal pull low)		3		3		uA	Input ports with weak pull-low
			4.5		10			
Ioh	Output-high current		3		-3		mA	4MHz, RM (IO ports)
			4.5		-10			
Iol	Output-low current		3		7			
			4.5		19			
Cout	DAC output current (8-level option)		3	0.8 ~ 4.8			mA	4MHz, RM (Full scale)
			4.5	0.9 ~ 6.5				
dF/F	Frequency stability			-5		5	%	$\frac{Fosc(3v- 2.4v)}{Fosc (3v)}$
dF/F	Fosc lot variation			-10		10	%	Vdd=3V, Rosc=180k, 4MHz

FIGURE 2 : Frequency vs. Rosc (at 3V)

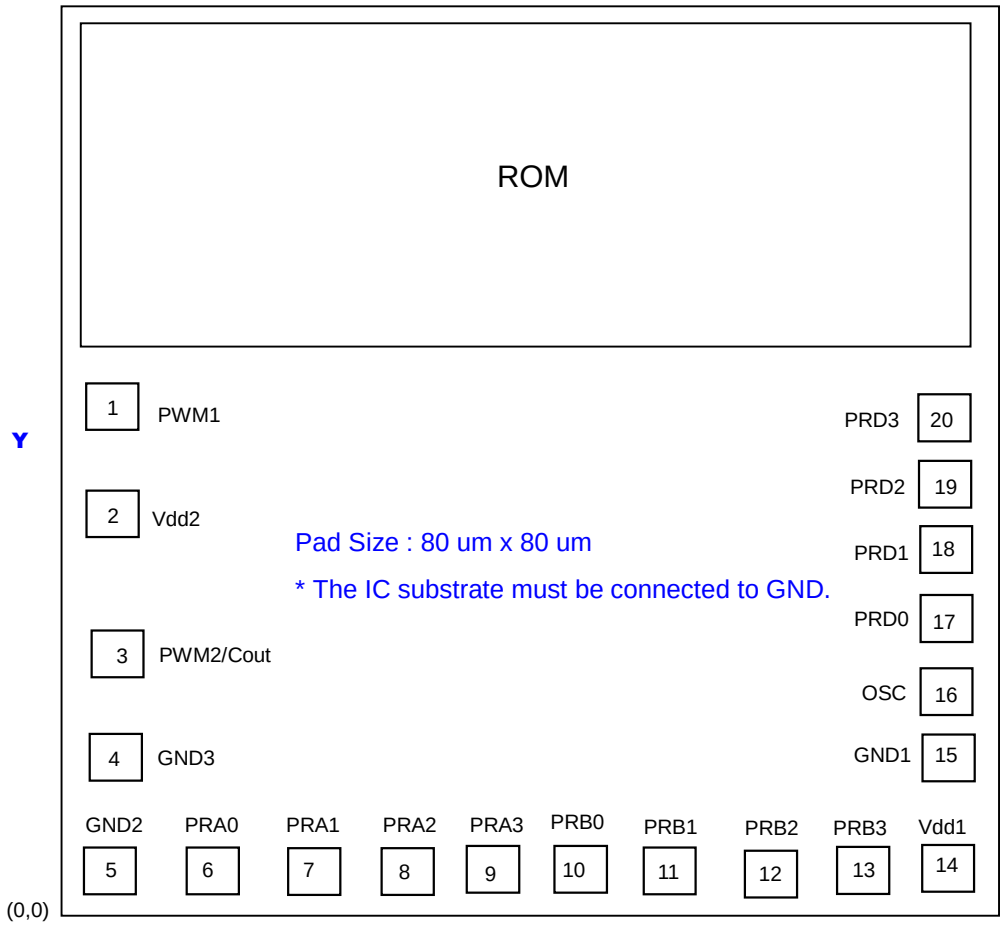
Resistor (Rosc ohms)	110k	200k	300k	430k
Frequency (MHz)	14.84	8.25	5.54	3.92



5.0 Application Circuit



6.0 Bonding Diagram



Pad #	Pad Name	X	Y	Pad #	Pad Name	X	Y
1	PWM1	57	865	**11**	PRB1	725	87
2	Vdd2	58	670	**12**	PRB2	835	87
3	PWM2/ Cout	58	386	**13**	PRB3	945	87
4	GND3	58	235	**14**	Vdd1	1055	87
5	GND2	65	87	**15**	GND1	1059	241
6	PRA0	175	87	**16**	OSC	1059	351
7	PRA1	285	87	**17**	PRD0	1059	461
8	PRA2	395	87	**18**	PRD1	1059	571
9	PRA3	505	87	**19**	PRD2	1059	681
10	PRB0	615	87	**20**	PRD3	1059	791

Chip Size :

APE0612 : 1230 um x 1530 um, APE1012 : 1230 um x 1530 um

APE1512 : 1230 um x 1758 um, APE2012 : 1230 um x 1758 um

APE3112 : 1230 um x 2210 um, APE4112 : 1230 um x 2210 um

APE5212 : 1230 um x 3116 um, APE6312 : 1230 um x 3116 um

APE7312 : 1230 um x 3116 um, APE8412 : 1230 um x 3116 um