Am8257/9557

Programmable DMA Controller

Advanced Micro Devices

Advanced MOS/LSI

DISTINCTIVE CHARACTERISTICS

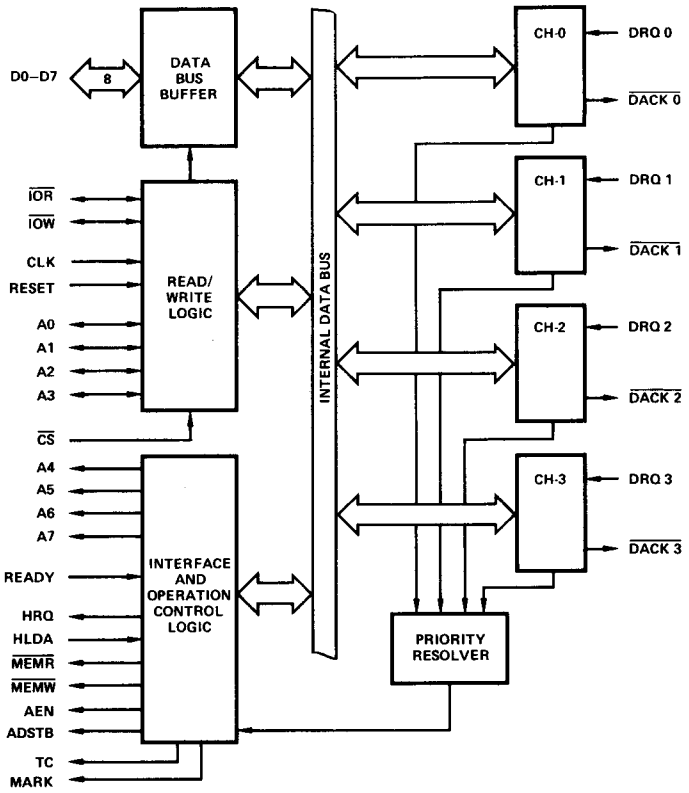
- **Direct plug-in replacement for Intel 8257**
- Four DMA channels with individual word count and address registers
- Single TTL clock
- Single +5V supply
- Standard 40 pin DIP
- Military version available
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am8257/9557 is a four channel Direct Memory Access controller which permits the high speed transfer of data directly between peripherals and memory in microcomputer systems. When a peripheral request is received, the Am8257/9557 resolves the request priority, issues a HOLD signal to the host processor, assumes control of the system busses, and generates the memory address necessary for the data transfer. It maintains a byte count for each channel and issues a terminal count signal upon completion of the programmed number of transfers.

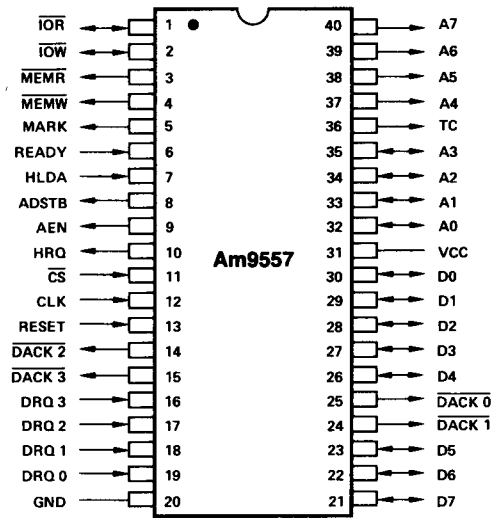
For improved functional and performance characteristics use the Am9517A Multimode DMA controller.

BLOCK DIAGRAM



MOS-474

CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

MOS-475

ORDERING INFORMATION

Package Type	Ambient Temperature	Order Number
Molded DIP	$0°C \leq T_A \leq +70°C$	AM9557PC/P8257
Hermetic DIP*		AM9557DC/D8257 AM9557CC/C8257
Hermetic DIP	$-55°C \leq T_A \leq +125°C$	AM9557DM

*Hermetic = Ceramic = DC = CC = D-40-1.

MAXIMUM RATINGS above which useful life may be impaired

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground	−0.5 to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC CHARACTERISTICS (T_A = 0 to 70°C, VCC = +5.0V ±5%, GND = 0V)

Parameters	Description	Test Conditions	Min	Max	Units
VIL	Input Low Voltage		−0.5	0.8	Volts
VIH	Input High Voltage		2.0	VCC+.5	Volts
VOL	Output Low Voltage	IOL = 1.6mA		0.45	Volts
VOH	Output High Voltage	IOH = −150μA for AB, DB and AEN IOH = −80μA for Others	2.4	VCC	Volts
VHH	HRQ Output High Voltage	IOH = −80μA	3.3	VCC	Volts
ICC	VCC Current Drain			120	mA
IIL	Input Leakage	VIN = VCC to 0V		±10	μA
IOFL	Output Leakage During Float	VOUT = VCC to 0V		±10	μA

CAPACITANCE (T_A = 25°C; VCC = GND = 0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
CIN	Input Capacitance	fc = 1MHz Unmeasured Pins Returned to GND			10	pF
CI/O	I/O Capacitance				20	pF

AC CHARACTERISTICS: PERIPHERAL (SLAVE) MODE (T_A = 0 to 70°C, VCC = 5.0V ±5%, GND = 0V, Note 1)

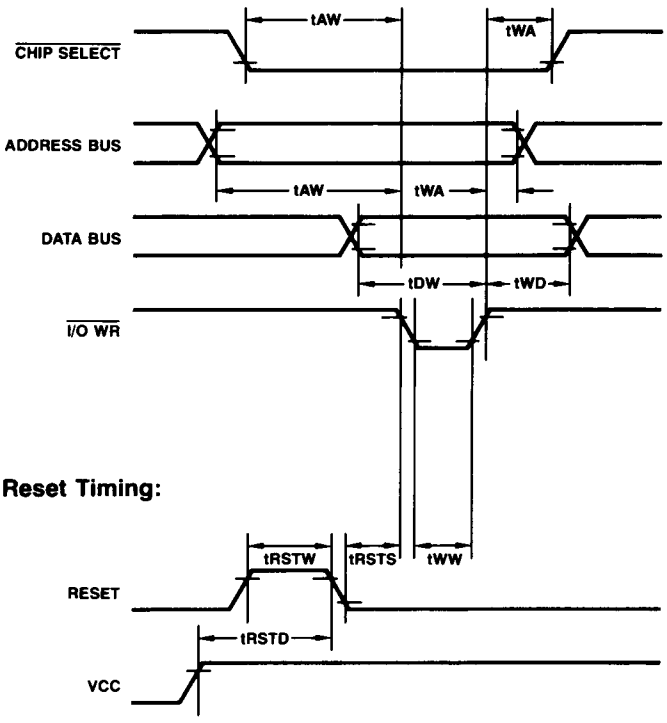
Am9080A Bus Parameters

Parameters	Description	Test Conditions	Min	Max	Units
Read Cycle:					
tAR	Address or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$		0		ns
tRA	Address of $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$		0		ns
tRD	Data Access from $\overline{RD}\downarrow$	Note 2	0	300	ns
tDF	DB → Float Delay from $\overline{RD}\uparrow$		20	150	ns
tRR	$\overline{RD}$ Width		250		ns
Write Cycle:					
tAW	Address Setup to $\overline{WR}\downarrow$		20		ns
tWA	Address Hold from $\overline{WR}\uparrow$		20		ns
tDW	Data Setup to $\overline{WR}\uparrow$		200		ns
tWD	Data Hold from $\overline{WR}\uparrow$		20		ns
tWW	$\overline{WR}$ Width		200		ns
Other Timing:					
tRSTW	Reset Pulse Width		300		ns
tRSTD	Power Supply↑ (VCC) Setup to Reset↓		500		μs
tr	Signal Rise Time			20	ns
tf	Signal Fall Time			20	ns
tRSTS	Reset to First $\overline{I/O}\overline{WR}$		2		tCY

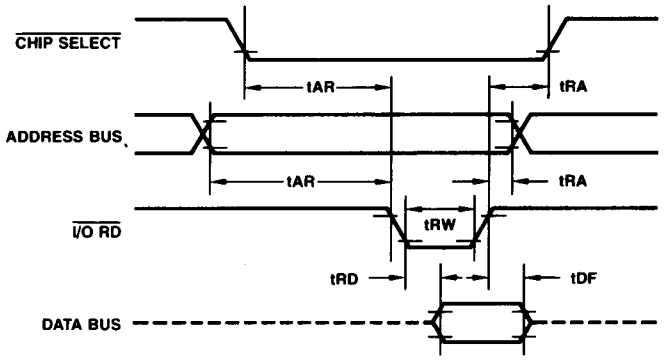
Notes: 1. All timing measurements are made at the following reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.
2. CL = 100pF.

PERIPHERAL MODE TIMING DIAGRAMS

Write Timing:



Read Timing:



Reset Timing:

Input Waveform for AC Tests:

AC CHARACTERISTICS: DMA (MASTER) MODE (T_A = 0 to 70°C, VCC = 5.0V ±5%, GND = 0V)

Timing Requirements

Parameters	Description	Min	Max	Units
tCY	Cycle Time (Period)	0.320	4	μs
tθ	Clock Active (High)	120	.8tCY	ns
tQS	DRQ↑ Setup to θ↓ (S1, S4)	120		ns
tQC	DRQ↓ Hold from CLK↓ (S1)	0		ns
tHS	HLDA↑ or ↓Setup to θ↓ (S1, S4)	100		ns
tRS	READY Setup Time to θ↑ (S3, Sw)	30		ns
tRH	READY Hold Time from θ↑ (S3, Sw)	20		ns

TRACKING PARAMETERS

Signals labeled as Tracking Parameters (footnotes 4-7 under AC Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50ns.

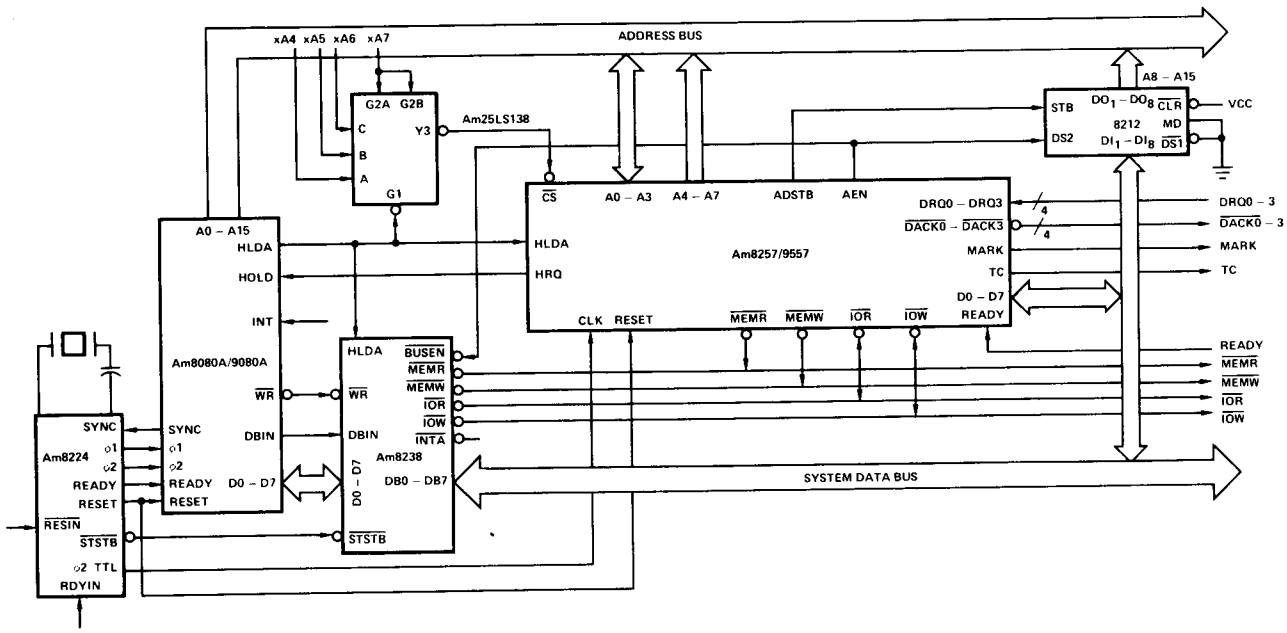
Suppose the following timing equation is being evaulated,

$$TA(MIN) + TB(MAX) \leq 150ns$$

and only minimum specifications exist for TA and TB. If TA(MIN) is used, and if TA and TB are tracking parameters, TB(MAX) can be taken as TB(MIN) + 50ns.

$$TA(MIN) + (TB(MIN)^* + 50ns) \leq 150ns$$

*If TA and TB are tracking parameters.



Basic DMA Configuration.

AC CHARACTERISTICS: DMA (MASTER) MODE (T_A = 0 to 70°C, VCC = 5.0V ±5%, GND = 0V)

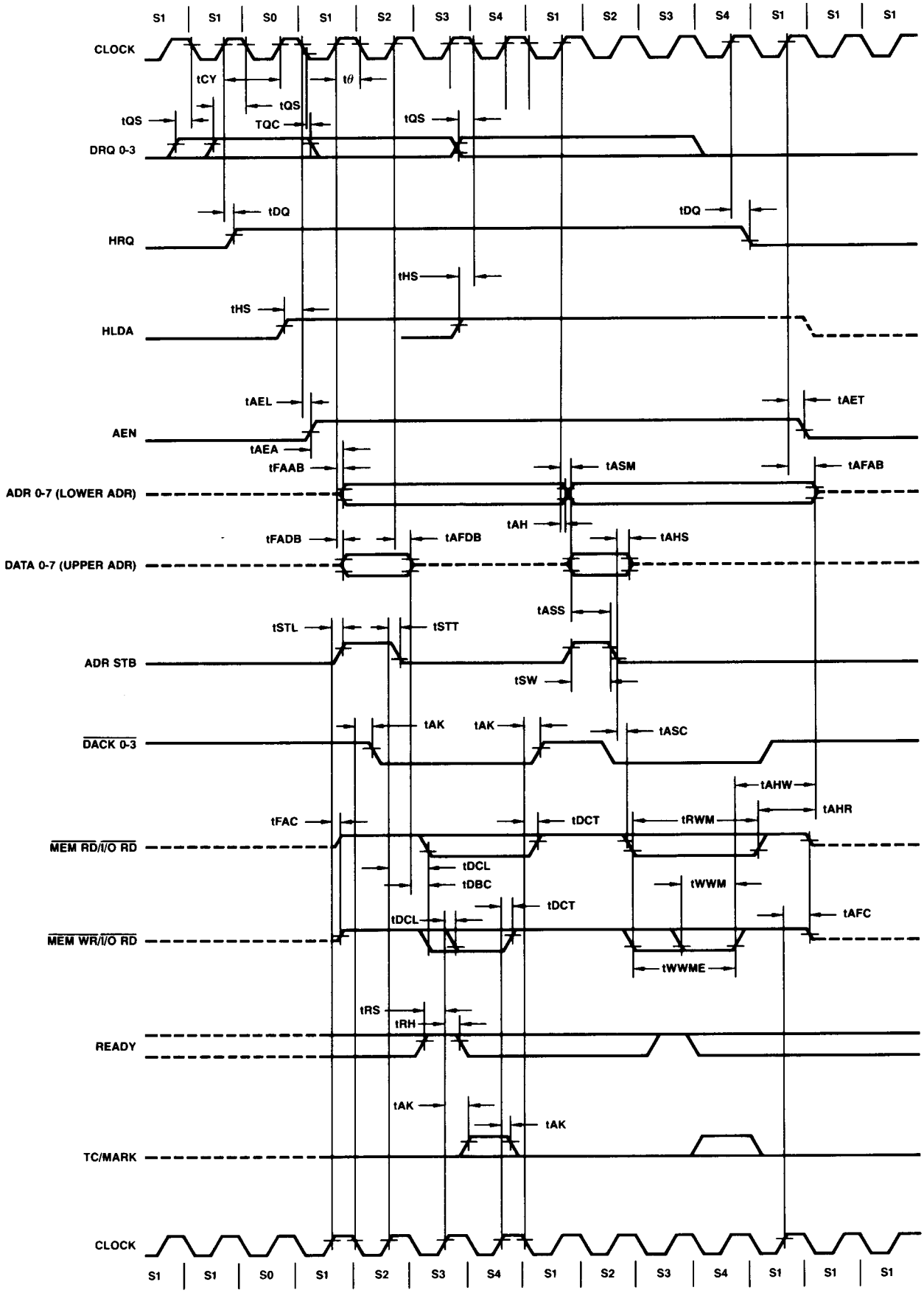
Timing Requirements

Parameters	Description	Min	Max	Units
tDQ	HRQ↑ or ↓Delay from θ↑ (SI, S4) (Measured at 2.0V) (Note 1)		160	ns
tDQ1	HRQ↑ or ↓Delay from θ↑ (SI, S4) (Measured at 3.3V) (Note 3)		250	ns
tAEL	AEN↑ Delay from θ↓ (S1) (Note 1)		300	ns
tAET	AEN↓ Delay from θ↑ (SI) (Note 1)		200	ns
tAEA	Address (AB) (Active) Delay from AEN↑ (S1) (Note 4)	20		ns
tFAAB	Address (AB) (Active) Delay from θ↑ (S1) (Note 2)		250	ns
tAFAB	Address (AB) (Float) Delay from θ↑ (SI) (Note 2)		150	ns
tASM	Address (AB) (Stable) Delay from θ↑ (S1) (Note 2)		250	ns
tAH	Address (AB) (Stable) Hold from θ↑ (S1) (Note 2)	tASM−50		ns
tAHR	Address (AB) (Valid) Hold from $\overline{RD}$↑ (S1, SI) (Note 4)	60		ns
tAHW	Address (AB) (Valid) Hold from $\overline{WR}$↑ (S1, SI) (Note 4)	300		ns
tFADB	Address (DB) (Active) Delay from θ↑ (S1) (Note 2)		300	ns
tAFDB	Address (DB) (Float) Delay from θ↑ (S2) (Note 2)	tSTT+20	250	ns
tASS	Address (DB) Setup to Address Stable↓ (S1, S2) (Note 4)	100		ns
tAHS	Address (DB) (Valid) Hold from Address Stable↓ (S2) (Note 4)	50		ns
tSTL	Address Stable↑ Delay from θ↑ (S1) (Note 1)		200	ns
tSTT	Address Stable↓ Delay from θ↑ (S2) (Note 1)		140	ns
tSW	Address Stable Width (S1, S2) (Note 4)	tCY−100		ns
tASC	$\overline{RD}$↓ or $\overline{WR}$ (Ext)↓ Delay from Address Stable↓ (S2) (Note 4)	70		ns
tDBC	$\overline{RD}$↓ or $\overline{WR}$ (Ext)↓ Delay from Address (DB) (Float) (S2) (Note 4)	20		ns
tAK	DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark↑ Delay from θ↑ (S3) and TC/Mark↓ Delay from θ↑ (S4) (Notes 1, 5)		250	ns
tDCL	$\overline{RD}$↓ or $\overline{WR}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{WR}$↓ Delay from θ↑ (S3) (Notes 2, 6)		200	ns
tDCT	$\overline{RD}$↑ Delay from θ↓ (S1, SI) and $\overline{WR}$↑ Delay from θ↑ (S4) (Notes 2, 7)		200	ns
tFAC	$\overline{RD}$ or $\overline{WR}$ (Active) from θ↑ (S1) (Note 2)		300	ns
tAFC	$\overline{RD}$ or $\overline{WR}$ (Float) from θ↑ (SI) (Note 2)		150	ns
tRWM	$\overline{RD}$ Width (S2, S1 or SI) (Note 4)	2tCY+tθ−50		ns
tWWM	$\overline{WR}$ Width (S3, S4) (Note 4)	tCY−50		ns
tWWME	$\overline{WR}$ (Ext) Width (S2, S4) (Note 4)	2tCY−50		ns

Notes: 1. Load = 1 TTL.
2. Load = 1 TTL + 50pF.
3. Load = 1 TTL + (RL = 3.3K), VOH = 3.3V.
4. Tracking Parameter.
5. ΔtAK < 50ns.
6. ΔtDCL < 50ns.
7. ΔtDCT < 50ns.

DMA MODE WAVEFORMS

CONSECUTIVE CYCLES AND BURST MODE SEQUENCE



Note: The clock waveform is duplicated for clarity. The Am8257/9557 requires only one clock input.

Figure 1. Consecutive Cycles and Burst Mode Sequence.

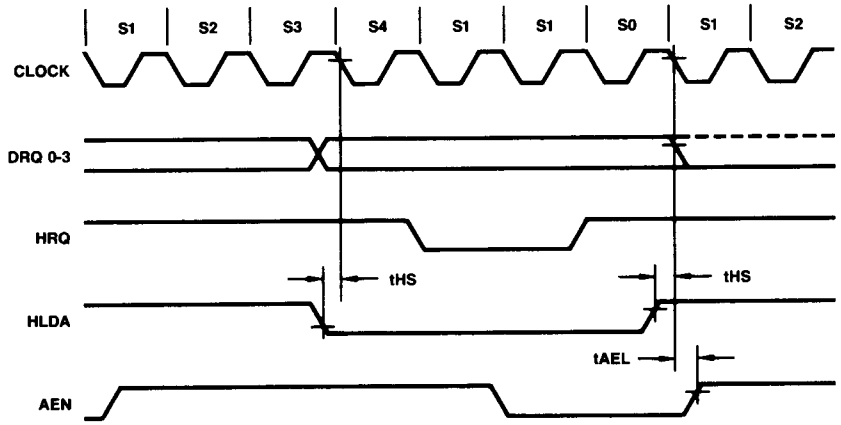


Figure 2. Control Override Sequence.

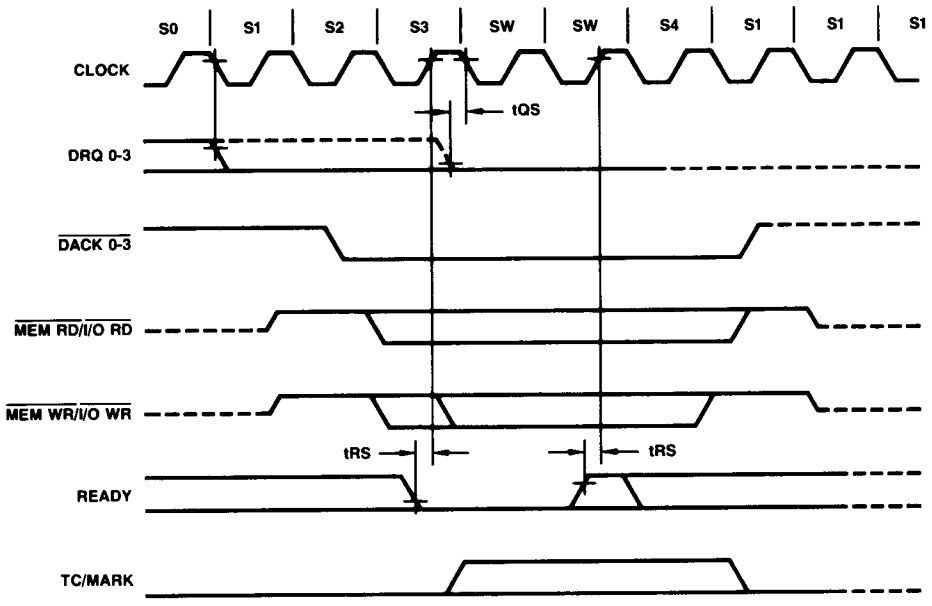
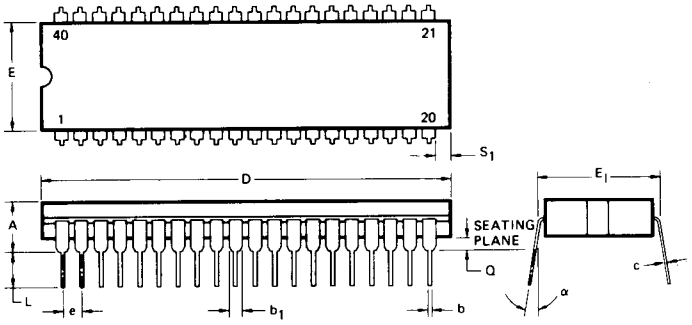


Figure 3. Not Ready Sequence.

PHYSICAL DIMENSIONS

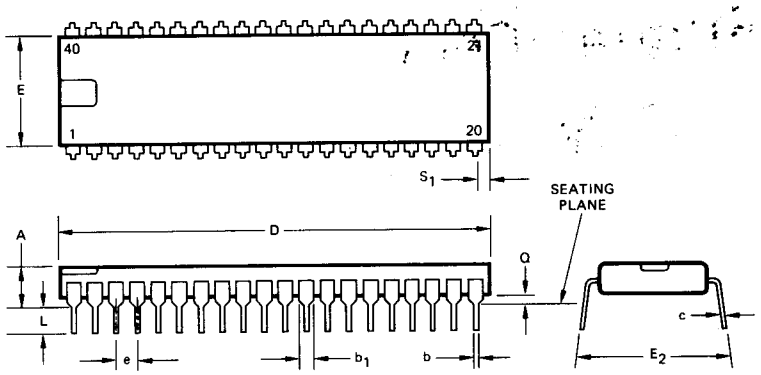
40-Pin Cerdip



Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.011
D	2.020	2.100
E	.510	.550
E_1	.600	.630
e	.090	.110
L	.120	.150
Q	.015	.060
S_1*	.005	
α	3°	13°

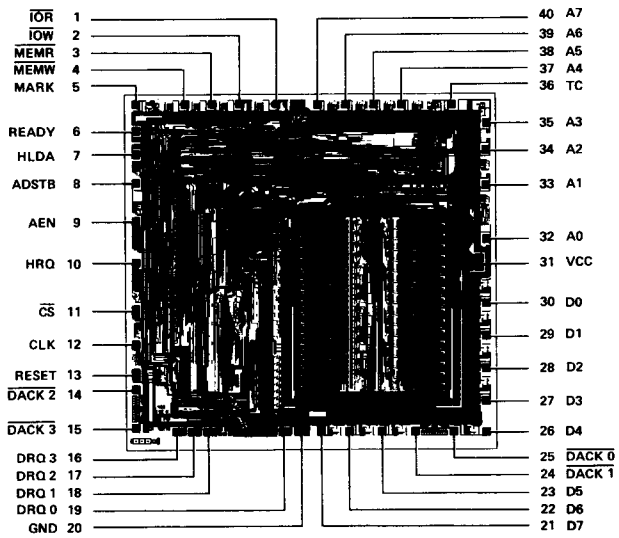
*From edge of end lead.

40-Pin Molded DIP



Reference Symbol	Inches	
	Min	Max
A	.150	.200
b	.015	.020
b_1	.055	.065
c	.009	.011
D	2.050	2.080
E	.530	.550
E_2	.585	.700
e	.090	.110
L	.125	.160
Q	.015	.060
S_1	.040	.070

Metallization and Pad Layout



ADVANCED MICRO DEVICES, INC.
901 Thompson Place
P.O. Box 453
Sunnyvale,
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306
TOLL FREE
(800) 538-8450